AN6870N

Dual Fluorescent Display Tube Driver with 18-Dot Peak Hold

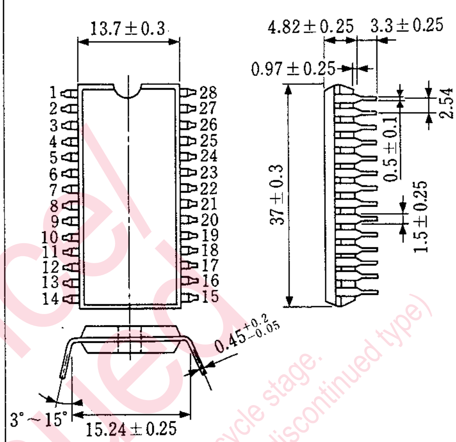
■ Outline

The AN6870 is an integrated circuit designed for driving the fluorescent display tube for bar graph display. It also drives total of 36 dots of 18 segments/2 channels in channel dynamic system and has a peak hold function.

■ Features

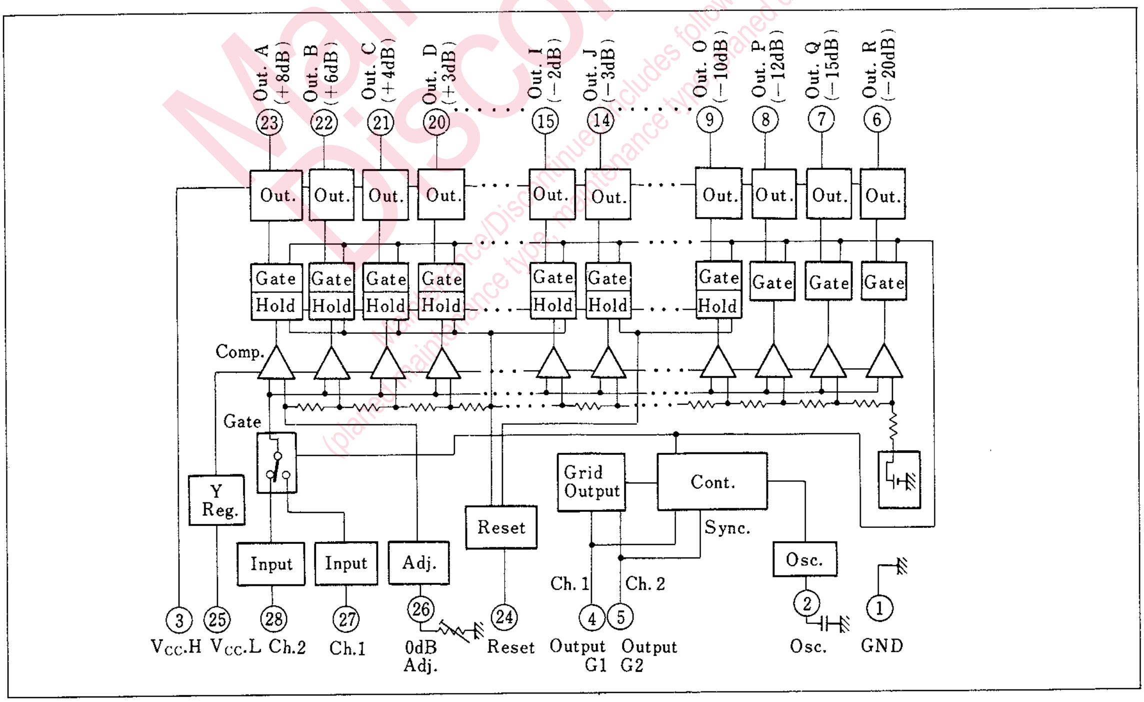
- 2-channel dynamic drive system
- 18-point/Ch. peak hold
- Reset terminal
- 0dB point adjustable
- Fewer external components

Unit : mm



28-Lead DIL Plastic Package

■ Block Diagram



■ Absolute Maximum Ratings (Ta=25℃)

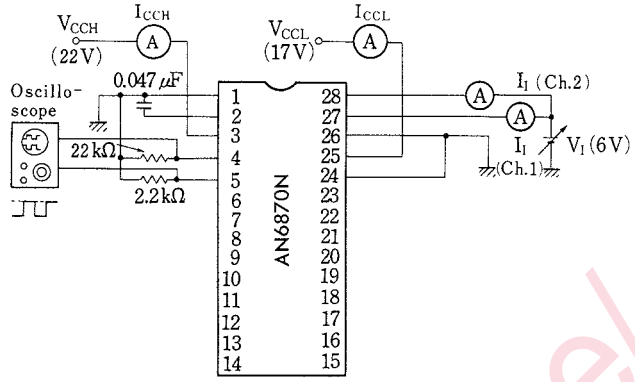
Item		Symbol	Rating		Unit
Voltage	Supply Voltage	V_{CCH}	24		V
	High Level Display Output Voltage	V_{OH}	V_{CCH}		V
	Low Level Display Output Voltage	V_{OL}	6		V
	High Level Grid Output Voltage	V_{OHG}	V_{CCH}		V
	Low Level Grid Output Voltage	V_{OLG}	6		V
	Signal Input Voltage	V_I	0	8	V
	Reset Pin Input Voltage	$V_{I(Reset)}$	0	8	V
	Adjust Pin Input Voltage	$V_{I(Abj.)}$	0	8	V
Current	Supply Current	I_{CC1}	18		mA
	High Level Display Output Current	$-I_{OH}$	3		mA
	High Level Grid Output Current	$-I_{OHG}$	20		mA
Power Dissipation		P_D	700		mW
Temperature	Operating Ambient Temperature	T_{opr}	−20～+75		℃
	Storage Temperature	T_{stg}	−55～+125		℃

Note) Voltage should not be applied to the connection Pin ② for oscillator capacitance.

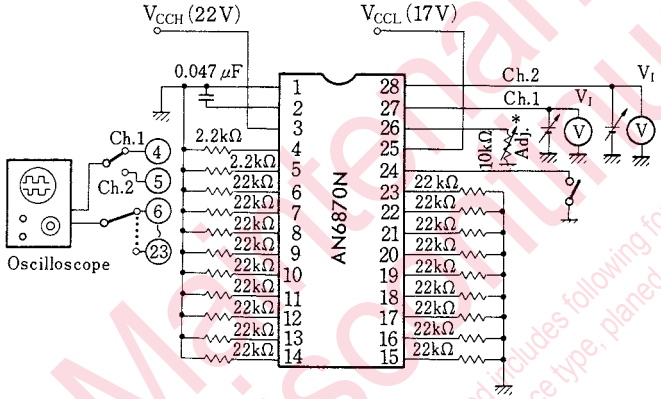
■ Electrical Characteristics (V_{CCH}=20V, V_{CCL}=15V, Ta=25℃)

Item		Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Signal Input Pin Current		I_I	1				5	μA
Output LED ON Input Level	A	V_{C+8}	2	RESET pin GND Adjust the output G LED ON level to be 3.7V.	6.32		6.90	V
	B	V_{C+6}	2		5.39		5.84	V
	C	V_{C+4}	2		4.66		4.99	V
	D	V_{C+3}	2		4.34		4.62	V
	E	V_{C+2}	2		4.04		4.33	V
	F	V_{C+1}	2		3.78		4.05	V
	G	V_{C+0}	2		3.56		3.78	V
	H	V_{C-1}	2		3.36		3.57	V
	I	V_{C-2}	2		3.14		3.38	V
	J	V_{C-3}	2		2.96		3.21	V
	K	V_{C-4}	2		2.79		3.06	V
	L	V_{C-5}	2		2.65		2.94	V
	M	V_{C-6}	2		2.52		2.81	V
	N	V_{C-8}	2		2.30		2.62	V
	O	V_{C-10}	2		2.13		2.47	V
	P	V_{C-12}	2		2.00		2.35	V
	Q	V_{C-15}	2		1.85		2.21	V
	R	V_{C-20}	2		1.68		2.06	V
Low Level Output Voltage		V_{OL}	2	R_L=22kΩ	0		0.5	V
High Level Output Voltage		V_{OH}	2	R_L=22kΩ	18	19	20	V
Low Level Grid Output Voltage		V_{OLG}	1	R_L=2.2kΩ	0		0.5	V
High Level Grid Output Voltage		V_{OHG}	1	R_L=2.2kΩ	18	19	20	V
Low Level Reset Input Current		$-I_{ILR}$	3	V_{24-1}=0			1.5	mA
High Level Reset Output Current		I_{IHR}	4	V_{24-1}=5V			1.5	mA
Low Level Adjust Input Current		$-I_{ILA}$	3	V_{26-1}=0	0.54			mA
High Level Adjust Input Voltage		V_{IHA}	4	I_{26}=0	7.7		9	V
Supply Current		I_{CCH}	1		3		10	mA
Supply Current		I_{CCL}	1		0		33	mA
Oscillator Pin Current		$-I_{OSC}$	3	V_{2-1}=0	25		60	μA

Test Circuit 1 (I_I, V_{OLG}, V_{OHG}, I_{CCH}, I_{CCL})

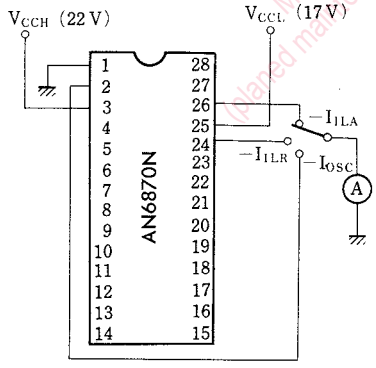


Test Circuit 2 (V_{C+8}~V_{C-20}, V_{OL}, V_{OH})

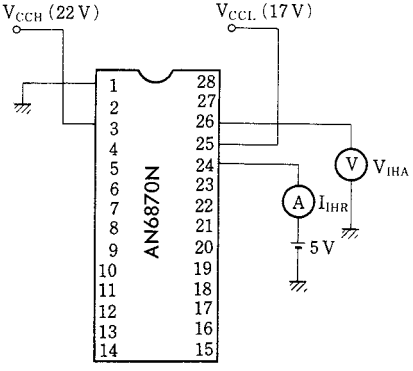


*Measurement is made for V_{C-18}~V_{C-20} after adjusting adj. volume.

Test Circuit 3 ($-I_{ILR}$, $-I_{ILA}$, $-I_{OSC}$)

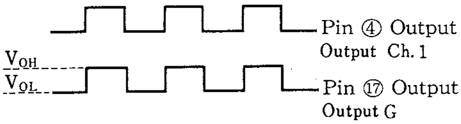


Test Circuit 4 (I_{IHR}, V_{IHA})



1. Adjusting Method

① At Test Circuit B, set V_I and Ch. 1 to 3.7 V and V_I and Ch. 2 to 0V. Pin④ and Pin⑰ are observed with an osicilloscope.

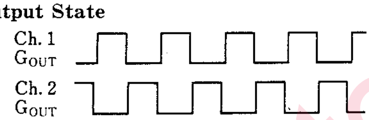


②Turn slowly the Adj. VR and stop when the state where no output is generated at Pin ⑰ becomes the state as shown in the figure above.

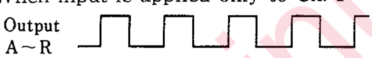
2. Measuring Method

Observe the level output pin to be measured and channel grid output pin (Output Ch. 1: ④, Output Ch. 2: ⑤) with an osilloscope and lower the input voltage V_1 gradually from the state where no output is generated at the output pin ("L" level). When output is generated at the output pin, stop the input voltage. The input voltage V_1 at this time is the comparator voltage Vcn. In this case, the input voltage V_1 of channel which has not been measured is assumed to be 0V.

3. Output State



(1)When input is applied only to Ch. 1



(2)When input is applied only to Ch.2

(3)When input is applied to both Ch. 1 and Ch. 2

4. Operational Explanation

This IC is used to drive a fluorescent display tube for bar graph display. It also drives a total of 36 dots of 18 segments/2 channels in channel dynamic system and has a peak hold function.

· Input Signals (Ch. 1: Pin ㉗, Ch. 2: Pin ㉘)
18 comparators with present reference level are available and inverted from the low level side sequentially in accordance with input signal level. These comparators are selected by two input signals and a channel signal at the gate circuit, being connected to another comparator.

· Input Signals (Pins ⑥～㉓)
When the comparator is inverted, the output level becomes "H" level, causing the flourescent display tube to light. Pin name, pin No. and display level are as follows.

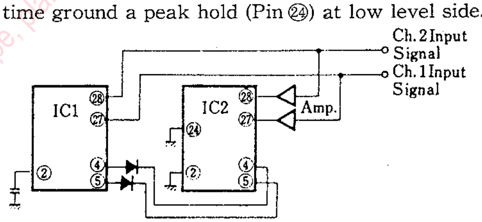
Output Pin	R	Q	P	O	N	M	L	K	J
Pin No.	6	7	8	9	10	11	12	13	14
Input Level (dB)	−20	−15	−12	−10	−8	−6	−5	−4	−3
Output Pin	I	H	G	F	E	D	C	B	A
Pin No.	15	16	17	18	19	20	21	22	23
Input Level (dB)	−2	−1	0	1	2	3	4	6	8

· Adjustment (Pin ㉖)
In adjustment, only voltage can be varied by the external variable resistor without changing each reference level.

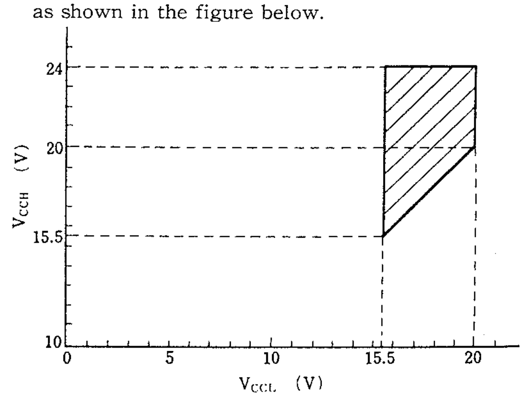
· Peak Hold (Pin ㉔)
A peak hold function is provided at level higher than the fourth level from the bottom. Max. peak point after peak hold is kept lighting with each channel. This function is configured so that output can be generated from only single memory owing to the internal 15-level × 2-channel memory. In this peak hold function, when the reset pin (Pin ㉔) is made "H" level, the memory starts its operation, while, when grounded, all memory is reset. Then, a peak hold is not to be applied.

· Dynamic LED ON
This IC executes a dynamic driving between Ch. 1 and Ch. 2. Connecting with Pin ② causes the internal oscillator to operate and generate a switching pulse. With this pulse, the input signal gate is switched. The oscillator also generates a grid switching pulse. When this pulse (Ch. 1: Pin ④, Ch. 2: Pin ⑤) is output, each "H" level channel is lit up.

· Driving other than 18-dot/Ch.
Two or more AN6870Ns are used to increase the number of dots for fluorescent display tube. When synchronization with a switching pulse is required, one AN6870N with capacitance is oscillated. For the other one, grounding the oscillator capacitance pin (Pin ②). IC grid output being oscillated is applied via diode to the IC grid output pin which does not oscillate. In this case, set appropriate signal input level and at the same time ground a peak hold (Pin ㉔) at low level side.

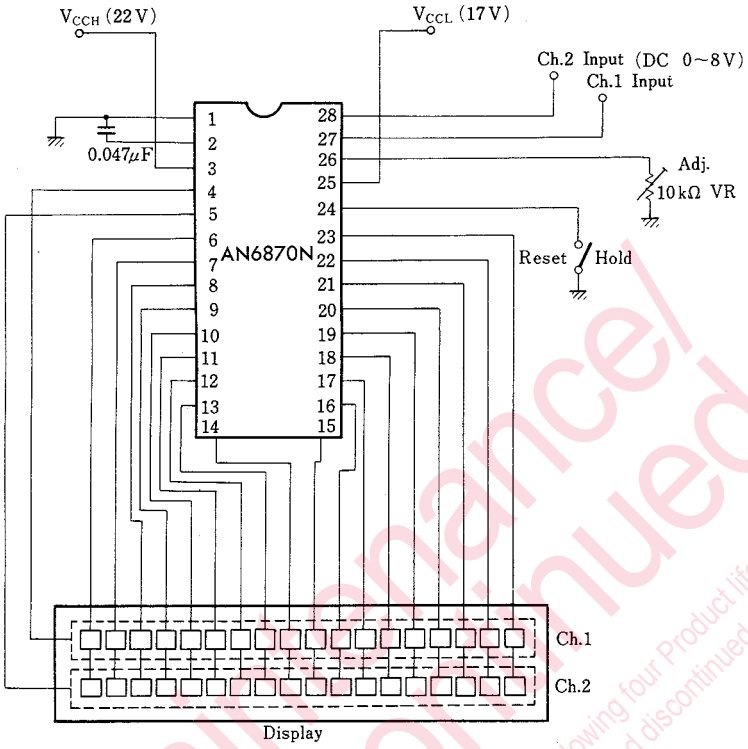


Supply voltage should be used within slant lines as shown in the figure below.



Note) When V_{CCH} and V_{CCL} are low, the highest level may sometimes not light.

■ Application Circuit



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