Semiconductor Corporation

CS8123/4

OPTIMODEM™

Features

- Time Compression Multiplexing for full-duplex communication over a single optical fiber
- Synchronous operation from 2.4 kbps to 256 kbps
- Asynchronous operation from dc to 38.4 kbps
- 10^{-9} BER up to 1.3 km
- System diagnostic capabilities
- Four optional secondary control channels provide independent end-to-end transmission links
- Independent transmit and receive clocks

General Description

The CS8123 and CS8124 from Crystal Semiconductor Corporation are SMART *Analog*™ full-duplex modem devices that receive and transmit serial binary data over a single fiber-optic cable. Both devices provide the filtering, encoding, decoding, and data buffering to implement a "ping-pong" communication channel

The CS8123 device supports asynchronous communication. The CS8124 device supports asynchronous and synchronous communicatons. The $\overline{RTS}$, $\overline{CTS}$, $\overline{DTR}$, and $\overline{DSR}$ control lines can be used for RS232C compatible modem control, or end-to-end transmission channels.

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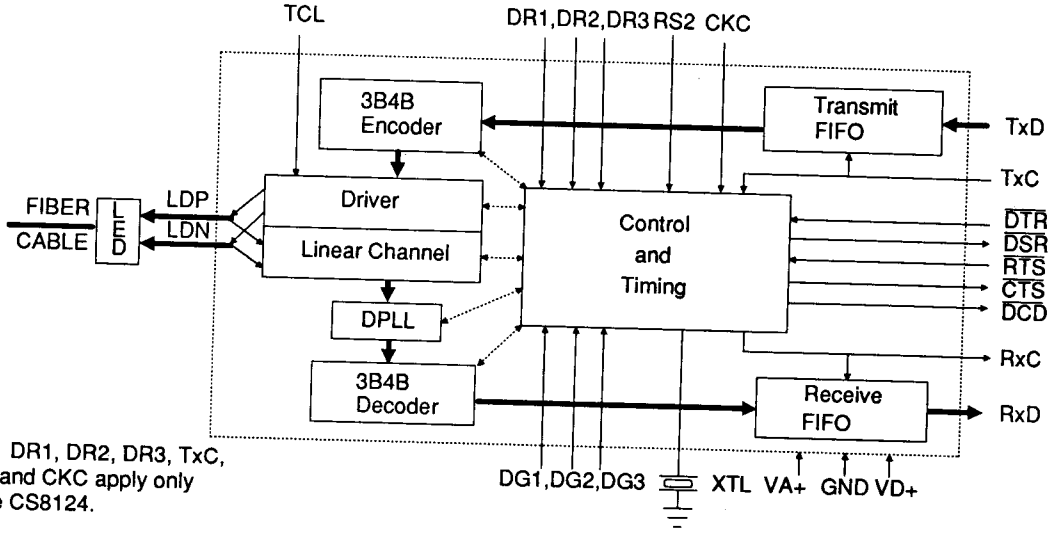
Ordering Information: See Page 8-22



Note: DR1, DR2, DR3, TxC, RxC, and CKC apply only to the CS8124.

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Preliminary Product Information | This document contains information for a new product. Crystal Semiconductor reserves the right to modify this product without notice.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
DC Supply (VA+, VD+ pins)	V+ - GND	- 0.3	6.0	V
Input Voltage	V_{in}	GND - 0.3	V+ + 0.3	V
Input Current (Note 1) (Any pin except LDP, LDN, VA+, VD+, and GND)	I_{in}	-	10	mA
Ambient Operating Temperature	T_A	- 40	85	°C
Storage Temperature	T_{stg}	- 65	150	°C
Average Power Dissipation	P_D	-	500	mW

WARNING: Operating this device at or beyond these limits may result in permanent damage to the device. Normal operation of the part is not guaranteed at or beyond these extremes.

Note: 1. Transient currents of up to 100 mA will not cause SCR latch-up.

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Min	Typ	Max	Units
DC Supply		V+	4.75	5.0	5.25	V
Ambient Operating Temperature		T_A	-40	25	85	°C
LED Drive Current	TCL Floating	I_{LDC}	90	100	115	mA
	TCL Grounded	I_{LDC}	-	10	-	mA

DIGITAL CHARACTERISTICS (T_A = -40 °C to 85 °C; VD+, VA+ = 5V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
High-Level Input Voltage	(Note 2)	V_{IH}	2.0	-	-	V
Low-Level Input Voltage	(Note 2)	V_{IL}	-	-	0.8	V
High-Level Input Voltage	XTL Pin 6	V_{IH}	.9VD+	-	-	V
Low-Level Input Voltage	XTL Pin 6	V_{IL}	-	-	.2VD+	V
High-Level Output Voltage I_{OUT} = -40 uA	(Notes 3,4)	V_{OH}	2.4	-	-	V
Low-Level Output Voltage I_{OUT} = 1.6 mA	(Notes 3,4)	V_{OL}	-	-	0.4	V
Input Leakage Current		I_{in}	-	± 10.0	-	uA
Three-State Leakage Currents		I_{oz}	-	-	± 10	uA

Notes: 2. Input pins are: DR 1/2/3, DG 1/2/3, RS2, CKC, $\overline{DTR}$, $\overline{RTS}$, TxD, TxC.
3. Output pins are: $\overline{DSR}$, $\overline{CTS}$, $\overline{DCD}$, RxD, RxC, TxC.
4. Output drivers will output CMOS logic levels into a CMOS load.

OPERATING CHARACTERISTICS (T_A = -40 °C to 85 °C; VD+ , VA+ = 5V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
Power Consumption, TCL Floating (Notes 5, 6)	Ping Pong	P_C	-	210	300	mW
	Continuous Transmission	P_C	-	375	475	mW
Power Consumption, TCL tied to ground, Ping Pong (Notes 5, 6)		P_C	-	135	-	mW
Power Consumption, Continuous Receive	(Note 6)	P_C	-	125	-	mW
Receiver Input Current Range (Notes 6, 7)	-IP5	I_{IN}	1	-	30	µA
	-IP	I_{IN}	30	-	30,000	nA
LED Capacitance Presented to LDP/LDN		C_T	-	55	80	pF

Notes: 5. Total power dissipated by IC and LED, LED as specified in Table A3.
6. Crystal Frequency = 9.216 MHz.
7. For a 10^{-9} BER.

SWITCHING CHARACTERISTICS (T_A = -40 °C to 85 °C; VD+, VA+ = 5V ± 5%; GND = 0V)

Parameter		Symbol	Min	Typ	Max	Units
Crystal Frequency		f_C	-	9.216	-	MHz
TxC & RxC Frequency:	Synchronous	f_{ckc}	2.4	-	256	kHz
	Continuous Transmit or Receive	f_{ckc}	-	$f_C/8$	-	kHz
RxD & TxD Data Rate:	Synchronous		2.4	-	256	kHz
(Note 8)	Asynchronous		dc	-	38.4	kHz
RxC & TxC Duty Cycle	(Notes 9, 10)		-	50	-	%
Rise Time, All Digital Outputs	(Note 11)	t_r	-	-	100	ns
Fall Time, All Digital Outputs	(Note 11)	t_f	-	-	100	ns
TxD to TxC Rising Setup Time	(Note 10)	t_{su1}	200	-	-	ns
TxC Falling to TxD Hold Time	(Note 10)	t_{h1}	25	-	-	ns
RxD to RxC Rising Setup Time	(Note 10)	t_{su2}	-	$\frac{1}{2\ f_{ckc}}$ -100	-	ns
RxC Rising to RxD Hold Time	(Note 10)	t_{h2}	-	$\frac{1}{2\ f_{ckc}}$ +100	-	ns
Frequency Deviation at TxC Input from Selected Rate	(Note 10, 12)		-	300	-	ppm
Ext. Clock Oscillator	(Notes 9, 13)		-	50	-	%

Notes: 8. CS8124-IP5 units support synchronous communication at 2.4 kbps only in the -40 to +70°C temperature range. CS8124-IP units, when available, will support 2.4 kbps synchronous communication over the -40 to +85°C range.
9. Duty cycle is $(t_{pwh}/(t_{pwh} + t_{pwl})) * 100\%$. See Figure 2.
10. CS8124 in synchronous operation (not all DR1/2/3 low).
11. At maximum load of 1.6 mA and 50 pF.
12. In Synchronous mode, data rate selected by DR1/2/3. In Transmit Only mode, selected rate is fc/8. Crystal frequency must be within ± 50 ppm of specified frequency.
13. For overdriving XTL pin with external clock source.

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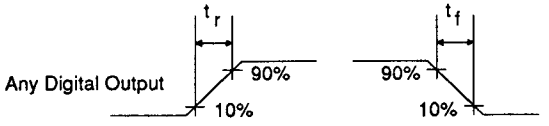

Figure 1. Digital Output Rise and Fall Characteristics

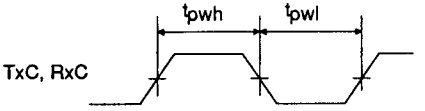

Figure 2. Clock Signal Timing

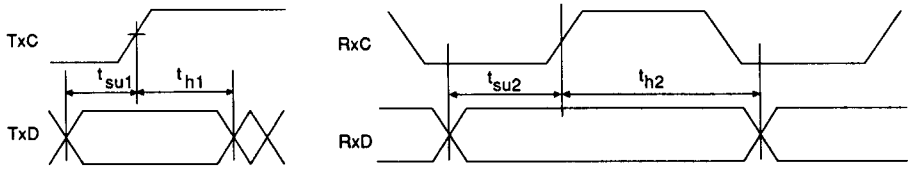

Figure 3. Switching Characteristics

CIRCUIT DESCRIPTION

The CS8123/4 OPTIMODEMs receive and transmit serial binary data over a single fiber-optic cable. Refer to Figure 4 for a typical system connection diagram. The modems provide the filtering, encoding, decoding and data buffering to implement a Time Compression Multiplexed "ping-pong" channel. Both modems support full-duplex asynchronous operation up to 38.4 kbps. The CS8124 also supports full-duplex synchronous communication at 2.4, 9.6, 19.2, 64, 160, 192 and 256 kbps.

The $\overline{RTS}$, $\overline{CTS}$, $\overline{DSR}$ and $\overline{DTR}$ pins can be selectively used in one of two modes: as end-to-end communication channels, or as conventional modem control lines used in handshakes with the OPTIMODEMs (DCE). The two modes are shown in Table 1 and Figure 5

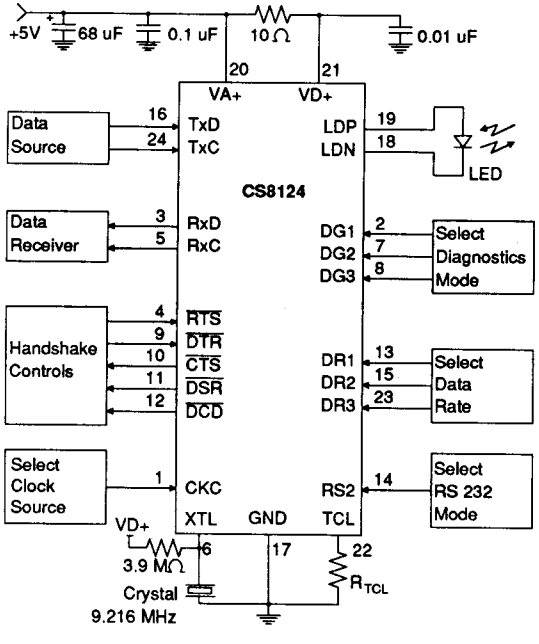

Figure 4. Typical System Connection Diagram

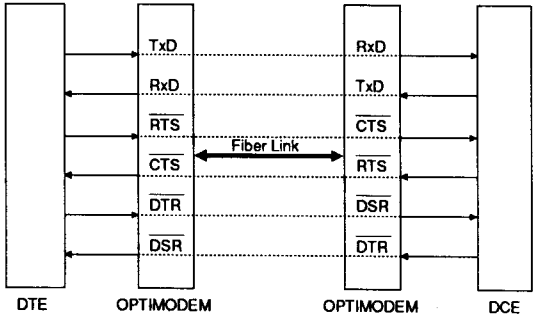

Figure 5. - End-to-End (Transparent) Mode

respectively. The desired mode is selected through the RS2 pin.

In the end-to-end mode, the $\overline{RTS}$ and $\overline{DTR}$ inputs are oversampled at approximately 12 kHz, allowing asynchronous communications at speeds up to 4.8 kHz. The actual data rate achieved will depend upon the jitter tolerance of the circuitry connected to the $\overline{DSR}$ and $\overline{CTS}$ outputs. Oversampling a 4.8 kHz signal at 12 kHz implies 40% jitter (4.8/12) on the rising and falling edges of the $\overline{DSR}$/$\overline{CTS}$ outputs.

Both modems provide extensive diagnostic and maintenance capabilities. Note that the OPTIMODEM digital signals are standard logic levels. RS232 level translators/buffers are required for interfacing to DTE or DCE equipment.

Efficient 3B4B line encoding is employed to ensure error-free data transmission regardless of ones density. The 3B4B line code technique generates a four-bit binary code which corresponds to three binary input bits. This DC balanced code provides sufficient ones density to satisfy the requirements of the receiver's phase-lock loop while optimizing transmission bandwidth and reducing noise. At the receive end, the four-bit code is converted back to the original three bits before being output on RxD.

OPTIMODEM (DCE)	DTE
1. Modem powers up, then asserts $\overline{DSR}$.	1. DTE initializes, then asserts $\overline{DTR}$.
2. Recognizes $\overline{DTR}$. Ping-pong synchronization is in progress.	2. Recognizes $\overline{DSR}$ and waits for $\overline{DCD}$.
3. When Synchronization is achieved, asserts $\overline{DCD}$. *	3. Recognizes $\overline{DCD}$, then asserts $\overline{RTS}$.
4. Recognizes $\overline{RTS}$, then asserts $\overline{CTS}$. **	4. Recognizes $\overline{CTS}$, then starts communication with far end. ***

* If synchronization is lost, modem takes $\overline{DCD}$ and $\overline{CTS}$ high.
** If $\overline{RTS}$ goes high, modem takes $\overline{CTS}$ high.
*** DTE takes $\overline{DTR}$ high, then DCE forces $\overline{DCD}$ high.

Table 1. - Modem Control Mode

In order to accomplish ping-pong communication, the near-end and far-end OPTIMODEMs must establish sychronization so that one OPTIMODEM receives while its counterpart transmits. Each OPTIMODEM operates on an internal master clock which is one sixth the oscillator frequency (1.536 MHz for a 9.216 MHz crystal). A machine cycle, which consists of 128 master clock cycles, is divided into four pieces: time to transmit, a delay period, time to receive, and another delay period. The delay times are established during synchronization to adjust positioning of the transmit and receive windows to account for signal propagation time through the length of fiber being used.

The OPTIMODEM attempts to establish synchronization upon power up or reset. In normal operation, both OPTIMODEMs attempt to communicate using a fixed code. The difference in crystal oscillator frequencies at either end will cause the transmit and receive windows of the two OPTIMODEMs to drift with respect to each other. When one OPTIMODEM first recognizes the transmission from its counterpart, it assumes the slave mode and changes its synchronization control word to direct its counterpart to be the master. In the slave mode, the OPTIMODEM will adjust the length of its machine cycle to speed synchronization with the master. Once synchronized, the slave will make small adjustments in machine cycle time to compensate for differences in oscillator frequencies of the two OPTIMODEMs. The OPTIMODEM can tolerate up to 100 ppm difference in oscillator frequencies between the master and slave. See section on Forced-Slave mode for information on quick synchronization.

The CS8123/4 minimizes the number of external components required, using just one LED to both send and receive data on a single fiber. The CS8123/4 can support cables up to 1300 meters as discussed in the section on LED requirements in the *Applications* section which appends this data sheet. Total transmission delay through two OPTIMODEMs and 1.3 km of cable will be, typically, 38 times the data rate bit period, plus 10µs for fiber delay. For example, at 256 kbps, the transmission delay is approximately 158µs.

TRANSMIT SECTION

In the asynchronous mode, the TxC clock is not used and the CS8123/4 accepts data asynchronously on the TxD input pin. The TxD input is oversampled by at least 6.7 times. This data is temporarily stored in the Transmit

FIFO, encoded and then transmitted to the far end OPTIMODEM.

In the synchronous mode, the CS8124 accepts data on the TxD input pin using the TxC clock. This data is stored in the Transmit FIFO, encoded then transmitted down the fiber. The Clock Control (CKC) input is used to select either an internally generated TxC clock or an externally provided TxC clock. The 160 kbps synchronous data rate operates only with an externally-provided transmit clock (TxC).

Clocks

The CS8123 operates asynchronously. The CS8124 may be operated in either the synchronous or asynchronous mode by setting the data rate inputs, DR1, DR2, and DR3. The data rates and settings are shown in Table 2. The OPTIMODEM's internal frequency reference is provided by connecting a crystal between the XTL pin and ground. Alternatively, the XTL pin may be overdriven by an external clock. When overdriving the XTL pin with a clock signal, the minimum High-Level Input Voltage is 0.9VD+, and the nominal duty cycle of the clock signal is 50%.

The CS8124 provides three clock options:

1) Asynchronous operation: DR1/2/3 = low. RxC and TxC pins of CS8124 are held in a high impedance state.

2) Synchronous with externally provided transmit clock: Not all DR1/2/3 = low; CKC = low. An externally generated clock must be input to the TxC pin at the rate selected by DR1/2/3.

3) Synchronous with internally provided transmit clock: Not all of DR1/2/3 = low; CKC = high. The CS8124 generates the transmit clock and outputs it at the TxC pin.

In the synchronous mode, the two TxC clocks at either end of the link are allowed to deviate from each other by several hundred ppm. Also, an externally provided TxC clock can deviate from the rate selected on DR/1/2/3 by several hundred ppm. In both cases the OPTIMODEMs will make internal adjustments to compensate for the frequency differences. All combinations

DR1	DR2	DR3	Data Rate (kbps)* with 9.216 MHz crystals
0	0	0	Async : dc to 38.4
0	0	1	2.4
0	1	0	9.6
0	1	1	19.2
1	0	0	64
1	0	1	160**
1	1	0	192
1	1	1	256

* Note that a 56 kbps link can be implemented by using 8.064 MHz crystals and the 64 kbps data rate selection.

** The 160 kbps data rate clock must be externally generated.

Table 2 - Data Rate Selection

IMAGE UNAVAILABLE

DG1	DG2	DG3	Diagnostic Mode
0	0	0	Normal Full-Duplex Operation
0	0	1	Local Loopback
0	1	0	Remote Loopback
0	1	1	Remote Loopback with Forced-Slave Mode
1	0	0	Reset
1	0	1	Continuous Receive
1	1	0	Continuous Transmit
1	1	1	Full-Duplex Operation with Forced-Slave Mode

Table 3. Diagnostic Mode Selection

CS8123/4 in Forced-Slave mode, DG 1, 2, 3 = 1/1/1, for at least 50 ms at power-up should ensure rapid and reliable synchronization as long as the two ends of the link are powered up at different times. See the applications section for schematics.

Loopbacks

Two loopback modes are provided on the CS8123/4: local and remote loopbacks. Loopbacks are supported in both asynchronous or synchronous modes, with either internal or external TxC clock. In local loopback mode, the transmit data and clock (if applicable) inputs are looped back inside the near-end CS8123/4 and output on the receive data and clock outputs. This allows the near-end user to verify performance up to the OPTIMODEM. Ping-pong synchronization between the OPTIMODEMs is maintained. Data is still transmitted to the far-end OPTIMODEM. Inputs to the near-end receiver are not output at RxD, and $\overline{DCD}$ is high. Local loopback takes precedence over remote loopback. The local loopback path is the shortest logical path through the OPTIMODEM, and does not include the driver or linear channel.

When remote loopback is selected on the near-end CS8123/4, the near-end OPTIMODEM directs the far-end OPTIMODEM to loop back its received data. This allows the user to verify performance of the complete near-end CS8123/4, the fiber, the LEDs and most of the far-end CS8123/4. The far-end OPTIMODEM also outputs received data and clock (when applicable) at RxD and RxC. When remote loopback is selected and synchronization is achieved, $\overline{DCD}$ goes low on the near-end OPTIMODEM. When remote loopback is in effect, the far-end OPTIMODEM ignores inputs on TxC and TxD and brings $\overline{DCD}$ high.

Continuous Transmit and Receive Modes

The CS8123/4 has two special operating modes: continuous transmit and continuous receive. In continuous transmit mode, the near-end CS8123/4 sends the encoded version of the data input on TxD. TxD must be clocked into the part at a rate of approximately one-eighth the crystal frequency. The 3B4B coding is still employed so the actual transmission rate is one-sixth the crystal frequency. As in normal synchronous operation, TxC can be either an input or an output. If TxC is externally

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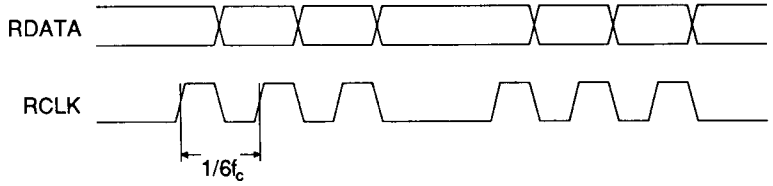


Figure 7. Receiver Output Timing in Continuous Receive Mode

RS2 Input	$\overline{\text{DSR}}$ Output	$\overline{\text{CTS}}$ Output
HIGH	LOW except during reset	Same as $\overline{\text{DCD}}$
LOW	Undefined	Undefined

Table 4. Pin Definitions in Continuous Modes

generated, its frequency can differ from the nominal frequency by several hundred ppm.

When continuous transmit is selected, the receiver is inoperative, no ping-pongs take place and $\overline{\text{DCD}}$ stays high. Measurements can then be made at the output of the near-end LED and at the far-end output of the fiber cable to isolate LED and/or cable failures.

When in the continuous transmission mode, and under control of the $\overline{\text{RTS}}$ pin, the OPTIMODEM will generate a repetitive encoded pattern to achieve 3B4B code alignment of the far-end receiver to the transmitter. The far-end receiver takes no special action in response to this pattern, other than normal 3B4B decoding and receiver synchronization. The user must maintain $\overline{\text{RTS}}$ high for 50ms. When the user returns $\overline{\text{RTS}}$ low, the first data bits input to TxD may be lost (up to 5 bits).

In continuous receive mode, the receiver continually receives data, and outputs the data and clock on the receive outputs, RxD and RxC. The RxC output will be gapped in the following manner: three clock pulses will be followed by one clock hole in a repetitive manner (see Figure 7). $\overline{\text{DCD}}$ is held low in the continuous receive mode once synchronization is achieved. The transmitter is inactive in this mode.

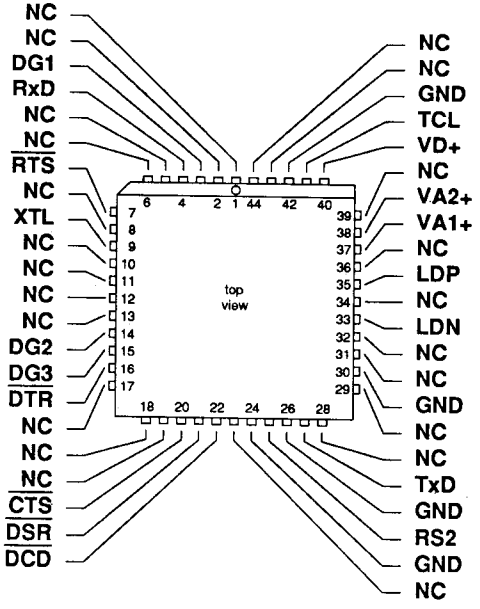
When in the continuous transmit or receive mode, the $\overline{\text{DTR}}$ input is ignored, and the $\overline{\text{DSR}}$ and $\overline{\text{CTS}}$ outputs are defined as in Table 4.

For single direction transmission of asynchronous data, select internally generated TxC. Data input on TxD will be sampled at the TxC rate (fc/8) and transmitted to the receive end. The received data will be present at RxD and RxC may be ignored.

PIN DESCRIPTIONS

CS8123

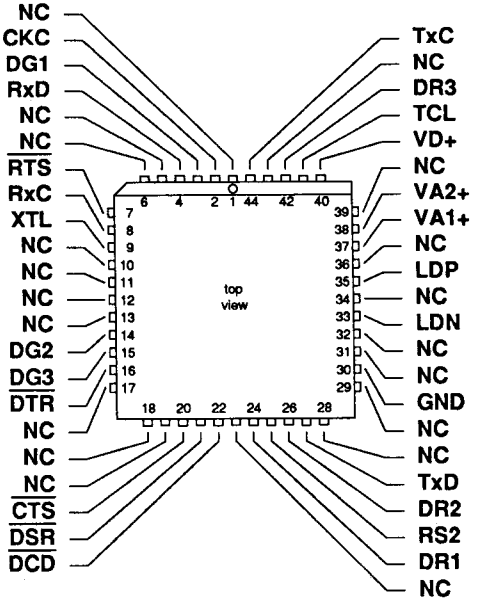
NO CONNECT	NC	1	24	NC	NO CONNECT
DIAGNOSTIC 1	DG1	2	23	GND	GROUND
RECEIVE DATA	RxD	3	22	TCL	TRANSMIT CURRENT LEVEL
REQUEST TO SEND	$\overline{RTS}$	4	21	VD+	DIGITAL POWER SUPPLY
NO CONNECT	NC	5	20	VA+	ANALOG POWER SUPPLY
CRYSTAL OSCILLATOR	XTL	6	19	LDP	LED POSITVE I/O
DIAGNOSTIC2	DG2	7	18	LDN	LED NEGATIVE I/O
DIAGNOSTIC 3	DG3	8	17	GND	GROUND
DATA TERMINAL READY	$\overline{DTR}$	9	16	TxD	TRANSMIT DATA
CLEAR TO SEND	$\overline{CTS}$	10	15	GND	GROUND
DATA SET READY	$\overline{DSR}$	11	14	RS2	RS-232 MODE
DIGITAL CARRIER DETECT	$\overline{DCD}$	12	13	GND	GROUND



Important Note: The initial DIP package will be 600-mil wide. Crystal will introduce a 300-mil DIP package in the future, at which time the 600-mil package will be discontinued. All through-hole board designs for the 600-mil package should have a dual footprint so that the 300-mil package can be dropped in at a later time.

CS8124

CLOCK CONTROL	CKC	1	24	TxC	TRANSMIT CLOCK
DIAGNOSTIC 1	DG1	2	23	DR3	DATA RATE SELECT 3
RECEIVE DATA	RxD	3	22	TCL	TRANSMIT CURRENT LEVEL
REQUEST TO SEND	$\overline{RTS}$	4	21	VD+	DIGITAL POWER SUPPLY
RECEIVE CLOCK	RxC	5	20	VA+	ANALOG POWER SUPPLY
CRYSTAL OSCILLATOR	XTL	6	19	LDP	LED POSITIVE I/O
DIAGNOSTIC 2	DG2	7	18	LDN	LED NEGATIVE I/O
DIAGNOSTIC 3	DG3	8	17	GND	GROUND
DATA TERMINAL READY	$\overline{DTR}$	9	16	TxD	TRANSMIT DATA
CLEAR TO SEND	$\overline{CTS}$	10	15	DR2	DATA RATE SELECT
DATA SET READY	$\overline{DSR}$	11	14	RS2	RS-232 MODE
DIGITAL CARRIER DETECT	$\overline{DCD}$	12	13	DR1	DATA RATE SELECT 1



Important Note: The initial DIP package will be 600-mil wide. Crystal will introduce a 300-mil DIP package in the future, at which time the 600-mil package will be discontinued. All through-hole board designs for the 600-mil package should have a dual footprint so that the 300-mil package can be dropped in at a later time.

Pin numbers apply to 24 pin DIP packages

Power Supplies

VA+ - Analog Power Supply, PIN 20.
Typically +5 volts.

VD+ - Digital Power Supply, PIN 21.
Typically +5 volts.

GND - Ground, PIN 17 on CS8124; PINS 13, 15, 17, and 23 on CS8123.
Ground reference.

Oscillator

XTL - Crystal Oscillator, PIN 6.
Crystal or external CMOS clock input. Standard operation requires a 9.216 MHz (± 50 ppm) crystal or clock. Other frequencies may be used to adjust the OPTIMODEM throughput and data rates. The crystal, if used, should have one pin connected to XTL with minimal length trace on the printed circuit board; the other pin of the crystal should be tied to ground. A 3.9 MΩ pull-up resistor is required between the XTL pin and V+. Crystal specifications are given in the Applications Section. This pin may also be driven at CMOS logic levels.

Inputs

TxD - Transmit Data, PIN 16.
Data to be transmitted. In the asynchronous mode, the rate of the data can be from dc to 38.4 kbps. In the synchronous mode, data is clocked into the CS8124 on the rising edge of TxC.

TxC - Transmit Clock (CS8124 Only), PIN 24.
When CKC is high, TxC will output a clock at the rate selected by DR1/DR2/DR3. When CKC is low, TxC accepts input clock from an external source. TxC goes into a high impedance state when asynchronous operation is selected. For synchronous operation TxD is sampled on the rising edge of TxC. For synchronous operation at 160kbps, an externally-provided clock must be used.

CKC - Clock Control (CS8124 Only), PIN 1.
Defines the source of the clock signal on TxC for synchronous operation. A low on CKC indicates that external clock is being input on TxC. A high on CKC indicates the the CS8124 is sending out TxC at one of the rates selected on the DR1/DR2/DR3 data rate selection inputs. If CKC is left unconnected (floating), CKC pulls low, selecting the external clock. CKC must be held low for synchronous operation at 160kbps since this case requires an externally-provided clock.

DG1; DG2; DG3 - Diagnostic 1; 2; 3, PINS 2, 7, 8.

Select a diagnostic mode as shown in Table 3 in the *Circuit Description* section. If these pins are left unconnected, (floating), the OPTIMODEM assumes the mode for Normal Operation.

DR1; DR2; DR3 - Data Rate 1; 2; 3 (CS8124 Only), PINS 13, 15, 23.

Select a data rate for the TxC and RxC pins as shown in Table 2 in the *Circuit Description* section. If these pins are left unconnected (floating), the CS8124 defaults to asynchronous operation.

RS2 - RS-232C Control Mode Select, PIN 14.

Selects whether the $\overline{\text{CTS}}$, $\overline{\text{RTS}}$, $\overline{\text{DSR}}$ and $\overline{\text{DTR}}$ are used in an end-to-end mode, or modem control handshake mode. When RS2 is low, the end-to-end mode is in effect as shown in Figure 4 in the *Circuit Description* section. If RS2 is left unconnected, (floating), the end-to-end mode is in effect. When RS2 is high, the modem control mode, as shown in Table 1 in the *Circuit Description* section, is in effect.

$\overline{\text{DTR}}$ - Data Terminal Ready , PIN 9.

In the end-to-end mode, data input on $\overline{\text{DTR}}$ is transmitted over the link and presented at the far end as the $\overline{\text{DSR}}$ output. The $\overline{\text{DTR}}$ input is oversampled at approximately 12 kHz, allowing asynchronous communications at speeds up to 4.8 kHz. The actual data rate achieved will depend upon the jitter tolerance of the circuitry connected to the $\overline{\text{DSR}}$ output. Oversampling the 4.8 kHz signal at 12 kHz implies 40% jitter (4.8/12) on the rising and falling edges of the $\overline{\text{DSR}}$ output.

In the modem control mode, a logic 0 indicates that the DTE is powered up and initialized. $\overline{\text{DTR}}$ has an internal pull down.

$\overline{\text{RTS}}$ - Request To Send , PIN 4.

In the end-to-end mode, the $\overline{\text{RTS}}$ input is transmitted over the link and presented at the far end as the $\overline{\text{CTS}}$ output. The $\overline{\text{RTS}}$ input is oversampled at approximately 12 kHz, allowing asynchronous communications at speeds up to 4.8 kHz. The actual data rate achieved will depend upon the jitter tolerance of the circuitry connected to the $\overline{\text{CTS}}$ output. Oversampling the 4.8 kHz signal at 12 kHz implies 40% jitter (4.8/12) on the rising and falling edges of the $\overline{\text{CTS}}$ output.

In the modem control mode, a logic 0 indicates that the DTE is ready to communicate to the far end. In continuous transmit mode, setting $\overline{\text{RTS}}$ to logic 1 causes a repetitive synchronization pattern to be transmitted. $\overline{\text{RTS}}$ has an internal pull down.

TCL - Transmit Current Level, PIN 22.

Defines the current driven into LDP/LDN. When left unconnected, the current level is typically 100mA. When tied to ground, output current level is at a minimum of about 10 mA. Current can be set at an intermediate level, (as shown in Figure 5 in the *Circuit Description* section), by tying this pin to ground through a resistor.

Outputs

$\overline{DCD}$ - Digital Carrier Detect, PIN 12.

A low level indicates that the receiver's 3B4B decoder has achieved synchronization with respect to the incoming data stream. $\overline{DCD}$ is always forced high on the OPTIMODEM for which local loopback has been selected, and during a remote loopback selected by the far-end terminal, and when continuous transmit has been selected. Upon loss of digital carrier, the OPTIMODEM initiates a reset.

$\overline{CTS}$ - Clear To Send, PIN 10.

In the end-to-end mode, CTS shows the state of the far-end $\overline{RTS}$ input. Each $\overline{CTS}/\overline{RTS}$ pair can be used as a uni-directional data channel. The channel is always asynchronous for both the CS8123 and the CS8124, and is oversampled at a rate of approximately 12 kHz.

In the modem control mode (RS2 = high), a logic 0 indicates that the DTE can begin transmission via the TxD and RxD pins.

$\overline{DSR}$ - Data Set Ready, PIN 11.

In the end-to-end mode, $\overline{DSR}$ outputs the data input on the far end $\overline{DTR}$ pin. Each $\overline{DSR}/\overline{DTR}$ pair can be used as a uni-directional data channel. The channel is always asynchronous for both the CS8123 and the CS8124, and is oversampled at a rate of approximately 12 kHz.

In the modem control mode (RS2 = high), a logic 0 indicates that the OPTIMODEM is powered up.

RxD - Received Data, PIN 3.

The data can be read asynchronously (in that mode) or is valid on the rising edge of RxC (in the synchronous mode).

RxC - Received Clock (CS8124 only), PIN 5.

In the synchronous mode, RxD is valid and stable on the rising edge of RxC. RxC goes into a high impedance state when asynchronous operation is selected.

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Inputs/Outputs

LDP; LDN - LED Positive I/O; LED Negative I/O, PIN 19 & 18 .

These bidirectional pins connect directly to the LED, and alternately drive and receive from the LED. LDP connects to the LED anode and LDN connects to the LED cathode. It is absolutely critical that LED be connected to LDP and LDN with the shortest possible traces on the printed circuit board.

APPLICATION NOTES

The use of a CDB8124 or CDB8123 Evaluation Kit to evaluate an OPTIMODEM is highly recommended because system performance is dependent upon the quality of the board layout. In particular, the use of wire-wrapped boards for IC evaluation can result in a non-functional link.

Temperature Effects

LED emission spectrum shifts with temperature, as does the responsivity peak. When LEDs at the opposite ends of link are at different temperatures, the link budget may be decreased. See Table A4.

Fiber Optic Cable

Some specifications for the various cable types are given in Table A1. Table A2 provides some information on cables and manufacturers. There are many variations: contact the manufacturers for more details.

Crystal has used Hewlett-Packard's plastic fibers and associated LEDs (the VERSATILE HFBR-152x family), and observed that the link functioned. These LED's are approximately one-third the cost of the glass-fiber compatible LED's. However, the length of the cable is severely limited by the attenuation characteristics of plastic fiber (about 1dB per meter). The VERSATILE family may prove workable for links of a few meters.

LED Requirements

Typical LED specifications are given in Table A4, and some suggested LEDs are listed in Table A3. It is recommended that the emitted wavelengths of the LED's on each end of a link be the same. The Hafo, HP and Honeywell LED's have different peak wavelengths and power requirements, and should not be interchanged in a system.

Type	Numerical Aperture	Attenuation (dB per km)
200 um PCS	0.40	6.0
100/140um	0.29	4.5
62.5/125 um	0.28	3.75
50/125 um	0.20	3.5
1000 um Plastic	0.50	1000

Table A1 - Typical Cable Specifications

Vendor	Part Number	Package
Crystal Semi	CS8127	ST Fiber DIP
Honeywell	HFE4214-013	ST Fiber DIP
	HFE4404-013	SMA Fiber DIP
Hewlett Packard	HFBR1405	SMA Fiber DIP
	HFBR1415	ST Fiber DIP
ABB Hafo	1A-212	TO-46

Table A3 - Approved LED Vendors

Cable	Manufacturer	Part Number	Phone
200um	Ensign-Bickford Optics Co	HCP-M02000T-A01VS	(203) 678-0371
62.5/125 Ceramic ST	Amphenol Fiber Optics	907-11035-10xxx	(800) 752-5797
100/140 Ceramic ST		907-11036-10xxx	

Table A2 - Fiber Cable and Manufacturer Information

TYPICAL LED SPECIFICATIONS (T_A = 25°C; VA+ = 5V±5%; GND = 0V)

Parameter		Symbol	Typ	Units
Forward Voltage	(I_F = 100 mA)	V_F	1.7	V
Breakdown Voltage	(I_R = 10 µA)	V_{BR}	8.0	V
Series Resistance	(dc)	r_s	8	Ohms
Diode Capacitance (Note A1)	(V_R = 0 V) (f = 1 MHz)	C_T	55	pF
Fiber Coupled Power	(I_F = 100 mA, 100 µm Graded, NA = 0.29)	P_{OC}	116	µW
P_{OC} Temperature Coefficient (Note A2)	(I_F = 100 mA, 100 µm Graded, NA = 0.29)	$\Delta P_{OC}/\Delta T$	-0.025	dB/°C
Response Time	(10 - 90%, I_F = 100 mA No Pre-Bias)	t_r t_f	7 4	ns ns
Responsitivity	(V_R = 0 V)	R_O	0.10	A/W
R_O, Temperature Coeff. (Notes A2, A3)	("+" for detector temp increasing)	$\Delta R_O/\Delta T$	+1.86	mA/W°C
R_O, Wavelength Coeff.	("-" for emitter wavelength increasing	$\Delta R_O/\Delta\lambda$	-3.7	%/nm
Leakage Current	(V_R = 1 V)	I_D	1.0	nA

Notes: A1. For low capacitance diodes, an additional capacitor must be added to meet this specification.
A2. Industrial Temperature Range (-40°C to 85°C).
A3. Includes Spectral Variance.

Table A4 - LED Specifications

Power Supply Decoupling

VA+, VD+ and GND should be decoupled using the circuit shown in Figure A1. The 68 µF capacitor is required to filter the power supply, and prevent power supply ripple. Ripple can occur at the power supply pins of the device as a result of the different current demands when the OPTIMODEM is transmitting or receiving.

Other circuitry on the same board as the OPTIMODEM should have a separate power supply trace (from the point at which the power supply enters the board). All ICs on the board should be decoupled. OPTIMODEM performance will improve as power supply noise is minimized.

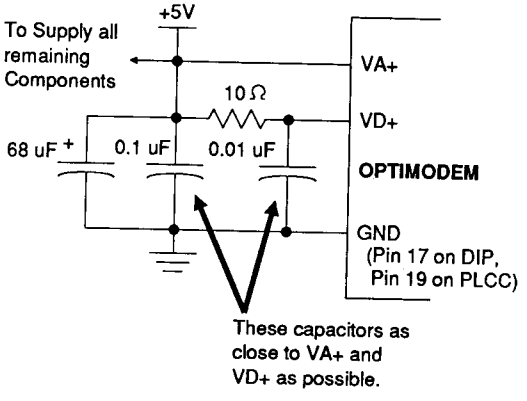

Figure A1 - Power Supply Decoupling

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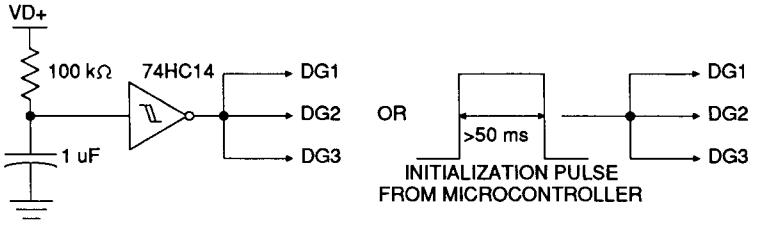

Figure A2. Synchronization Techniques

Fast and Reliable Synchronization

When OPTIMODEMs are operated in normal full-duplex mode, the time requred to synchronize may increase as the frequency difference between the two OPTIMODEM master clocks (XTL) decreases. To ensure fast synchronization, the following circuitry can be used. The circuits shown in Figure A2 momentarily place the OPTIMODEM into Forced-Slave mode on power-up. Holding the OPTIMODEM in Forced-Slave mode for 50 ms will assure synchronization even if the oscillator frequency at either end is exactly the same. As long as the time at which the two ends of a link are powered is different by 50 ms, the first OPTIMODEM powered will be in Normal-Operation mode, while the second is initialized in Forced-Slave mode. Switching from Forced-Slave to Normal-Operation should not effect synchronization once it has been established.

CABLE	200µm Min	100µm Min	62.5µm Min	50µm Min	Units	Notes
1. Transmit power coupled to fiber	640	116	44	20	µW	From LED vendor @I_F = 100 mA See Equation 1 below
2. LED Responsivity	0.05	0.08	0.09	0.10	A/W	From LED vendor
3. LED Output Current	32000	9280	3960	2000	nA	Responsivity x Power
4. Minimum receiver sensitivity	1000	1000	1000	1000	nA	CS8123/4 requirement
5. Budget available for cable and splices	15.1	9.8	6.0	3.0	dB	See Equation 2 below
APPLICATION EXAMPLE						
6. Number of splices	6	4	2	0	splices	System design
7. dB of loss per splice	0.5	0.5	0.5	-	dB	From cable vendor
8. km of cable	1.3	1.3	1.0	0.5	km	System design
9. dB of loss/km cable	6	4.5	3.75	3.5	dB	From cable vendor
10. Total cable/splice loss	10.8	7.8	4.75	1.75	dB	See Equation 3 below
11. Operating Margin	4.3	2.0	1.25	1.25	dB	Power - Losses

Note: LED coupled power must be limited (using TCL pin) so that the signal input to receiver is ≤30 µA

Equation 1: If coupled power is specified in dBm, dBm can be converted to Watts by: $10^{(dBm/10)}$ x .001
Equation 2: 10 x log(I_{in}/LED Output Currrent)
Equation 3: (Number of Splices x dB of loss per splice) + (km of cable x dB of loss per km cable)

Table A5. Worst Case Link Budget Calculation for CS8127 LED Performance at 25°C

Link Budget Calculation

Table A5 gives a link budget assuming *worst case* CS8127 LED performance at 25°C. The link budget calculations are based upon the minimum coupled power and responsivity of a CS8127 LED. Note that the 200 µm cable couples much more power to the LED and is therefore preferable for applications where transmission over significantly long links is required. No matter how much current is input to the OPTIMODEM, timing control structures of the OPTIMODEM limit maximum cable length to 1300 meters.

The link budget calculation is also used to ensure that the OPTIMODEM linear channel is not over-driven (30 µA maximum input allowed). See the CS8127 data sheet for more information on estimating link budgets.

Crystal Oscillator

A 3.9 MΩ pull-up resistor is required between the XTL pin and V+. The crystal should be located as close as possible to the XTL pin. One end of the resistor should also be physically close to the XTL pin. The other end of the resistor (which is tied to V+) should be located away from the OPTIMODEM. The resistor should not be on the back of the PCB directly underneath the IC.

The total capacitance on the XTL input (including capacitance resulting from adjacent traces, power and ground planes, socket, etc.) should be ≤ 4 pF.

The crystal requirements are:

$C_O \leq 5.5$ pF

C_L=14 pF at 9.216 MHz

R_S = 9Ω (typically). In all cases must be < 13Ω. The lower the resistance, the more reliable the oscillator start-up will be. During crystal manufacturing, if a crystal vendor attempts to keep the worst-case R_S < 13Ω, the typical R_S will be < 9Ω.

Crystal Semiconductor offers a crystal which meets these crystal requirements - the CXT9216.

When overdriving the XTL pin with a clock signal, the minimum High-Level Input Voltage is 0.9 VD+, and the nominal clock signal duty cycle should be 50%.

Layout Considerations

It is recommended that a judicious amount of ground plane be used around LDN and LDP, and the LED pins (on both sides of the board in case of two-layer boards); and also around the quartz crystal. Trace length from the LED to the LDN and LDP pins on the OPTIMODEM should be kept to a minimum. The receiver is very sensitive and will be adversely affected by noise. Also, physically isolating the OPTIMODEM from potential noise sources on a circuit board is beneficial.

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Ordering Guide

Model	Package	Minimum Sensitivity
CS8123-IP5	24 Pin 0.6" DIP*	1 µA
CS8123-IP	24 Pin 0.6" DIP*	30 nA
CS8123-IL5	44 Pin PLCC	1 µA
CS8123A-IP	24 Pin 0.3" DIP	30 nA
CS8124-IP5	24 Pin 0.6" DIP*	1 µA
CS8124-IP	24 Pin 0.6" DIP *	30 nA
CS8124-IL5	44 Pin PLCC	1 µA
CS8124A-IP	24 Pin 0.3" DIP	30 nA

* The 24-pin 0.6" package will be discontinued and replaced by the 24-pin 0.3" package. Lay out your PCB for both.