GM3054/GM3057

SERIAL INTERFACE CMOS CODEC/FILTER

Description

The GM3054, GM3057 family consists of μ-law and A-law monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using GoldStar's advanced double Polysilicon Gate CMOS process.

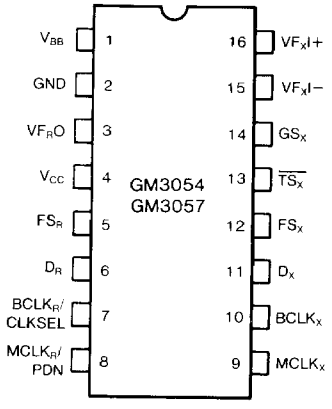
The transmit portion of each device consists of an input gain adjust amplifier, an active RC pre-filter which eliminates very high frequency noise prior to entering a switched-capacitor band-pass filter that rejects signals below 200 Hz and above 3400 Hz. Also included are autozero circuitry and a compressing coder which samples the filtered signal and encodes it in the compressed μ-law or A-law PCM format. The receive portion of each device consists of an expanding decoder, which reconstructs the analog signal from the compressed μ-law or A-law code, a low-pass filter which corrects for the sin x/x response of the decoder output and rejects signals above 3400 Hz and is followed by a single-ended power amplifier capable of driving low impedance loads. The devices require two 1.536 MHz, 1.544 MHz or 2.048 MHz transmit and receive master clocks, which may be asynchronous, transmit and receive bit clocks, which may vary from 64 KHz to 2.048 MHz, and transmit and receive frame sync pulses. The timing of the frame sync pulses and PCM data is compatible with both industry standard formats.

Features

- **Complete Codec and Filtering System Including:**
  - **Transmit High-Pass and Low-Pass Filtering**
  - **Receive Low-Pass Filter With Sin X/X Correction**
  - **Active RC Noise Filter**
  - **μ-Law or A-Law Compatible Coder and Decoder**
  - **Internal Precision Voltage Reference**
  - **Serial I/O Interface**
  - **Internal Auto-Zero Circuitry**
- **μ-Law, 16 Pin—GM3054**
- **A-Law, 16 Pin—GM3057**
- **Meets or Exceeds All D3/D4 and CCITT Specifications**
- **$\pm$5.0V Operation**
- **Low Operating Power—Typically 60 mW**
- **Power-Down Standby Mode—Typically 3.0 mW**
- **Automatic Power-Down**
- **TTL or CMOS Compatible Digital Interfaces**
- **Maximizes Line Interface Card Circuit Density**

Pin Configuration

(Top View)



Block Diagram

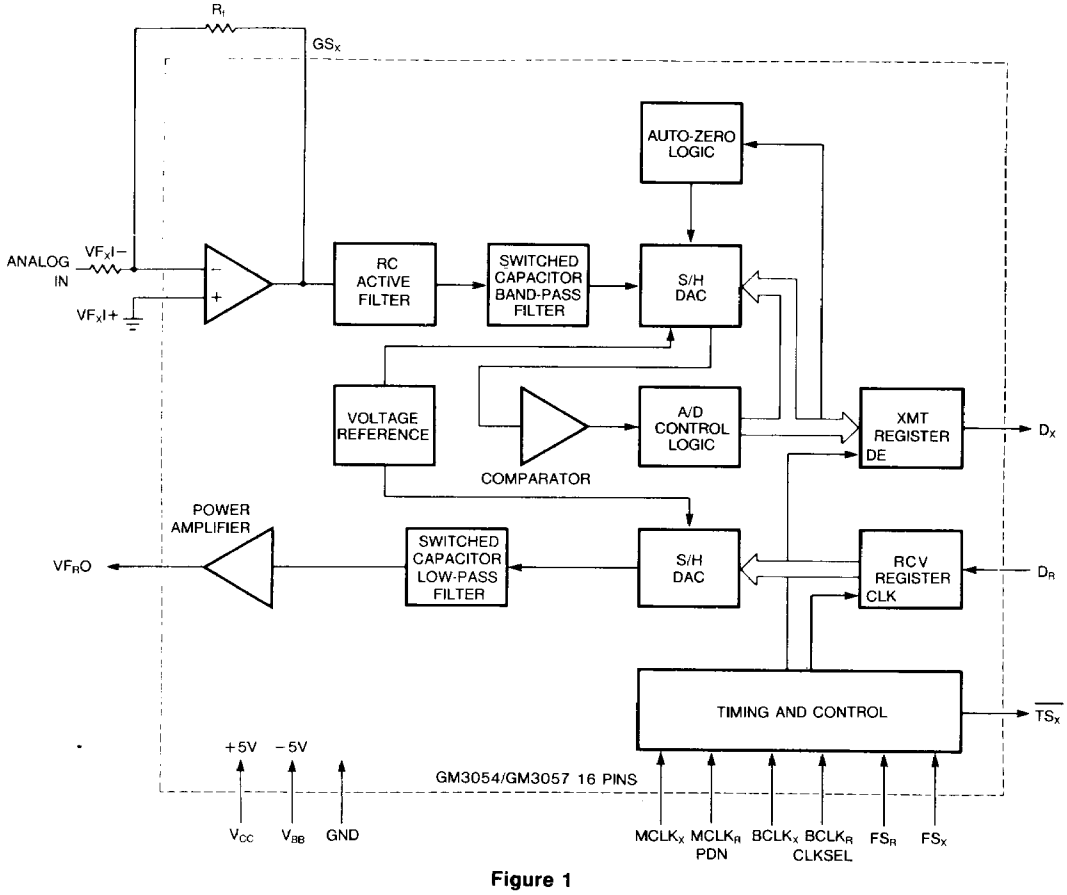


Figure 1

Pin Description

Pin NO.	Name	Function
1	V_{BB}	Negative power supply pin. $V_{BB}=-5V\pm5\%$
2	GND	Ground. All signals are referenced to this pin.
3	VF_RO	Analog output of the receive filter.
4	V_{CC}	Positive power supply pin. $V_{CC}=+5V\pm5\%$.
5	FS_R	Receive frame sync pulse which enables $BCLK_R$ to shift PCM data into D_R. FS_R is an 8 KHz pulse train. See Figures 2 and 3 for timing details.
6	D_R	Receive data input. PCM data is shifted into D_R following the FS_R leading edge.
7	$BCLK_R$/CLKSEL	The bit clock which shifts data into D_R after FS_R leading edge. May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCKL_R$. Alternatively, may be a logic input which selects either 1.536 MHz/1.544 MHz or 2.048 MHz for master clock in synchronous mode and $BCLK_X$ is used for both transmit and receive directions (See Table 1).
8	$MCLK_R$/PDN	Receive master clock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. When $MCLK_R$ is connected continuously low, $MCLK_X$ is selected for internal timing. When $MCLK_R$ is connected continously high, the device is powered down.
9	$MCLK_X$	Transmit master cock. Must be 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with $MCLK_R$.
10	$BLCK_X$	The bit clock which shifts out the PCM data on D_X. May vary from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.
11	D_X	The 3-State PCM data output which is enabled by FS_X.
12	FS_X	Transmit frame sync pulse input which enables $BCLK_X$ to shift out the PCM data on D_X. FS_X is an 8 KHz pulse train; see Figures 2 and 3 for timing details.
13	$\overline{TS_X}$	Open drain output which pulses low during the encoder time slot.
14	GS_X	Analog output of the transmit input amplifier. Used to externally set gain.
15	VF_XI-	Inverting input of the transmit Input amplifier.
16	VF_XI+	Non-inverting input of the transmit input amplifier.

Functional Description

POWER-UP

When power is first applied, power-on reset circuitry initializes the device and places it into the power-down mode. All non-essential circuits are deactivated and the D_X and VF_RO outputs are put in high impedance states. To power-up the device, a logical low level or clock must be applied to the $MCLK_R$/PDN pin and FS_X and/or FS_R pulses must be present. Thus, 2 power-down control modes are available. The first is to pull the $MCLK_R$/PDN pin high; the alternative is to hold both FSX and FSR inputs continuously low—the device will power-down approximately 2ms after the last FS_X or FS_R pulse. Power-up will occur on the first FS_X or FS_R pulse. The 3-State PCM data output, D_X, will remain in the high impedance state until the second FS_X pulse.

SYNCHRONOUS OPERATION

For synchronous operation, the same master clock and bit clock should be used for both the transmit and receive directions. In this mode, a clock must be applied to $MCLK_X$ and the $MCLK_R$/PDN pin can be used as a power-down control. A low level on $MCLK_R$/PDN powers up the device and a high level powers down the device. In either case, $MCLK_X$ will be selected as the master clock for both the transmit and receive circuits. A bit clock must also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be also be applied to $BCLK_X$ and the $BCLK_R$/CLKSEL can be used to select the proper internal divider for a master clock of 1.536 MHz, 1.544 MHz or 2.048 MHz. For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame.

Functional Description (Continued)

With a fixed level on the $BCLK_R$/CLKSEL pin, $BCLK_X$ will be selected as the bit clock for both the transmit and receive directions. Table 1 indicates the frequencies of operation which can be selected, depending on the state of $BCLK_R$ CLKSEL. In this synchronous mode, the bit clock, $BCLK_X$, may be from 64 KHz to 2.048 MHz, but must be synchronous with $MCLK_X$.

Each FS_X pulse begins the encoding cycle and the PCM data from the previous encode cycle is shifted out of the enabled D_X output on the positive edge of $BCLK_X$. After 8 bit clock periods, the 3-State D_X output is returned to a high impedance state. with an FS_R pulse, PCM data is latched via the D_R input on the negative edge of $BCLK_X$ (or $BCLK_R$ if running). FS_X and FS_R must be synchronous with $MCLK_{X/R}$.

Table I. Selection Of Master Clock Frequencies

$BCLK_R$/CLKSEL	Master Clock Frequency Selected	
	GM3057	GM3054
Clocked	2.048 MHz	1.536 MHz or 1.544 MHz
0	1.536 MHz or 1.544 MHz	2.048 MHz
1 (or Open Circuit)	2.048 MHz	1.536 MHz or 1.544 MHz

ASYNCHRONOUS OPERATION

For asynchronous operation, separate transmit and receive clocks may be applied. $MCLK_X$ and $MCLK_R$ must be 2.048 MHz for the GM3057, and 1.536 MHz or 1.544 MHz for the GM3054 and need not be synchronous. For best transmission performance, however, $MCLK_R$ should be synchronous with $MCLK_X$, which is easily achieved by appling only static logic levels to the $MCLK_R$/PDN pin. This will automatically connect $MCLK_X$ to all internal $MCLK_R$ functions (see Pin Description). For 1.544 MHz operation, the device automatically compensates for the 193rd clock pulse each frame. FS_X starts each encoding cycle and must be synchronous with $MCLK_X$ and $BCLK_X$ FSR starts each decoding cycle and must be synchronous with $BCLK_R$ which must be a clock. The logic levels shown in Table 1 are not valid for asynchronous operation. $BCLK_X$ and $BCLK_R$ may operate from 64 KHz to 2.048 MHz.

SHORT FRAME SYNC OPERATION

The device can utilize either a short frame sync pulse or a long frame sync pulse. Upon power initialization, the device assumes a short frame mode. In this mode, both frame sync pulses, FS_X and FS_R, must be one bit clock period long, with timing relationships specified in Figure 2. With FS_X high during a falling edge of $BCLK_X$ the next rising edge of $BCLK_X$ enables the D_X 3-State output buffer, which will output the sign bit. The following seven rising edges clock out the remaining seven bits, and the next falling edge disables the D_X output. With FS_R high during a falling edge of $BCLK_R$ ($BCLK_X$ in synchronous mode), the next falling edge of $BCLK_R$ latches in the sign bit. The following seven falling edges latch in the seven remaining bits. Both devices may utilize the short frame sync pulse in synchronous or asynchronous operating mode.

LONG FRAME SYNC OPERATION

The use the long frame sync mode, both the frame sync pulses, FS_X and FS_R, must be three or more bit clock periods long, with timing relationships specified in Figure 3. Based on the transmit frame sync, FS_X, the device will sense whether short or long frame sync pulses are being used. For 64 KHz operation, the frame sync pulse must be kept low for a minimum of 160 ns. The D_X TRI-STATE output buffer is enabled with the rising edge of FS_X or the rising edge of $BCLK_X$, whichever comes later, and the first bit clocked out is the sign bit. The following seven $BCLK_X$ rising edges clock out the remaining seven bits. The D_X output is disabled by the falling $BCLK_X$ edge following the eighth rising edge, or by FS_X going low, whichever comes later. A rising edge on the receive frame sync pulse, FS_R, will cause the PCM data at D_R to be latched in on the next eight falling edge of $BCLK_R$ ($BCLK_X$ in sychronous mode). Both devices may utilize the long frame sync pulse in synchronous or asynchronous mode.

TRANSMIT SECTION

The transmit section input is an operational amplifier with provision for gain adjustment using two external resistors, see Figure 4. The low noise and wide bandwidth allow gains in excess of 20 dB across the audio passband to be realized. The op amp drives a unity-gain filter consisting of RC active pre-filter, followed by an eighth order switched-capacitor bandpass filter clocked at 256 KHz. The output of this filter directly drives the encoder sample-and-hold circuit. The A/D is of compressing type according to μ-law (GM3054) or A-law (GM3057) coding conventions. A precision voltage reference is trimmed in manufacturing to provide an input overload (t_{MAX}) or nominally 2.5V peak (see table of Transmission Characteristics). The FS_X frame sync pulse controls the sampling of the filter output, and then the successive-approximation encoding cycle begins. The 8-bit code is then loaded into a buffer and shifted out through D_X at the next FS_X pulse. The total encoding delay will be approximately 165 μs (due to the transmit filter) plus 125 μs (due to encoding delay), which total 290 μs. Any

offset voltage due to the filters or comparator is cancelled by sign bit integration.

RECEIVE SECTION

The receive station consists of an expanding DAC which drives a fifth order switched-capacitor low pass filter clocked at 256 KHz. The decoder is A-law (GM3057) or μ-law (GM3054) and the 5th order low pass filter corrects for sin x/x attenuation due to the 8 KHz sample/hold. The filter is then followed by a power amplifier capable of driving a 600Ω load to a level of 7.2 dBm. The receive section is unity-gain. Upon the occurrence of FS_R, the data at the D_R input is clocked in on the falling edge of the next eight $BCLK_R$ ($BCLK_X$) periods. At the end of the decoder time slot, the decoding cycle begins, and 10 μs later the decoder DAC output is updated. The total decoder delay is 10 μs (decoder update) plus 110 μs (filter delay) plus 62.5 μs d(½ frame), which gives approxiamtely 180 μs.

Absolute Maximum Ratings

V_{CC} to GND	7V
V_{SS} to GND	−7V
Voltage at any Analog Input or Output	V_{CC}+0.3V to V_{SS}−0.3V
Voltage at any Digital Input or Output	V_{CC}+0.3V to GND −0.3V
Operating Temperature Range	−25°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics

Unless otherwise noted: V_{CC}=5.0V±5%, V_{BB}=−5V±5%, GND=OV, T_A=0°C to 70°C; typical characteristics specified at V_{CC}=5.0V, V_{BB}=−5.0V, T_A=25°C; all signals are referenced to GND.

Operating Current

$I_{CC}0$	Power-Down Current			0.5	1.5	mA
$I_{BB}0$	Power-Down Current			0.05	0.3	mA
$I_{CC}1$	Active Current			6.0	9.0	mA
$I_{BB}1$	Active Current			6.0	9.0	mA

Digital Interface

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, $I_L=-3.2mA$ $\overline{TS}_X$, $I_L=3.2mA$, Open Drain			0.4 0.4	V V
V_{OH}	Output High Voltage	D_X, $I_H=-3.2mA$	2.4			V
I_{IL}	Input Low Current	$GND \leq V_{IN} \leq V_{IL}$, All Digital Inputs	−10		10	μA
I_{IH}	Inptu High Current	$V_{IH} \leq V_{IN} \leq V_{CC}$	−10		10	μA
I_{OZ}	Output Current in High Impedance State	D_X, $GND \leq V_O \leq V_{CC}$	−10		10	μA

Analog Interface With Transmit Input Amplifier

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_IXA	Input Leakage Current	$-2.5V \leq V \leq +2.5V$, VF_XI^+or VF_XI^-	−200		200	nA
R_IXA	Input Resistance	$-2.5V \leq V \leq +2.5V$, VF_XI^+or VF_XI^-	10			MΩ
R_OXA	Output Resistance	Closed Loop, Unity Gain		1	3	Ω
R_LXA	Load Resistance	GS_X	10			KΩ
C_LXA	Load Capacitance	GS_X			50	pF
V_OXA	Output Dynamic Range	GS_X, $R_L \leq 10K\Omega$	±2.8			V
A_VXA	Voltage Gain	VF_XI^+ to GS_X	5000			V/V
F_UXA	Unity Gain Bandwidth		1	2		MHz
$V_{OS}XA$	Offset Voltage		−20		20	mV
$V_{CM}XA$	Common-Mode Voltage		−2.5		2.5	V
CMRRXA	Common-Mode Rejection Ratio		60			dB
PSRRXA	Power Supply Rejection Ratio		60			dB

Analog Interface With Receive Output

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
R_ORF	Output Resistance	Pin VF_RO		1	3	Ω
R_LRF	Load Resistance	$VF_RO=\pm 2.5V$	600			Ω
C_LRF	Load Capacitance				500	pF
VOS_RO	Output DC Offset Voltage		−200		200	mV

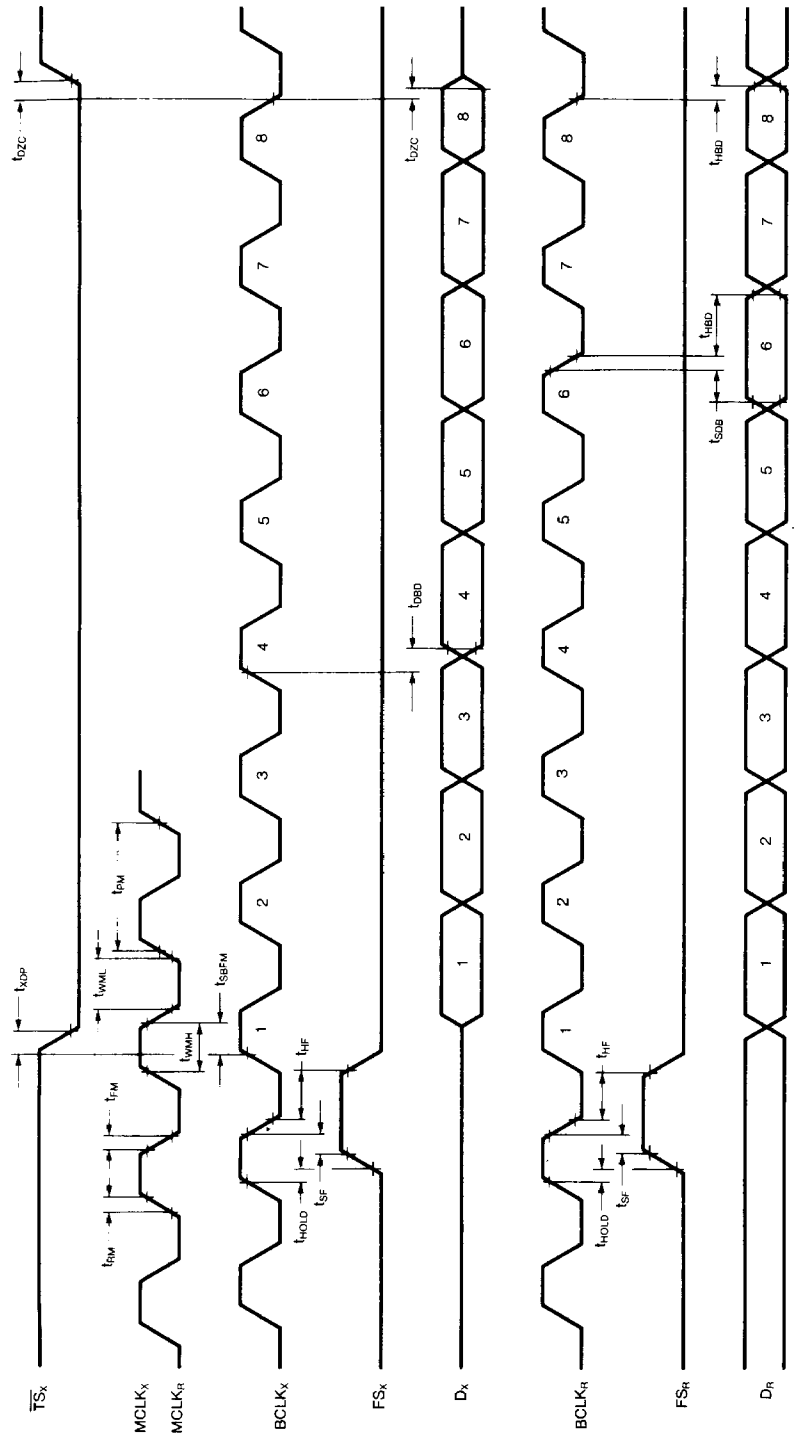
Timing Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$1/t_{PM}$	Frequency of Master Clocks	Depends on the Device Used and the $BCLK_R$/CLKSEL Pin		1.536		MHz
				1.544		MHz
		$MCLK_X$ and $MCLK_R$		2.048		MHz
t_{WMH}	Width of Master Clock High	$MCLK_X$ and $MCLK_R$	160			ns
t_{WML}	Width of Master Clock Low	$MCLK_X$ and $MCLK_R$	160			ns
t_{RM}	Rise Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{FM}	Fall Time of Master Clock	$MCLK_X$ and $MCLK_R$			50	ns
t_{SBFM}	Set-Up Time from $BCLK_X$ High (and FS_X in Long Frame Sync Mode) to $MCLK_X$ Falling Edge	First Bit Clock after the Leading Edge of FS_X	100			ns
t_{PB}	Period of Bit Clock		485	488	15,725	ns
t_{WBH}	Width of Bit Clock High	V_{IH}=2.2V	160			ns
t_{WBL}	Width of Bit Clock Low	V_{IL}=0.6V	160			ns
t_{RB}	Rise Time of Bit Clock	t_{PS}=488 ns			50	ns
t_{FB}	Fall Time of Bit Clock	t_{PB}=488 ns			50	ns
t_{HBF}	Holding Time from Bit Clock Low to Frame Sync	Long Frame Only	0			ns
t_{HOLD}	Holding Time from Bit clock High to Frame Sync	Short Frame Only	0			ns
t_{SFB}	Set-Up Time from Frame Sync to Bit Clock Low	Long Frame Only	80			ns
t_{DBD}	Delay Time from $BCLK_X$ High to Data Valid	Load=150 pF plus 2 LSTTL Loads	0		180	ns
t_{XDP}	Delay Time to TS_X Low	Load=150 pF plus 2 LSTTL Loads			140	ns
t_{DZC}	Delay Time from $BCLK_X$ Low to Data Output Disabled		50		165	ns
t_{DZF}	Delay Time to Valid Data from FS_X or $BCLK_X$, Whichever Comes Later	C_L=0 pF to 150 pF	20		165	ns
t_{SDB}	Set-Up Time from D_R Valid to $BCLK_{R/X}$ Low		50			ns
t_{HBD}	Hold Time from $BCLK_{R/X}$ Low to D_R Invalid		50			ns
t_{SF}	Set-Up time from $FS_{X/R}$ to $BCLK_{X/R}$ Low	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	50			ns
t_{HF}	Hold Time from $BCLK_{X/R}$ Low to $FS_{X/R}$	Short Frame Sync Pulse (1 or 2 Bit Clock Periods Long) (Note 1)	100			ns
t_{HBF1}	Hold Time from 3rd Period of Bit Clock Low to Frame Sync (FS_X or FS_R)	Long Frame Sync Pulse (from 3 to 8 Clock Periods Long)	100			ns
t_{WFL}	Minimum Width of the Frame Sync Pulse (Low Level)	64k Bit/s Operating Mode	160			ns

Note 1: For short frame sync timing, FS_X and FS_R must go high while their respective bit clocks are high.

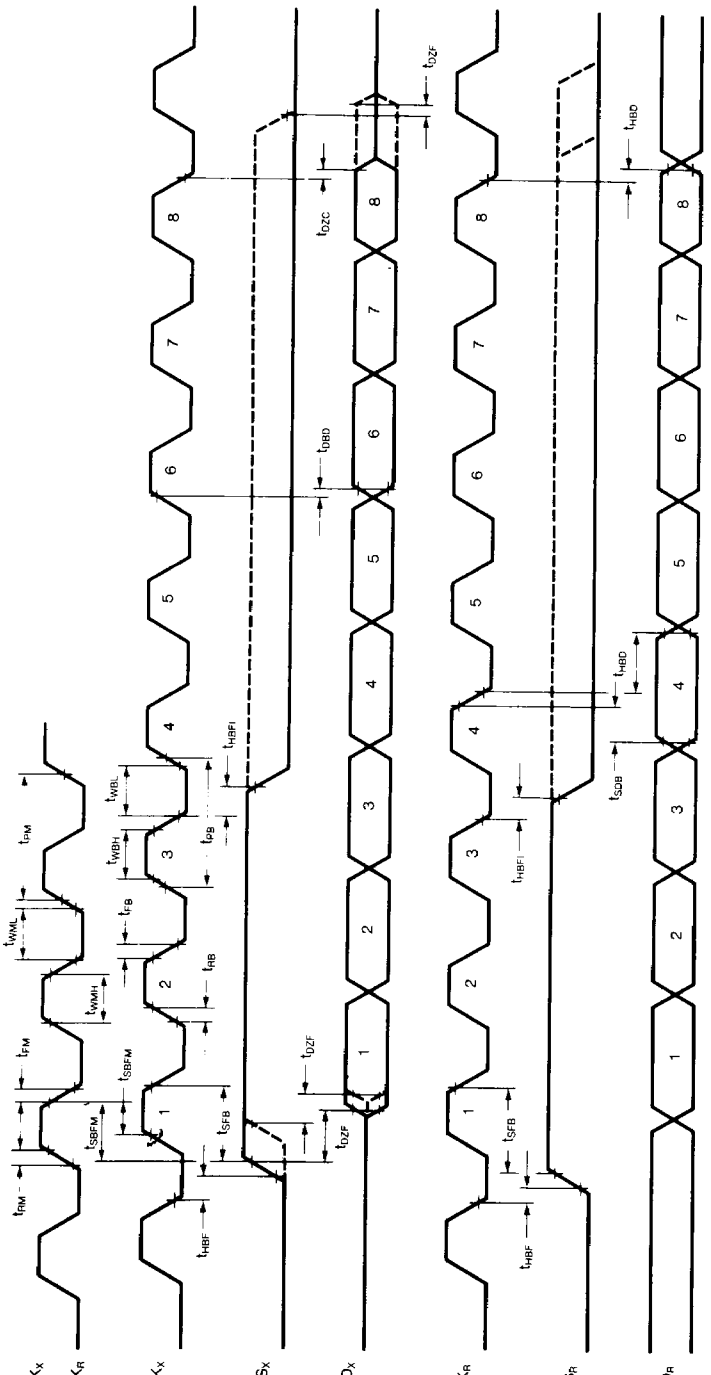
Timing Diagrams

Figure 2. Short Frame Sync Timing



Timing Diagrams (Continued)

Figure 3. Long Frame Sync Timing



Transmission Characteristics

Unless otherwise specified: T_A=0°C to 70°C, v_{CC}=5V±5%, V_{BB}=−5V±5%,GND=0V, f=1.02 KHz, V_{IN}=0 dBm 0, transmit input amplifier connected for unity-gain non-inverting.

Amplitude Response

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
	Absolute Levels	Nominal 0 dBm0 Level is 4dBm (600Ω)				
		0 dBm0				
		GM3054		1.2276		Vrms
		GM3057		1.2276		Vrms
t_{MAX}		Max Overload Level				
		GM3054 (3.17 dBm0)		2.501		V_{PK}
		GM3057 (3.14 dBm0)		2.492		V_{PK}
G_{XA}	Transmit Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input at GS_X=0 dBm0 at 1020 Hz	−0.15		0.15	dB
G_{XR}	Transmit Gain, Relative to G_{XA}	f=16Hz			−40	dB
		f=50 Hz			−30	dB
		f=60 Hz			−26	dB
		f=200 Hz	−1.8		−0.1	dB
		f=300 Hz-3000 Hz	−0.15		0.15	dB
		f=3300 Hz	0.35		0.05	dB
		f=3400 Hz	−0.7		0	dB
		f=4000 Hz			−14	dB
		f=4600 Hz and Up, Measure Response from 0 Hz to 4000 Hz			−32	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	T_A=0°C to 70°C			±0.1	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	V_{CC}=5V±5%, V_{BB}=−5V±5%			±0.05	dB
G_{XRL}	Transmit Gain Variations with Level	Sinusoidal Test method Reference Level=−10 dBm0				
		VF_XI^+=−40 dBm0 to + 3 dBm0	−0.2		0.2	dB
		VF_XI^+=−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		VF_XI^+=−55 dBm0 to −50 dBm0	−1.2		1.2	dB
G_{RA}	Receive Gain, Absolute	T_A=25°C, V_{CC}=5V, V_{BB}=−5V Input=Digital Code Sequence for 0 dBm0 Signal at 1020 Hz	−0.15		0.15	dB
G_{RR}	Receive Gain, Relative to G_{RA}	f=0 Hz to 3000 Hz	−0.15		0.15	dB
		f=3300 Hz	−0.35		0.05	dB
		f=3400 Hz	−0.7		0	dB
		f=4000 Hz			−14	dB
G_{RAT}	Absolute Receive Gain Variation with Termperature	T_A=0°C to 70°C			±0.1	dB
G_{RAV}	Absolute Receive Gain Variation with Supply Voltage	V_{CC}=5V±5%, V_{BB}=−5V±5%			±0.05	dB
G_{RRL}	Receive Gain Variations with Level	Sinusoidal Test Method; Reference Input PCM Code Corresponds to an Ideally Encoded—10 dBm0 Signal				
		PCM Level=−40 dBm0 to +3 dBm0	−0.2		0.2	dB
		PCM Level=−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		PCM Level=−55 dBm0 to −50 dBm0	−1.2		1.2	dB
V_{RO}	Receive Output Drive Level	R_L=600Ω	−2.5		2.5	V

Transmission Characteristics (Continued)
Unless otherwise specified: T_A=0°C to 70°C, V_{CC}=5V±5%, V_{BB}=−5V±5%, GND=0V, f=1.02 KHz, V_{IN}=0 dBm0, transmit input amplifier connected for unity-gain noninverting.

Envelope Delay Distortion With Frequency

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
D_{XA}	Transmit Delay, Absolute	f=1600 Hz		290	315	μS
D_{XR}	Transmit Delay, Relative to D_{XA}	f=500 Hz-600 Hz		195	220	μS
		f=600 Hz-800 Hz		120	145	μS
		f=800 Hz-1000 Hz		50	75	μS
		f=1000 Hz-1600 Hz		20	40	μS
		f=1600 Hz-2600 Hz		55	75	μS
		f=2600 Hz-2800 Hz		80	105	μS
		f=2800 Hzp3000 Hz		130	155	μS
D_{RA}	Receive Delay, Absolute	f=1600 Hz		180	200	μS
D_{RR}	Receive Delay, Relative to D_{RA}	f=500 Hz-1000 Hz	−40	−25		μS
		f=1000 Hz-1600 Hz	−30	−20		μS
		f=1600 Hz-2600 Hz		70	90	μS
		f=2600 Hz-2800 Hz		100	125	μS
		f=2800 Hz-3000 Hz		145	175	μS

Noise

N_{XC}	Transmit Noise, C Message Weighted	GM3054 VF_XI^+=0		12	15	dBmC0
N_{XP}	Transmit Noise, P Message Weighted	GM3057 VF_XI^+=0V		−74	−69 (Note 1)	dBmOp
N_{RC}	Receive Noise, C Message Weighted	GM3054 PCM Code Equals Alternating Positive and Negative Zero		8	11	dBmC0
N_{RP}	Receive Noise, P Message Weighted	GM3057 PCM Code Equals Positive Zero		−82	−79	dBm0p
N_{RS}	Noise, Single Frequency	f=0 KHz to 100 KHz, Loop Around Measurement, VF_XI^+=0 V_{rms}			−53	dBm0
$PPSR_X$	Positive Power Supply Rejection, Transmit	VF_XI^+=0 Vrms V_{CC}=5.0 V_{DC}+100 mVrms f=0 KHz-50 KHz	40			dBC
$NPSR_X$	Negative Power Supply Rejection, Transmit	VF_XI^+=0 Vms, V_{BB}=−5.0V V_{DC}+100 mVrms f=0 KHz-50 KHz	40			dBC
$PPSR_R$	Positive Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{CC}=5.0 V_{DC}+100 mVrms f=0 Hz-4000 Hz f=4 KHz-25 KHz f=25 KHz-50 KHz	40 40 36			dBC dB dB
$NPSR_R$	Negative Power Supply Rejection, Receive	PCM Code Equals Positive Zero V_{BB}=−5.0 V_{DC}+100 mVrms f=0 Hz-4000 Hz f=4 KHz-25 KHz f=25 KHz-50 KHz	40 40 36			dBC dB dB

Transmission Characteristics (Continued)

Unless otherwise specified: T_A=0°C to 70°C, V_{CC}=5V±5%, V_{BB}=−5V±5%, GND=0V, f=1.02 KHz, V_{IN}=0 dBm0, transmit input amplifier connected for unity-gain noninverting.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SOS	Spurious Out-of Band Signals at the Channel Output	Loop Around Measurement, 0 dBm0, 300 Hz-3400 Hz Input Applied to VF_XI^+, Measure Individual Image Signals at VF_RO				
		4600 Hz-7600 Hz			−32	dB
		7600 Hz-8400 Hz			−40	dB
		8400 Hz-100,000 Hz			−32	dB

Distortion

STD_X	Signal to Total Distortion	Sinusoidal Test Method				
STD_R	Transmit or Receive	Level=3.0 dBm0	33			dBC
	Half-Channel	=0 dBm0 to −30 dBm0	36			dBC
		=−40 dBm0 XMT	29			dBC
		RCV	30			dBC
		=−55 dBm0 XMT	14			dBC
		RCV	15			dBC
SFD_X	Single Frequency Distortion, Transmit				−46	dB
SFD_R	Single Frequency Distortion, Receive				−46	dB
IMD	Intermodulation Distortion	Loop Around Measurement, VF_X^+=−4 dBm0 to −21 dBm0, Two Frequencies in the Range 300 Hz-3400 Hz			−41	dB

Crosstalk

CT_{X-R}	Transmit to Receive Crosstalk, 0 dBm0 Transmit Level	f=300 Hz-3400 Hz, D_R=Steady PCM Code		−90	−75	dB
CT_{R-X}	Receive to Transmit Crosstalk, 0 dBm0 Receive Level	f=300 Hz-3400 Hz, VF_XI=0V		−90	−70 (Note 2)	dB

Note 1: Measured by extrapolation from the distortion test result.
Note 2: CT_{R-X} is measured with a −40dBm0 activating signal applied at VF_XI=0V

Encoding Format At D_X

	GM3054 μLaw								GM3057 A-Law (Includes Even Bit Inversion)							
V_{IN} (at GS_X)=+Full-Scale	1	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
V_{IN} (at GS_X)=0V	1	1	1	1	1	1	1	1	1	1	0	1	0	1	0	1
	0	1	1	1	1	1	1	1	0	1	0	1	0	1	0	1
V_{IN} (at GS_X)=−Full-Scale	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Application Information

POWER SUPPLIES

While the pins of the GM3054 family are well protected against electrical misuse, it is recommended that the standard CMOS practice be followed, ensuring that ground is connected to the device before any other connections are made. In applications where the printed circuit board may be pulgged into a "hot" socket with power and clocks already present, an extra long ground pin in the connector should be used.

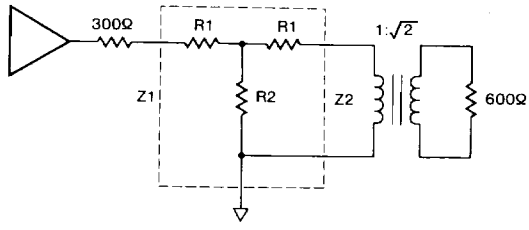
All ground connections to each device should meet at a common point as close as possible to the GND pin. This minimizes the interaction of ground return currents flowing through a common bus impedance. 0.1μF supply decoupling capacitors should be connected from this common ground point to V_{CC} and V_{BB}.

For best performance, the ground point of each CODEC/FILTER on a card should be connected to a common card ground in star formation, rather than via a ground bus. This common ground point should be decoupled to V_{CC} and V_{BB} with 10μF capacitors.

RECEIVE GAIN ADJUSTMENT

For applications where a GM3054 family CODEC/FILTER receive output must drive a 600Ω load, but a peak swing lower than ±2.5V is required, the receive gain can be easily adjusted by inserting a matched T-pad or π-pad at the output. Table II lists the required resistor vallues for 600Ω terminations. As these are generally non-standard values, the equations can be used to compute the attenuation of the closest practical set of resistors.It may be necessary to use unequal values for the R1 or R4 arms of the attenuators to achieve a precise attenuation. Generally it is tolerable to allow a small deviation of the input impedance from nominal while still maintaining a good return loss. For example a 30 dB return loss against 600Ω is obtained if the output impedance of the attenuator is in the range 282Ω to 319Ω (assuming a perfect transformer).

T-Pad Attenuator



$$R1 = Z1\left(\frac{N^2+1}{N^2-1}\right) - 2\sqrt{Z1,Z2}\left(\frac{N}{N^2-1}\right)$$

$$R2 = 2\sqrt{Z1,Z2}\left(\frac{N}{N^2-1}\right)$$

Where $N = \sqrt{\frac{\text{Power In}}{\text{Power Out}}}$

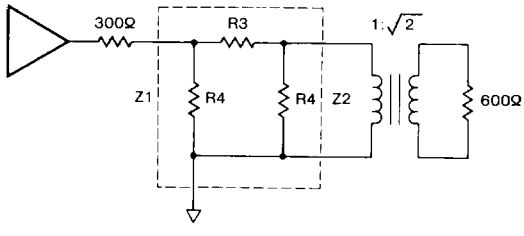
and $S = \sqrt{\frac{Z1}{Z2}}$

Also: $Z = \sqrt{Z_{SC} \cdot Z_{OC}}$

Where Z_{SC}=Impedance with short circuit termination

and Z_{OC}=Impedance with open circuit termination

π-Pad Attenuator



$$R3 = \sqrt{\frac{Z1,Z2}{2}}\left(\frac{N^2-1}{N}\right)$$

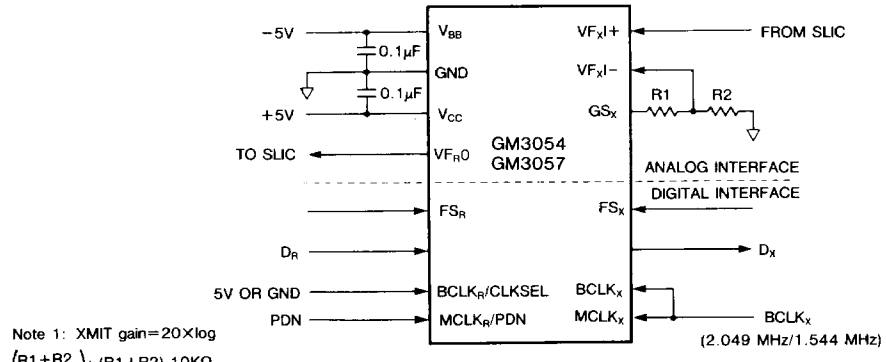
$$R3 = Z1\left(\frac{N^2-1}{N^2-2NS+1}\right)$$

Applications Information (Continued)

Table II. Attentuator Tables For Z1=Z2=300Ω (All Values In Ω)

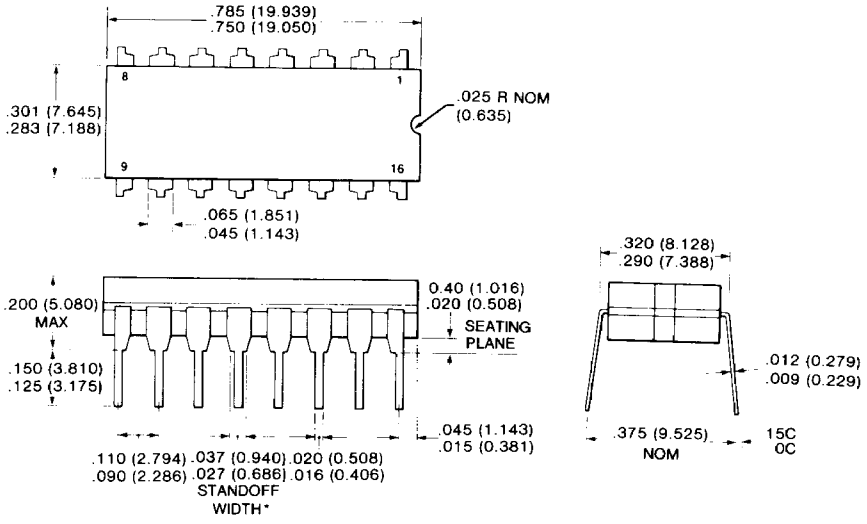
dB	R1	R2	R3	R4
0.1	1.7	26k	3.5	52k
0.2	3.5	13k	6.9	26k
0.3	5.2	6.7k	10.4	17.4k
0.4	6.9	6.5k	18.8	13k
0.5	8.5	5.2k	17.3	10.5k
0.6	10.4	4.4k	21.3	8.7k
0.7	12.1	3.7k	24.2	7.5k
0.8	13.8	3.3k	27.2	6.5k
0.9	15.5	2.9k	31.1	5.8k
1.0	17.3	2.6k	34.6	5.2k
2	34.4	1.3k	70	2.6k
3	51.3	850	107	1.8k
4	68	650	144	1.3k
5	84	494	183	1.1k
6	100	402	224	900
7	115	380	269	785
8	379	284	317	698
9	143	244	370	630
10	156	211	427	527
11	168	184	490	535
12	180	161	550	500
13	190	142	635	473
14	200	125	720	450
15	210	110	616	430
16	218	98	924	413
18	233	77	1.17k	386
20	246	61	1.5k	366

Typical Synchronous Application



Note 1: XMIT gain=20×log $\left(\frac{R1+R2}{R2}\right)$; (R1+R2) 10KΩ

16-Pin Ceramic Dual In-Line



All dimensions in inches bold and millimeters (parentheses).