IMI4350 PHASE DETECTOR

May 1998
Approved Product

CMOS LSI
PLL FREQUENCY SYNTHESIZERS

PRODUCT DESCRIPTION

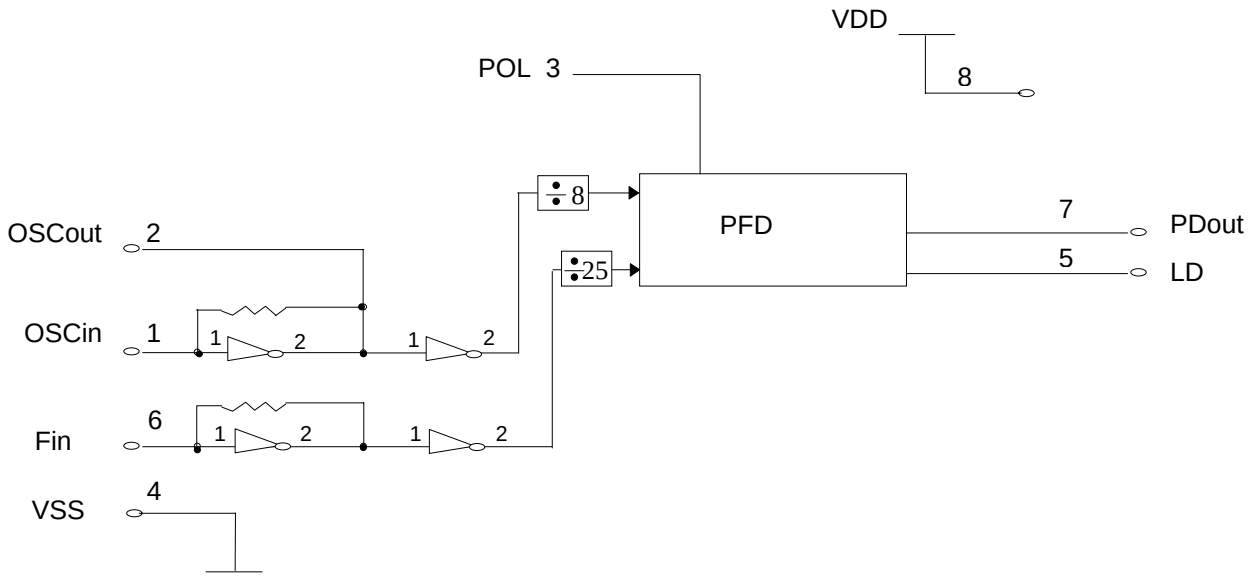
The IMI4350 is a member of a family of phaselock loop synthesizer ICs from International Microcircuits. This is a phase-frequency detector intended for use with high reference frequencies. Compatible with sinewave, ECL, TTL, and CMOS input waveforms makes the IMI4350 extremely versatile in wideband PLL applications.

The IMI4350 is a Type IV phase frequency detector which has eliminated by design the inherent dead zone which causes crossover distortion at the critical center lock point. The IMI circuitry enables consistent low noise loop designs using the simple single ended charge pump output. Lock detect output is also provided.

PRODUCT FEATURES

- >40 MHz typical input frequency
- Low power consumption CMOS
- -163 dBc/Hz total phase noise floor
- No dead zone, by design
- Lock detect output
- Polarity switch to invert PDout polarity for active filtering
- 380 µA Current Mode Charge Pump
- Unambiguous PLL acquisition
- Zero degree phase difference at lock
- ECL compatible inputs when AC coupled
- Sinewave inputs when AC coupled
- TTL, CMOS inputs can be DC coupled
- On- or off-chip reference oscillator operation
- Small 8 pin SOP package for SMT available
- 3-volt and 5-volt characterizations

BLOCK DIAGRAM



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MAXIMUM RATINGS

Voltage Relative to VSS:	-0.3V to 7V
Voltage Relative to VDD	0.3V
Storage Temperature:	-65ºC to 150ºC
Ambient Temperature:	-40º C to 85º C
Recommended Operating Range:	4.5-5.5V

This device contains circuitry to protect the inputs against damage due to high static voltages or electric field; however, precaution should be taken to avoid application for any voltage higher than the maximum rated voltages to this circuit. For proper operation, Vin and Vout should be constrained to the range:

Vss<(Vin or Vout)<VDD

Unused inputs must always be tied to an appropriate logic voltage level (either VSS or VDD).

PIN DESCRIPTIONS

PIN NO.	NAME	DESCRIPTION
1	OSCin	This input is self biased and is designed to be AC coupled for low level sinewave signals.
2	OSCout	Reference signal output can be used in conjunction with OSCin to form an internal crystal oscillator.
6	Fin	This input is intended to be AC coupled for low level sinewave signals. DC coupling can be used for CMOS logic level input signals.
4	VSS	Circuit ground.
8	VDD	Circuit positive power supply.
3	POL	Polarity swtich default is low (internal pull down).
5	LD	Loct detect output. This signal goes LOW when the loop is out of lock.
7	Pdout	Single-ended charge pump output, usually used with passive loop filters. This signal operates according to the following:
	If POL = 0	■ Frequency fv>fr at the phase detector: negative pulses. ■ Frequency fv<fr at the phase detector: positive pulses. ■ Frequency fv = fr at the phase detector: high-impedance state.
Can be used with inverting amplifier	If POL = 1	■ Frequency fv>fr at the phase detector: positive pulses. ■ Frequency fv<fr at the phase detector: negative pulses. ■ Frequency fv = fr at the phase detector: high-impedance state.

May 1998
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PLL OPERATING CHARACTERISTICS

VDD = 5 VOLTS

Characteristics		Symbol		-40ºC		0ºC		25ºC			70ºC		85ºC		Unit	Conditions
				Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max		
Dynamic	Operating Frequency	fin, fosc	Sine	-	50	-	-	-	-	50	-	40	-	40	MHz	
			Sine	-	50	-	-	-	-	50	-	40	-	40	MHz	
	Phase Noise Floor	PDNF							-160						dBc/Hz	
	Pin Capacitance	Cin		-	10			-	6	10			-	10	pF	
		Cout		-	10			-	6	10			-	10	pF	
Static	Input Voltages	VIL		1	1.5	-	1.5	-	2.75	1.5	-	1.5	-	1.5	Vdc	
		VIH		3.5	-	3.5	-	3.5	2.75	-	3.5	-	3.5	-		
	Output Voltages	VOL		-	0.05	-	0.05	-	0.0	0.05	-	.05	-	0.05	Vdc	
		VOH		4.95	-	4.95	-	4.95	5.0	-	4.95	-	4.95	-		
	Output Current	IOL	Logic	2.4	-			2.0	2.8	-			1.6	-		
			OSCout	1.2	-			1.0	1.4	-			0.8	-	mA	VOL = 0.40
		IOH	Logic	-2.4	-			-2.0	-2.8	-			-1.6	-	mA	VOH = 4.0
			OSCout	-1.2	-			-1.0	-1.4	-			-0.8	-	mA	VOH = 4.0
	Charge Pump	Icp							380						µA	Vdd = 5V
	Supply Currents	IDD		-	10	-	10	-	7	10	-	10	-	10	mA	fosc=fin-10 MHz
		ISB		-	150			-	40	150			-	150	µA	fosc=fin=0

PLL OPERATING CHARACTERISTICS

VDD = 3 VOLTS

Characteristics		Symbol		-40ºC		0ºC		25ºC			70ºC		85ºC		Unit	Conditions
				Min	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Max		
	Operating	fin,	Sine	-	40	-	-	30	-	40	-	-	-	40	MHz	
	Frequency	fosc	Sine	-	40	-	-	30	-	40	-	-	-	40	MHz	
Dynamic	Phase Noise Floor	PDNF							-155						dBc/Hz	
	Pin	Cin		-	10			-	6	10			-	10	pF	
	Capacitance	Cout		-	10			-	6	10			-	10	pF	
	Input	VIL		-	0.9	-	1.5	-	1.35	0.9	-	1.5	-	0.9	Vdc	
	Voltages	VIH		2.1	-		-	2.1	1.65	-			2.1	-		
	Output	VOL		-	0.05	-	0.05	-	0.0	0.05	-	0.05	-	0.05	Vdc	
	Voltages	VOH		2.95	-	2.95	-	2.95	3.0	-	2.95	-	2.95	-		
Static		IOL	Logic	1.6	-			1.4	2.0	-			0.8	-		
	Output		OSCout	0.8	-			0.7	1.0	-			0.4	-	mA	VOL = 0.30
	Current	IOH	Logic	-1.6	-			-1.4	-2.0	-			-0.8	-	mA	VOH = 2.4
			OSCout	-1.6	-			-0.7	-1.0	-			-0.4	-	mA	VOL = 2.4
	Charge Pump	Icp							240						µA	Vdd = 3V
	Supply	IDD		-	5	-	5	-	3	5	-	5	-	5	mA	fosc=fin-10 MHz
	Currents	ISB		-	150			-	40	150			-	150	µA	fosc=fin=0

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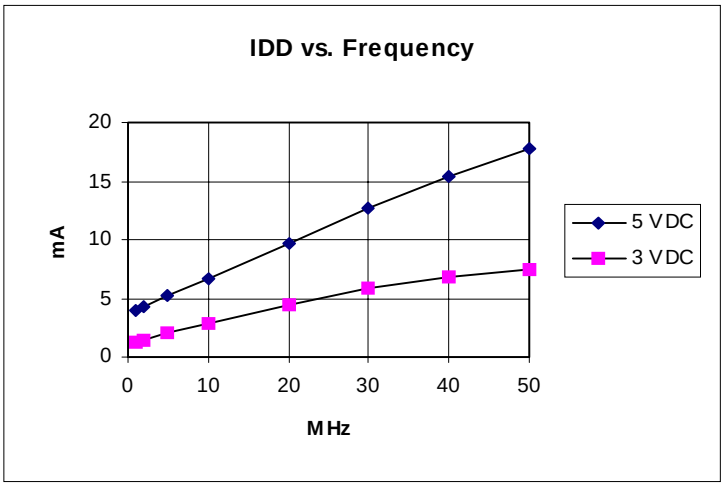

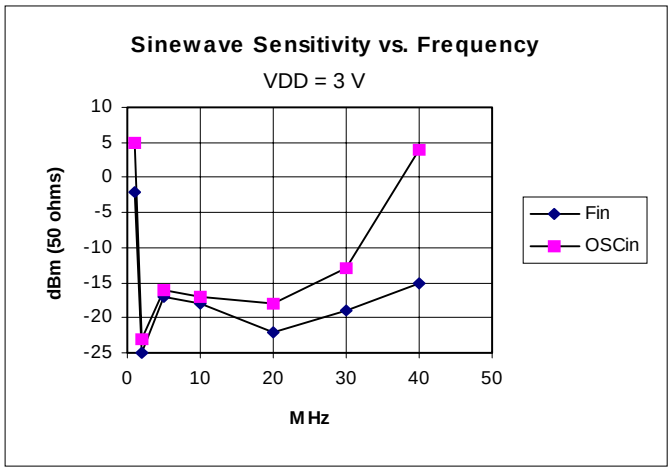

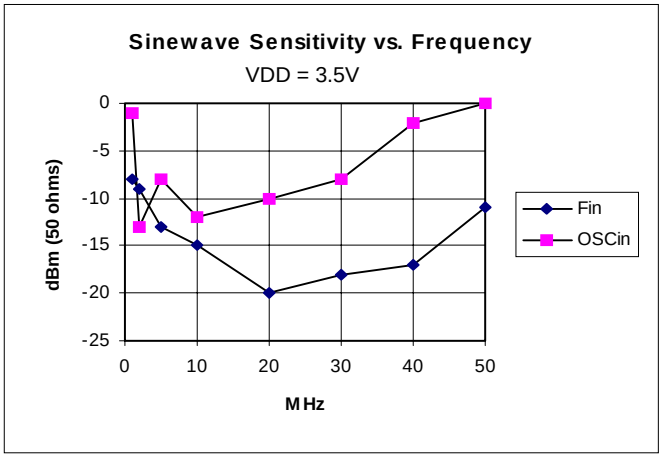

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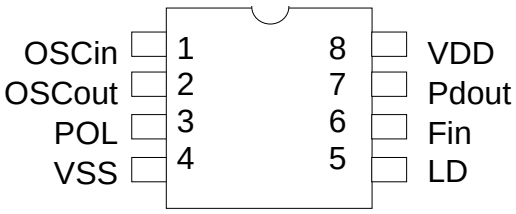
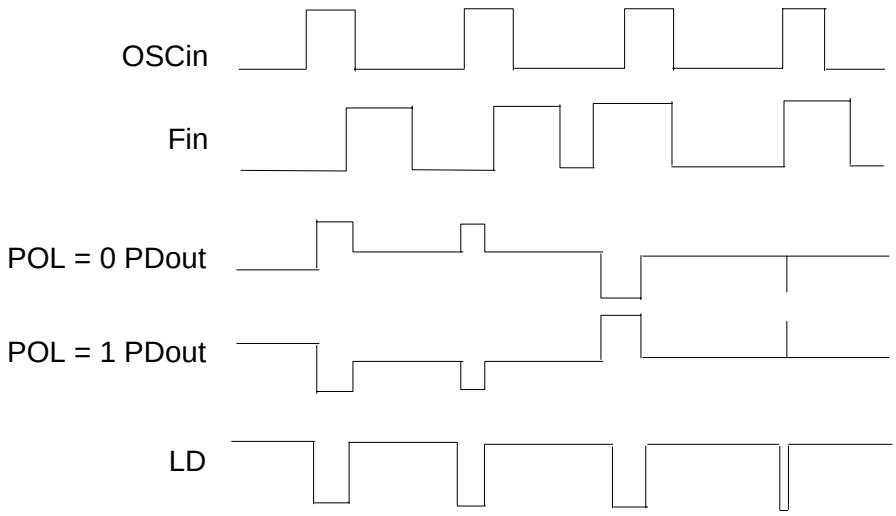
CONNECTION DIAGRAM



PHASE DETECTOR OUTPUT WAVEFORMS



Note: The Pdout state is equal to either VDD or VSS when active. When not active, the output is high impedance and the voltage at that pin is determined by the low pass filter capacitor.

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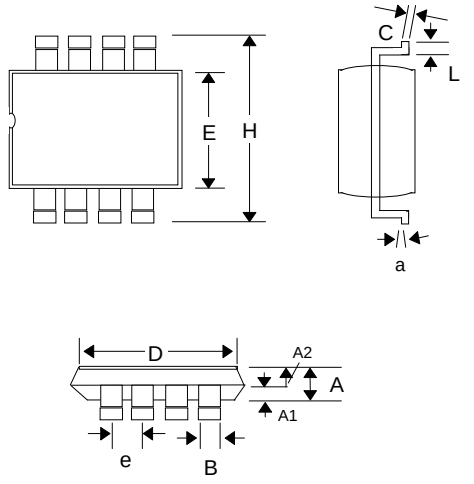
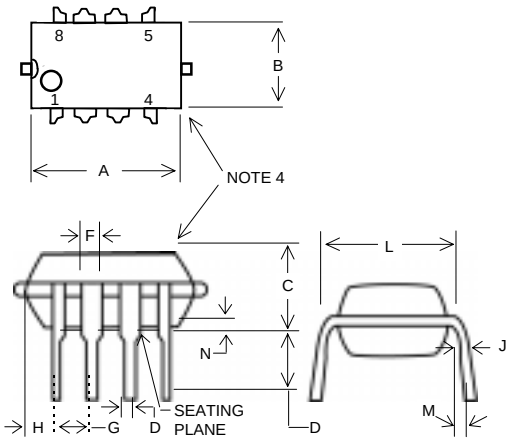
PACKAGE DRAWING AND DIMENSIONS



SOP PACKAGE

8-PIN SOP DIMENSIONS						
	INCHES			MILLIMETERS		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	0.080	-	-	2.03
A_1	0.0	0.0039	0.0078	0.0	0.10	0.20
A2	0.069	0.071	0.072	1.77	1.82	1.83
B	0.014	.016	.018	0.35	.040	0.45
C	0.007	-	0.009	0.17	-	0.23
D	0.203	0.207	0.210	5.15	5.25	5.35
E	0.205	0.208	0.213	5.20	5.30	5.40
e	0.050 BSC			1.27 BSC		
H	0.303	0.314	0.318	7.70	8.00	8.10
a	3°	6°	9°	3°	6°	9°
L	0.025	0.03	0.033	0.65	0.75	0.85

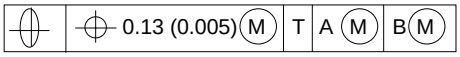


PDIP PACKAGE

8-PIN PLASTIC DIP DIMENSIONS						
	MILLIMETER			INCHES		
SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
A	9.40	-	10.16	0.370	-	0.400
B	6.10	-	6.60	0.240	-	0.260
C	3.94	-	4.45	0.155	-	.175
D	0.38	-	0.51	0.015	-	0.020
F	1.02	-	1.52	0.040	-	0.060
G	2.54 BSC			0.100 BSC		
H	0.76	-	1.27	0.030	-	0.050
J	0.20	-	0.30	0.008	-	0.012
K	2.92	-	3.43	0.115	-	0.135
L	7.62 BSC			0.300 BSC		
M	-	-	8°	-	-	8°
N	0.51	-	0.76	0.020	-	0.030

NOTES:

1. LEAD POSITIONAL TOLERANCE:



2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL
3. PACKAGE CONTOUR OPTION (ROUND OR SQUARE CORNERS)
4. DIMENSIONS A AND B ARE DATUMS
5. DIMENSIONING AND TOLERANCE PER ANSI Y14.5M, 1982

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ORDERING INFORMATION		
Part Number	**Package Type**	**Production Flow**
IMI4350xPB	8 PIN Plastic DIP	Industrial, -40ºC to + 85ºC
IMI4350xYB	8 PIN SOP	Industrial, -40ºC to + 85ºC

NOTE: The “x” following the IMI Device Number denotes the device revision. The ordering part number is formed by a combination of device number, device revision, package style, and screening as shown below.

Marking: Example: FS4350x
Date Code
Lot #

IMI4350xPB