MAS9142

Power Amplifier Controller (PAC) and 2.8 V, 50 mA LDO Voltage Regulator

- **Temperature Compensation of Sensor Signal**
- **Bias Current Source for Detector Diodes**
- **Applicable for a Wide Range of Power Amplifiers**
- **Low Noise LDO Regulator Included**

DESCRIPTION

MAS9142 is designed for use in both the GSM900 and DCS1800 systems and particularly with Hitachi PF08103B power amplifier module. Other PA modules can be used with the MAS9142, but external compensation elements may be required to maintain the stability of the PA control loop. MAS9142 incorporates the power detector biasing components, RC-filtering for power ramping signal, operational amplifier with AC feedback and a low dropout (LDO) voltage regulator. The regulator has the output voltage of 2.8 V and the maximum load current of 50 mA for generating supply voltage for VCO/Modulator in the radio channel of a mobile phone. The regulator's output is short-circuit protected. Both the PA control loop and LDO voltage regulator have common thermal (over-temperature) protection with 10 °C hysteresis.

FEATURES

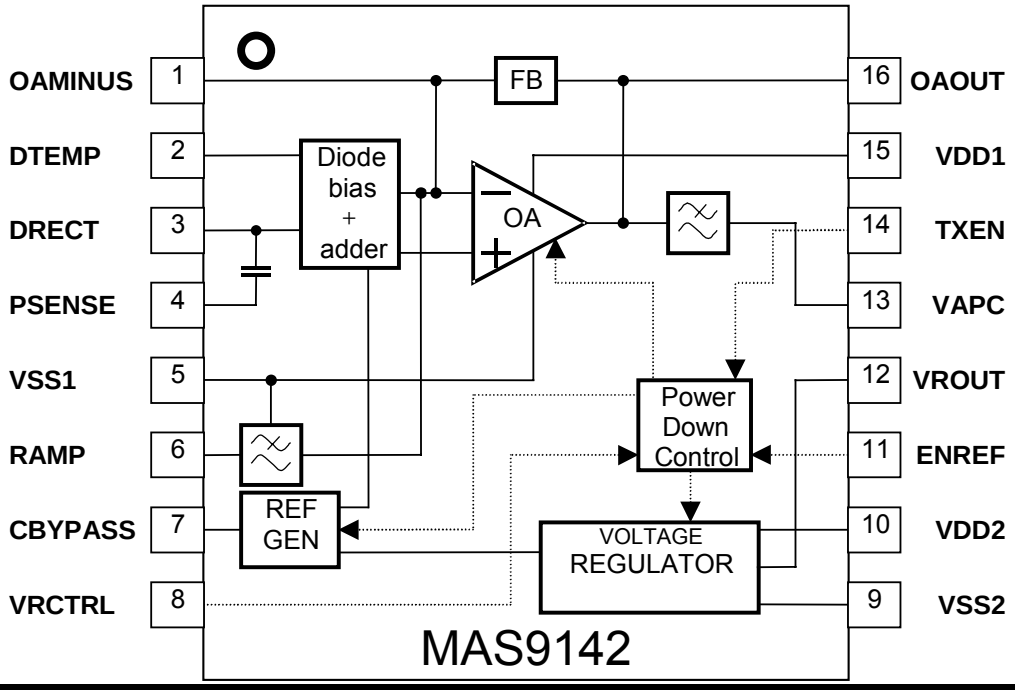
- Two functional blocks: Power Amplifier Controller and LDO Voltage Regulator
- Low current consumption
- Temperature compensated biasing for external RF power detection Schottky diodes
- Both PAC loop and LDO voltage regulator have temperature-controlled power-down feature
- LDO voltage regulator with short circuit current protection
- Excellent ripple rejection in regulator
- Various operating modes provide greater flexibility

APPLICATION

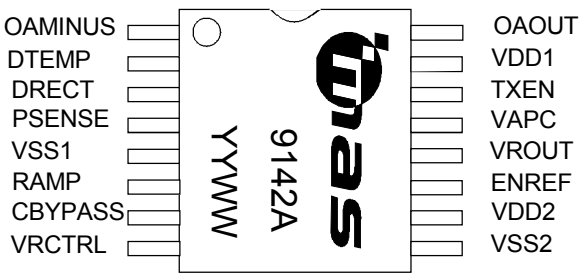
- Dual- and Triple-Band Cellular Phones
- PCMCIA GSM/DCS data communications
- GSM based controller for vehicles
- Other RF power controlling applications

NOT AVAILABLE IN THE USA AND CANADA

BLOCK DIAGRAM



PIN CONFIGURATION



Top Marking Definitions:
YYWW = Year Week

PIN DESCRIPTION

Pin name	Pin No	Type	Function
OAMINUS	1	I	OA Inverting Input (for Optional External Feedback Components)
DTEMP	2	I	Schottky Diode for Temperature Compensation
DRECT	3	I	RF Rectifier Schottky Diode
PSENSE	4	I	Power Measurement Input (from Directional Coupler)
VSS1	5	G	Ground for Power Amplifier Controller
RAMP	6	I	GSM Power Ramping Signal Input
CBYPASS	7	I	Voltage Regulator Reference Voltage Bypass Capacitor
VRCTRL (note 1)	8	I	Voltage Regulator Enable
VSS2	9	G	Ground for Voltage Regulator
VDD2	10	P	Supply for Voltage Regulator
ENREF (note 1)	11	I	Voltage Reference Enable ('warm-up')
VROUT	12	O	Voltage Regulator Output
VAPC	13	O	Automatic Power Control Output Voltage (to PA)
TXEN (note 1)	14	I	Transmit Enable
VDD1	15	P	Supply for Power Amplifier Controller
OAOUT	16	O	OA Output (for Optional External Feedback Components)

NOTE 1:Digital control pads with pull-down resistor, Active-High, CMOS-compatible voltage levels.
G = Ground, I = Input, O = Output, P = Power

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit	Note
Supply Voltage	V_{DD}		–0.3	6.5	V	
Voltage Range for All Pins			–0.3	6.5	V	1)
Voltage Range for Pins 2, 3 and 4			–6	6.5	V	
Storage Temperature	T_S		–55	+125	°C	
ESD Rating		Human Body Model, HBM		1	kV	
Operating Ambient Temperature	T_{OP}		–40	+95	°C	

NOTE: Except PSENSE (4), DRECT (3) and DTEMP (2) pins

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3.0	3.6	5.3	V
Supply Current	I_{DD}		0.5		2.0	mA
Operating Temperature	T_A		–30		+85	°C

ELECTRICAL CHARACTERISTICS

For typical values T_A = 27°C, for min/max values T_A = -30°C to +85°C, C_{IN} = 330 nF, C_L = 1 µF, C_{BYP} = 100 nF unless otherwise noted

Common Characteristics

◆ Thermal Protection

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Threshold High	T_H		145	155	165	°C
Threshold Low	T_L		135	145	155	°C

The hysteresis of 10°C prevents the device from turning on too soon after thermal shut-down.

◆ Digital Control Pin Parameters

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage HIGH-state LOW-state	V_{IN} V_{IN} (H) V_{IN} (L)	For Pin 8 (VRCTRL), pin 11 (ENREF) and pin 14 (TXEN)	0 2.0		V_{DD} 0.3	V
Input Current, in HIGH state	$I_{IN,H}$	For Pin 8 (VRCTRL), pin 11 (ENREF) and pin 14 (TXEN)	3.8	4.5	7.8	µA

◆ **Current Parameters**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Quiescent Supply Currents	I_{DD}	Total power down		0.01	5 (note 1)	µA
		PAC on		0.9	1.8	mA
		References 'warm-up'		190	300	µA
		LDO Regulator on		320	450	µA
		Whole chip on		1.1	2.0	mA

NOTE 1: Test limit. High value is used for speeding up production testing.

◆ **Power Dissipation**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Power Dissipation	P_d	V_{CC} = 6.0 V, T_A = 85 °C			285	mW
Power Dissipation	P_d	V_{CC} = 6.0 V, T_A = 25 °C			700	mW

Maximum power dissipation is calculated from $P_d=(T_j–T_A)/R_{\Theta JA}$, where $R_{\Theta JA}$ is thermal resistance of TSSOP16 package, $R_{\Theta JA}$ = 144 °C /W and T_j is maximum allowed junction temperature, T_j = 125 °C.

Regulator

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Regulator Output Current	I_{OUT}		0		50	mA
Output Current Limit	I_{MAX}		75	150	340	mA
Ground Pin Current	I_{VSS2}	No load for typical value, I_{OUT} = 50mA, T = 85 °C		320		µA
Regulator Output Voltage	V_{OUT}	V_{DD} = 3.6 V, I_{OUT} = 0 mA	2.75	2.80	2.85	V
Regulator Dropout Voltage	V_{DROP}	I_{OUT} = 50 mA		0.14	0.17	V
Load Regulation	$\frac{\Delta V_{OUT}}{\Delta I_{OUT}}$	V_{DD} = 3.6 V, I_{OUT} from 0 to 50 mA			0.5	$\frac{mV}{mA}$
Line Regulation	ΔV_{OUT}	I_{OUT} = 50 mA, V_{DD} from 6.0 V to 3.6 V		0.25	1.2	mV
PSRR		f = 1 kHz f = 10 kHz f = 100 kHz		68 54 37		dB
Output Noise Voltage	V_{RMS}	100 Hz < f < 100 kHz, C_{BYPASS} = 100 nF C_L = 1 µF, I_{OUT} = 50 mA		37		µVrms
Rise Time (V_{OUT} from 10% to 90%)	t_r	C_L = 1 µF, ENREF is ON at least for 10 ms		14	26	µs
Delay Time (From V_{RCTRL} 50% to V_{OUT} 50%)	t_d	C_L = 1 µF, ENREF is ON at least for 10 ms		15	35	µs
Overshoot		C_L = 1 µF		0.5	8	%
Settling Time (from V_{OUT} 90% to max ±0.1% fluctuation)		C_L = 1 µF			70	µs

◆ **External Capacitors**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Capacitor for Regulator	C_L		1			µF
Effective Series Resistance	ESR		0.05	1	3	Ω
Bypass Capacitor	C_{BYPASS}			100		nF

Power Amplifier Controller

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Maximum Output Current (sink and source)	I_{OUT}			3	5	mA
Output Voltage Range	V_{OUT}	I_{OUT} = 3 mA	0		V_{DD} -0.4 V	V
RF input power range	P_{IN}	At DRECT pin	–14		20	dBm
RAMP lowpass filter corner frequency	f_{-3dB}	2nd order RC filter	40		160	kHz
Bias current for external Schottky diodes	I_{DRECT}, I_{DTEMP}	Independent of V_{DD}	21.5	28	43.6	µA
PSRR		f = 1 kHz f = 10 kHz		56 41		dB

◆ **Parameters of Operational Amplifier**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Offset Voltage	V_{OS}			0.2	1.2	mV
DC gain	A_{VOL}	I_{OUT} from 0 to 3 mA		100		dB
Unity Gain Bandwidth	F_T			3.5		MHz
Phase margin	Φ_m	Unity-Gain buffer configuration	55	65	80	deg
Gain margin	A_m	Unity-Gain buffer configuration	13	15	26	dB
Small-signal Slew Rate	SR_S	V_- = 0.13 V, V_+ = 0…0.135 V step		0.2		V/µs
Large-signal Slew Rate	SR_L	V_- = 0.13 V, V_+ = 0…3 V step		1.5		V/µs

FUNCTION DESCRIPTION

MAS9142 contains two functionally distinct parts – the radio frequency power amplifier controller (PAC) and low-dropout voltage regulator (LDOVR). Both blocks have separate power lines, which must be connected together on the system printed circuit board.

PAC and LDOVR use common thermal protection and reference voltage generator blocks. There are three power-down pins on MAS9142: TXEN for PA controller, VRCTRL for the voltage regulator and ENREF for the reference generator and thermal protection block. All power-down pins are pull-down type and use standard CMOS control voltage levels and positive logic. The operating modes of MAS9142 are listed in the table below:

VRCTRL	ENREF	TXEN	Mode
0	0	0	Total power-down
0	0	1	PAC on
0	1	0	References 'warm-up'
0	1	1	PAC on
1	0	0	Voltage regulator on
1	0	1	Whole chip on
1	1	0	Voltage regulator on
1	1	1	Whole chip on

The ENREF control pin is included to provide flexibility: it can be used to switch on the voltage reference block in a sufficient amount of time before the regulator or PA controller. When not used, the two other signals will turn the internal reference generator on using a logical 'OR' operation. The start-up time of the reference generator is approximately 10 ms due to the large time constant generated by the external capacitor connected to CBYPASS pin and an on-chip resistor.

Power Amplifier Controller (PAC)

The PAC is an operational amplifier based controller for adjusting the output power of a radio frequency power amplifier. It takes a voltage input at the RAMP pin and adjusts the output power of the power amplifier to a known value. This power value depends on the external rectification diodes, the directional coupler and the power amplifier control curve.

The measurement results are obtained using MAS9142 PA controller, a Hitachi PF08103B RF power amplifier, an LDC15D type directional coupler with coupling attenuation of 14 dB and a Schottky diode pair BAT62 in a feedback loop. The measurement results are shown in Figure 1. It can be seen that a ±3σ corridor is approximately 1 dB even at very low power levels. The measurements were carried out at room temperature with a supply voltage of 3.6 V and RF input frequency of 900 MHz.

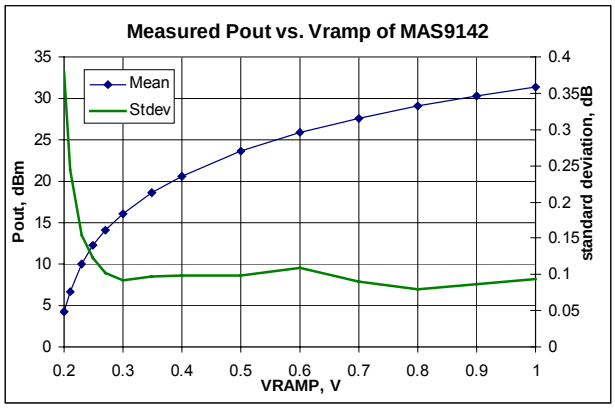


Figure 1. MAS9142 measurement results

To achieve a better power supply rejection ratio for the PAC, the rectification diode biasing is made using a on-chip 2.8 V voltage reference generator and biasing resistors. The bias current can vary from sample to sample, but is constant in the whole operating temperature and supply voltage range with accuracy of ±2%.

MAS9142 also guarantees that the radio power is ramped up and down properly, generating only few spurious frequency components. For that reason, the control signal that comes from a D/A converter to the PAC is first low-pass filtered inside MAS9142 chip. There are also other RC time constants on the chip, which help in assuring the stability of the PA control loop. An optional stabilising capacitor can be connected between the OAMINUS and OAOUT pins of MAS9142. In the measurement setup described above, the additional compensation capacitor was not used.

Low-Dropout Voltage Regulator (LDOVR)

The LDOVR is a high performance, low dropout voltage regulator including short circuit current and thermal protection. The circuit also contains necessary reference voltage and current generators, so minimum number of external components are required.

APPLICATION INFORMATION

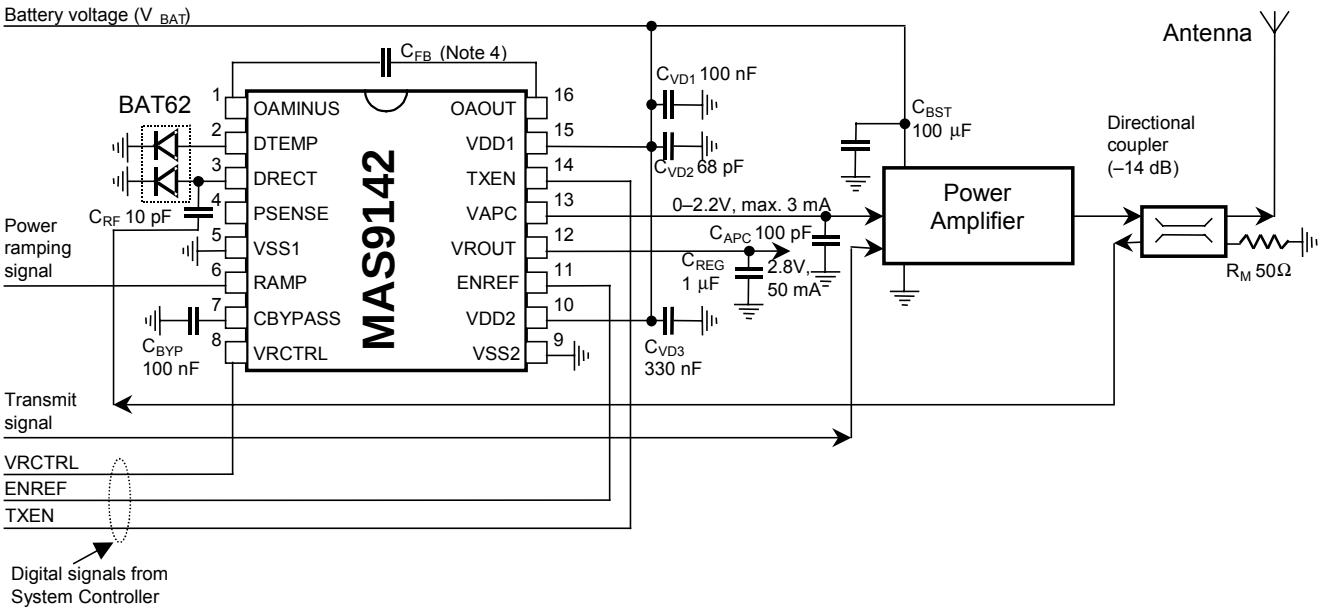
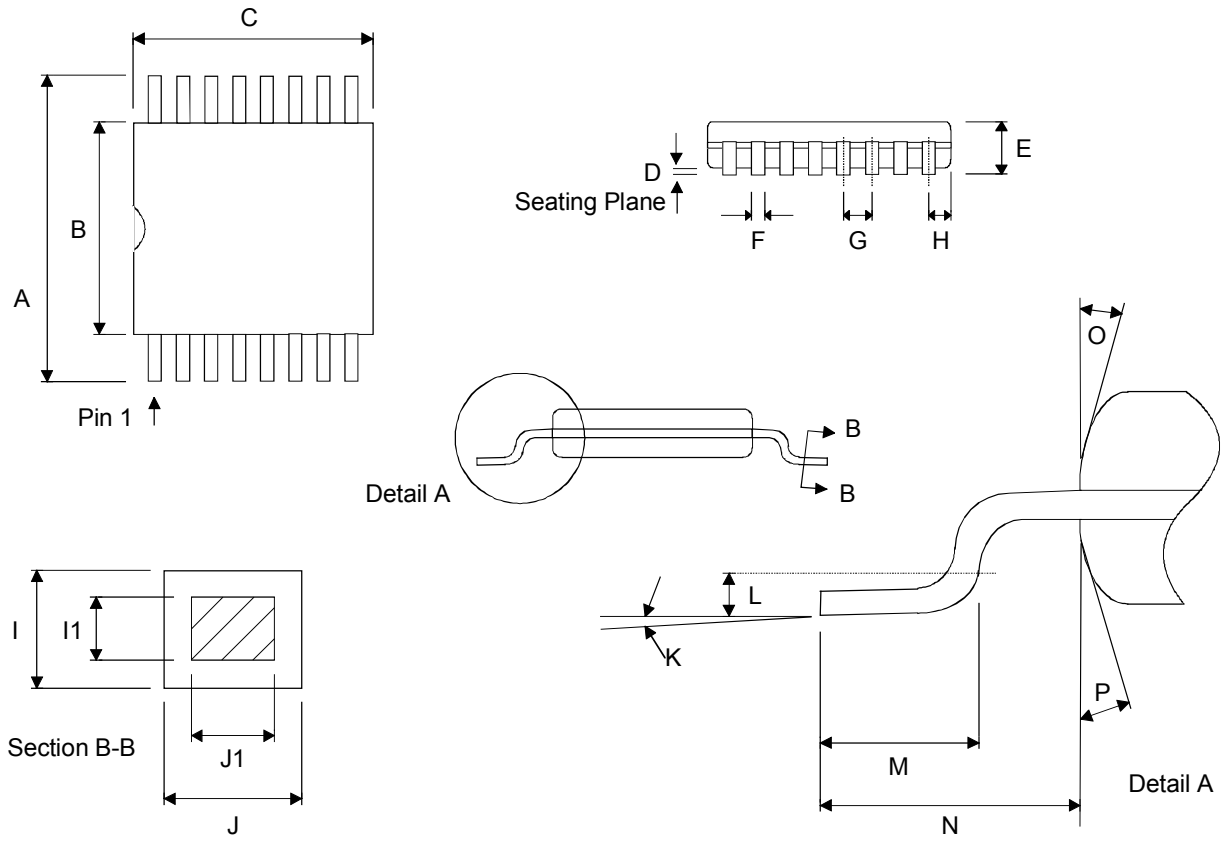


Figure 2. Application diagram of MAS9142

The application circuit diagram is shown in Figure 2.

1. The VSS1 (ground for PAC, pin 5) and VSS2 (ground for regulator, pin 9) must be connected together.
2. The VDD1 (pin 15) and VDD2 (pin 10) must be connected together.
3. There are no external biasing components needed for the RF rectifier, they are on the chip.
4. Loop time constant adjusting capacitor C_{FB} between the OAMINUS (pin 1) and OAOUT (pin 16) is optional and its recommended value is between 100 pF and 300 pF. This capacitor is not necessary when using Hitachi PF08103B power amplifier and Murata LDC15D type directional coupler.

PACKAGE (TSSOP16) OUTLINES



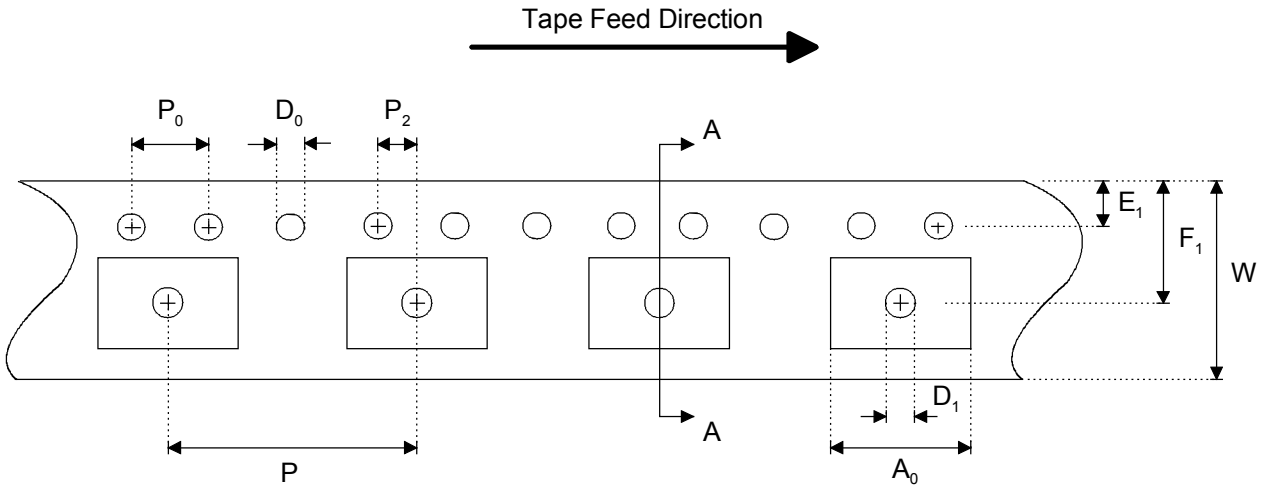
Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	4.90	5.10	mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M (The length of a terminal for soldering to a substrate)	0.50	0.75	mm
N	1.00 REF		mm
O	12°		
P	12°		

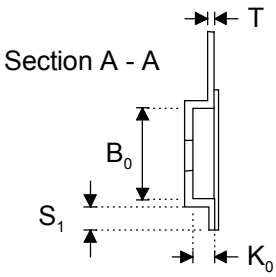
Dimensions do not include mold flash, protrusions, or gate burrs.
All dimensions are in accordance with JEDEC standard MO-153.

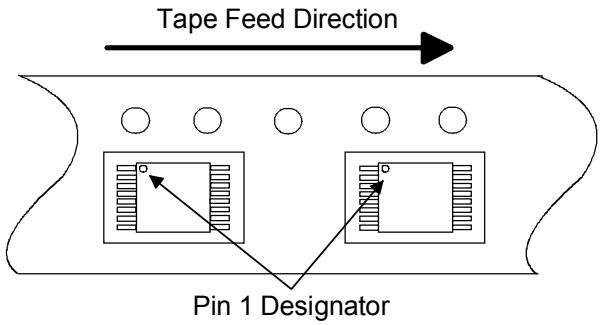
SOLDERING INFORMATION

Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20 2*220°C
Maximum Temperature	240°C
Maximum Number of Reflow Cycles	2
Reflow profile	Thermal profile parameters stated in JESD22-A113 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Sn 85% Pb 15%

EMBOSSED TAPE SPECIFICATIONS



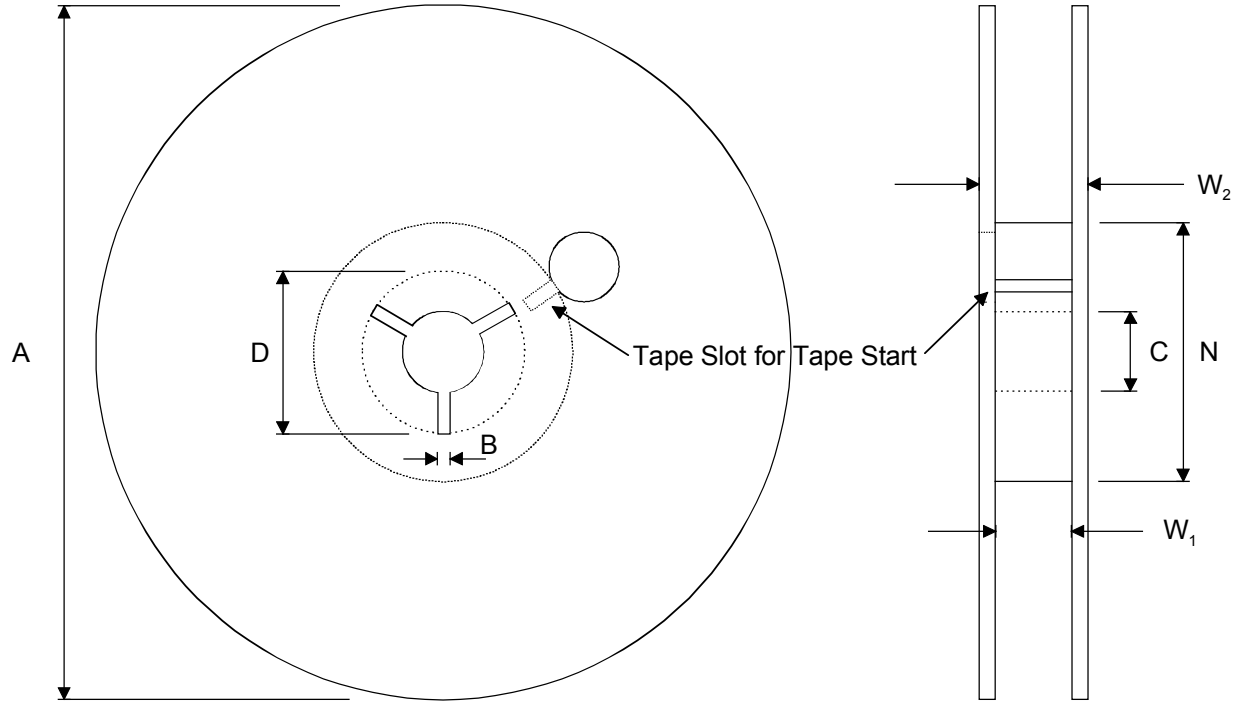




Dimension	Min	Max	Unit
A_0	6.50	6.70	mm
B_0	5.20	5.40	mm
D_0	1.50 +0.10 / -0.00		mm
D_1	1.50		mm
E_1	1.65	1.85	mm
F_1	7.20	7.30	mm
K_0	1.20	1.40	mm
P	11.90	12.10	mm
P_0	4.0		mm
P_2	1.95	2.05	mm
S_1	0.6		mm
T	0.25	0.35	mm
W	11.70	12.30	mm

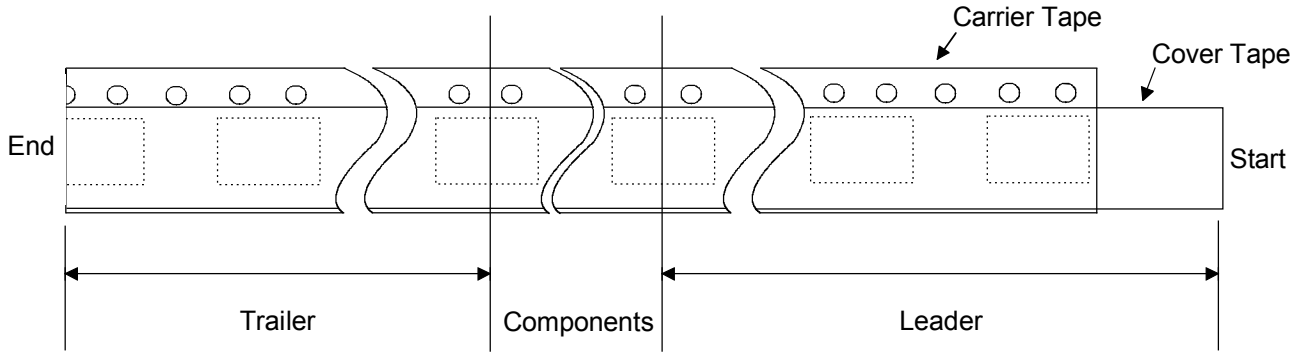
All dimensions are in accordance with EIA-481 Standard.

REEL SPECIFICATIONS



2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Package	Comments
MAS9142AUA1-T	PAC & 2.8 V LDO Regulator	TSSOP16	Tape & Reel

LOCAL DISTRIBUTOR

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