Am1402A/Am1403A/Am1404A
Am2802/Am2803/Am2804

1024-Bit Dynamic Shift Registers

Distinctive Characteristics

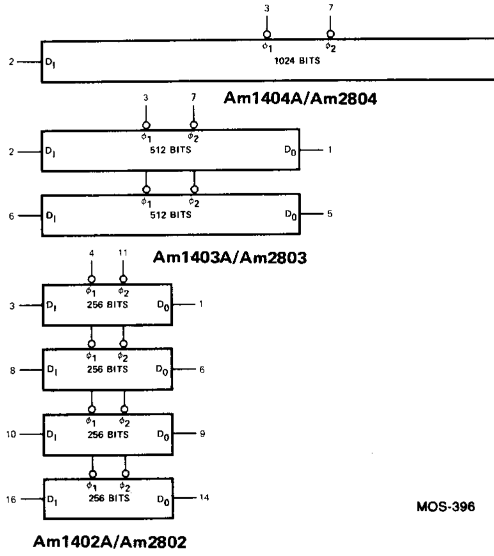
- Quad 256-bit, dual 512-bit, single 1024-bit
- 10 MHz frequency operation guaranteed for Am2802, Am2803 and Am2804.
- Low power dissipation of 0.1 mW/bit at 1 MHz
- DTL and TTL compatible
- Both military and commercial grade devices available
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Electrically tested and optically inspected die for the assemblers of hybrid products

FUNCTIONAL DESCRIPTION

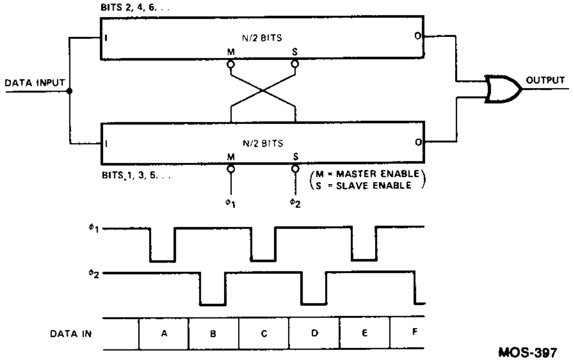
The Am1402A, 3A, and 4A are 1024-bit silicon gate dynamic shift registers. The low threshold characteristics of this technology allow high-speed operation and DTL and TTL compatibility. The Am1402A is a quad 256-bit device; the Am1403A is a dual 512-bit register; and the Am1404A is a single 1024-bit register. All three devices require two-phase non-overlapping clocks, and provide a one-bit shift on each clock pulse. The Am2802, 3, and 4 registers are functionally identical to the Am1402A, 3A, and 4A, but are guaranteed to operate over frequencies from 400Hz to 10MHz.

BLOCK DIAGRAMS

Am1402A/1403A/1404A Shift Registers



Functional Equivalent of Each Register



Since the two registers shift on opposite clock pulses, a new data bit is entered on both ϕ_1 and ϕ_2. Data entering the register on ϕ_1 will appear at the output on ϕ_1 (from the negative edge of ϕ_1 to the negative edge of ϕ_2).

ORDERING INFORMATION

Part Number	Package Type	Temperature Range	Standard Speed Range Order Number	Extended Speed Range Order Number
Am1402A/ 2802	Hermetic DIP	0°C to +70°C	AM1402A	AM2802DC
	Hermetic DIP	−55°C to+125°C	AM1402ADM	AM2802DM
	Molded DIP	0°C to +70°C	AM1402APC	AM2802PC
Am1403A/ 2803	TO-99	0°C to +70°C	AM1403A	AM2803HC
	TO-99	−55°C to +125°C	AM1403AHM	AM2803HM
	Molded DIP	0°C to +70°C	AM1403APC	AM2803PC
Am1404A/ 2804	TO-99	0°C to +70°C	AM1404A	AM2804HC
	TO-99	−55°C to +125°C	AM1404AHM	AM2804HM
	Mini DIP Plastic	0°C to +70°C	AM1404APC	AM2804PC

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +160°C
Temperature Under Bias	−55°C to +125°C
Power Dissipation (Note 1)	600 mW
Data and Clock Input Voltages with respect to most Positive Supply Voltage, V_{CC}	0.3 V to −20 V
Power Supply Voltage, V_{DD} with respect to V_{CC}	0.3 V to −20 V

OPERATING RANGE

Part Number	V_{CC}	V_{DD}	Temperature Range
Am1402A, Am1403A, Am1404A	5V ±5%	−4.75V to −9.45V	0°C to +70°C
Am1402ADM, Am1403AHM, Am1404AHM	5V ±5%	−4.75V to −9.45V	−55°C to +125°C
Am2802DC, Am2803HC, Am2804HC	5V ±5%	−5V ±5%	0°C to +70°C
Am2802DM, Am2803HM, Am2804HM	5V ±5%	−5V ±5%	−55°C to +125°C

ELECTRICAL CHARACTERISTICS over operating range

Parameters	Description	Test Conditions		Am1402A, 3A, 4A			Am2802, 3, 4			Units
				Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{IH}	Input HIGH Voltage			V_{CC}-2.0			V_{CC}-2.0			V
V_{IL}	Input LOW Voltage			V_{CC}-10		V_{CC}-4.2	V_{CC}-10		V_{CC}-4.2	V
I_I	Input Current	T_A = 25°C			<10	500		<10	500	nA
I_O	Output Leakage Current	T_A = 25°C, V_{OUT} = 0V			<10	1000		<10	1000	nA
$I_{\phi L}$	Clock Leakage Current	T_A = 25°C, V_ϕ = −12V			10	1000		10	1000	nA
V_{OH}	Output HIGH Voltage Driving TTL	R_L = 3k to V_{DD}, V_{DD} = −5V ±5%		2.4	3.5		V_{CC}-1.9	V_{CC}-1		
	Output HIGH Voltage Driving MOS	R_L = 4.7k to V_{DD}, V_{DD} = −5V ±5%		V_{CC}-1.9	V_{CC}-1		V_{CC}-1.9	V_{CC}-1		V
	Output HIGH Voltage Driving TTL	R_L = 4.7k to V_{DD}, V_{DD} = −9V ±5%		2.4	3.5					
	Output HIGH Voltage Driving MOS	R_L = 6.2k to V_{DD}, 3.9k to V_{CC} V_{DD} = −9V ±5%		V_{CC}-1.9	V_{CC}-1					
V_{OL}	Output LOW Voltage	V_{DD} = −5V ±5%, R_L = 3k to V_{DD}, I_{OL} = −1.6mA			−0.3	0.5		−0.3	0.5	V
		R_L = 4.7k to V_{DD} V_{DD} = −9V ±5%, I_{OL} = −1.6mA			−0.3	0.5				
$V_{\phi H}$	Clock Input HIGH Level			V_{CC}-1		V_{CC}+0.3	V_{CC}-1		V_{CC}+0.3	V
$V_{\phi L}$	Clock Input LOW Level	V_{DD} = −5V ±5%		V_{CC}-15		V_{CC}-17	V_{CC}-15		V_{CC}-17	V
		V_{DD} = −9V ±5%		V_{CC}-12.6		V_{CC}-14.7	V_{CC}-12.6		V_{CC}-14.7	
$I_{DD}(-5)$ (Note 1)	V_{DD} Current, V_{DD} = −5V ±5%	5MHz Data Rate 33% Duty Cycle $V_{\phi L}$ = V_{CC}-17V	T_A = 25°C		40	50		40	50	mA
			T_A = 0°C			56			56	
			T_A = −55°C						70	
	V_{DD} Current, V_{DD} = −5V ±5%	10MHz Data Rate 40% Duty Cycle $V_{\phi L}$ = V_{CC}-17	T_A = 25°C					50	60	mA
			T_A = 0°C						68	
			T_A = −55°C						80	
$I_{DD}(-9)$ (Note 1)	V_{DD} Current, V_{DD} = −9V ±5%	3MHz Data Rate 26% Duty Cycle $V_{\phi L}$ = V_{CC}-14.7V	T_A = 25°C		30	40		30	40	
			T_A = 0°C			45			45	mA
			T_A = −55°C						60	

Note: 1. Power dissipation is directly proportional to clock duty cycle and independent of frequency. The duty cycle is the clock LOW time (one clock line) divided by the clock period. At V_{DD} = −9V the maximum duty cycle is 26%. The duty cycle should be kept as small as possible to minimize power dissipation.

SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

Am1402A/Am1403A/Am1404A

Parameter	Description	Test Conditions	$V_{DD} = -5$ V ±5% (Test Load 1) Min.	Typ.	Max.	$V_{DD} = -9$ V ±5% (Test Load 2) Min.	Typ.	Max.	Units
f_C	Clock Frequency Range		(Note 1)		2.5	(Note 1)		1.5	MHz
f_d	Data Repetition Rate		(Note 1)		5.0	(Note 1)		3.0	MHz
$t_{\phi PW}$	Clock Pulse Width		0.13		10	0.17		10	μs
$t_{\phi d}$	Clock Pulse Delay (Note 2)	$t_{\phi PW}$ = 130 ns	10		(Note 2)	10		(Note 2)	ns
t_f, t_r	Clock Pulse Rise/Fall Time				1000			1000	ns
t_s	Data Set Up Time	$t_r = t_f \leqslant 50$ ns	30			60			ns
t_h	Data Hold Time	$t_r = t_f \leqslant 50$ ns	20			20			ns
t_{pd+}, t_{pd-}	Clock to Data Out Delay				90			110	ns
C_{IN}*	Input Capacitance	@ 1 MHz, 250 mVPP		5	10		5	10	pF
C_{OUT}*	Output Capacitance	@ 1 MHz, 250 mVPP		5	10		5	10	pF
C_ϕ*	Clock Capacitance	@ 1 MHz, 250 mVPP		110	140		110	140	pF

SWITCHING CHARACTERISTICS AND OPERATING CONDITIONS (Over Operating Range)

Am2802/Am2803/Am2804

Clock Pulse Width = 70nsec
Clock LOW Level = ($V_{CC}-15$)

Parameter	Description	Test Conditions	$V_{DD} = -5$ V ±5% (Test Load 1) Min.	Typ.	Max.	Units
f_C	Clock Frequency Range	$t_r = t_f = 10$ ns	(Note 1)		5.0 (Note 4)	MHz
f_d	Data Repetition Rate (Note 1)		(Note 3)		10.0 (Note 4)	MHz
$t_{\phi PW}$	Clock Pulse Width		0.07		10	μs
$t_{\phi d}$	Clock Pulse Delay	$t_{\phi PW}$ = 70 ns	10		(Note 2)	ns
t_f, t_r	Clock Pulse Rise/Fall Time				1000	ns
t_s	Data Set Up Time		30			ns
t_h	Data Hold Time		20			ns
t_{pd+}, t_{pd-}	Clock to Data Out Delay				90	ns

Notes:

1. See minimum operating frequency graph for low limits on data rep. rate.
2. Upper limit on $t_{\phi d}$ is determined by minimum frequency.
3. See max clock pulse delay graph for guarantee.
4. For additional information on 10MHz operation (5MHz clock rate) see AMD application note dated July 1973 on "Applications of Dynamic Shift Registers."

DESCRIPTION OF TERMS

OPERATIONAL TERMS

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.
V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} into junction of output and load resistor.
V_{IH} Logic HIGH input voltage.
V_{IL} Logic LOW input voltage.
V_{OL} Clock LOW input voltage.
V_{OH} Clock HIGH input voltage.
I_I Input leakage current.
I_O Output leakage current.
I_{DD} Power supply current.
C_{IN} Input capacitance.
C_ϕ Input clock capacitance.
C_{OUT} Output capacitance.

FUNCTIONAL TERMS

ϕ_1, ϕ_2 The two clock phases required by the dynamic shift register.
f_c The clock frequency of the shift register.
f_d The input data repetition rate.

SWITCHING TERMS

$t_{\phi d}$ The delay between the LOW to HIGH transition of a clock phase to the HIGH to LOW transition of the other clock phase.

$t_{\phi PW}$ The clock pulse widths necessary for correct operation.

t_f, t_r The clock pulse rise and fall times necessary for correct operation.

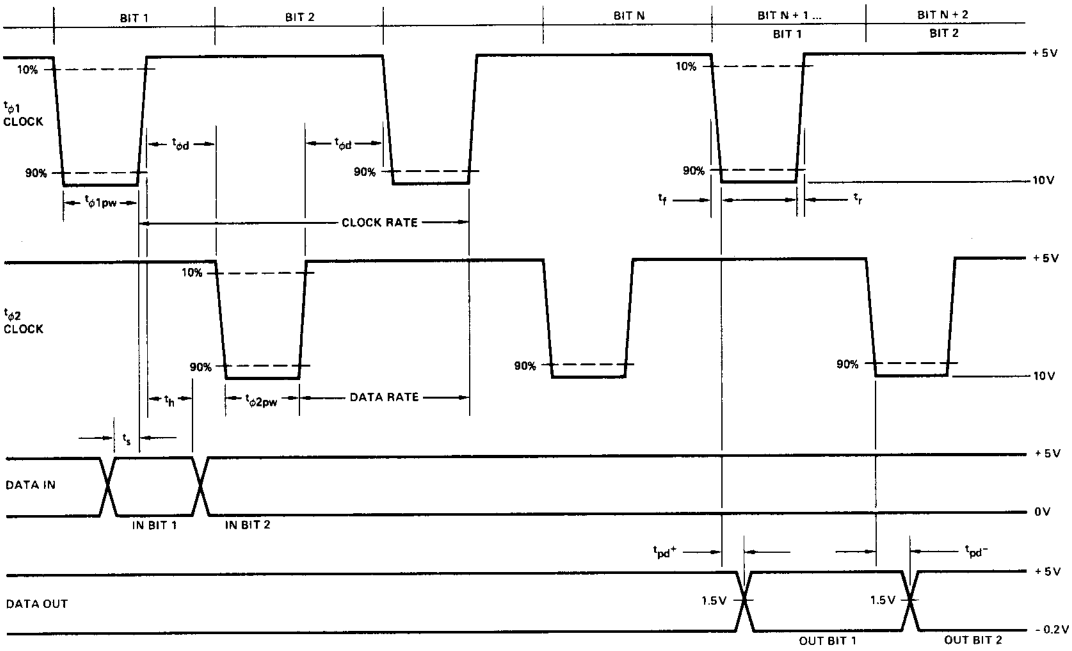
t_s The time required for the input data to be present prior to the LOW to HIGH transition of the clock phase to ensure correct operation.

t_h The time required for the input data to remain present after the LOW to HIGH transition of the clock phase to ensure correct operation.

t_{pd+} The propagation delay from the HIGH to LOW clock phase ϕ_1 transition to the output LOW to HIGH transition.

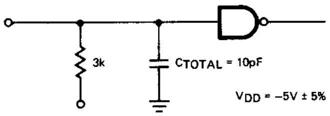
t_{pd-} The propagation delay from the HIGH to LOW clock phase ϕ_2 transition to the output HIGH to LOW transition.

SWITCHING WAVEFORMS

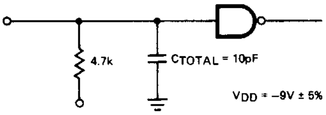


Clock Rise Time 10 ns
Clock Fall Time 10 ns
Output Load 1 TTL Load

Test Load 1



Test Load 2



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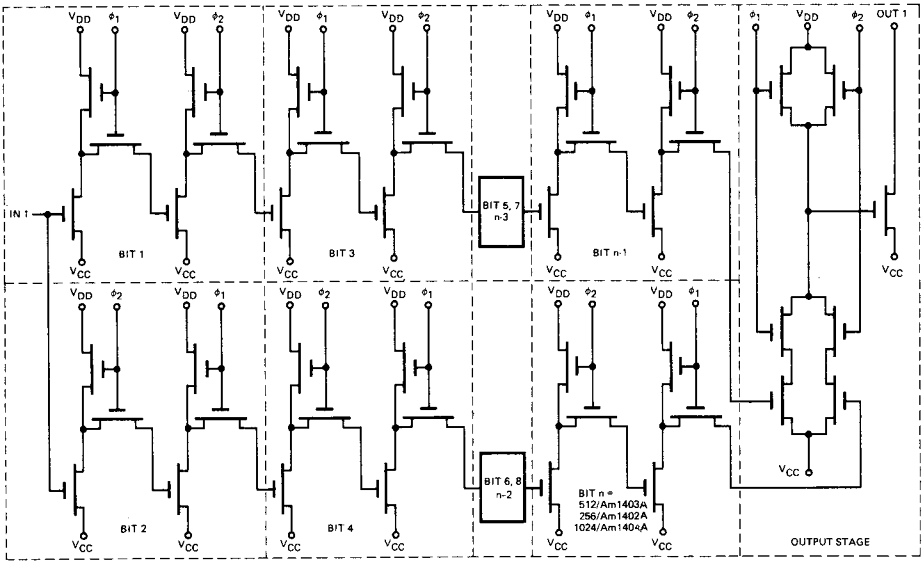
CIRCUIT DIAGRAM



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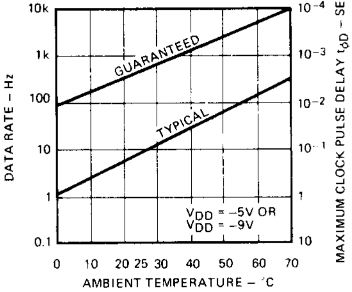
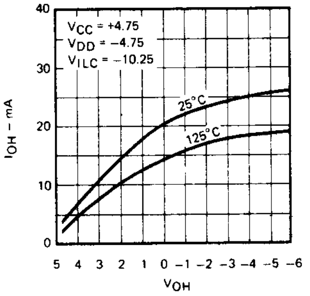
POWER CHARACTERISTICS

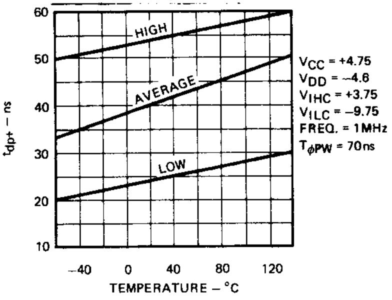
Minimum Operating Data Rate or Maximum Clock Pulse Delay Versus Temperature
(For Small Duty Cycles)



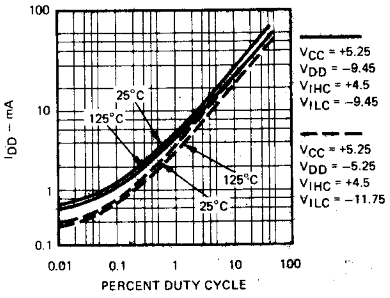
IOH Versus VOH



Typical Range of tpd+ Versus Temperature



IDD Versus Clock Duty Cycle



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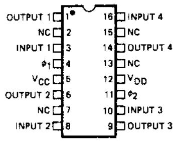
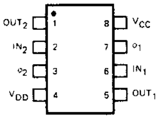
ORDERING INFORMATION

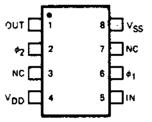
Am2802/Am1402A



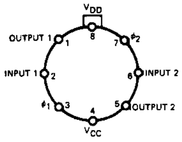
Am2803/Am1403A



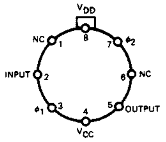
Am2804/Am1404A



Am2803/Am1403A



Am2804/Am1404A



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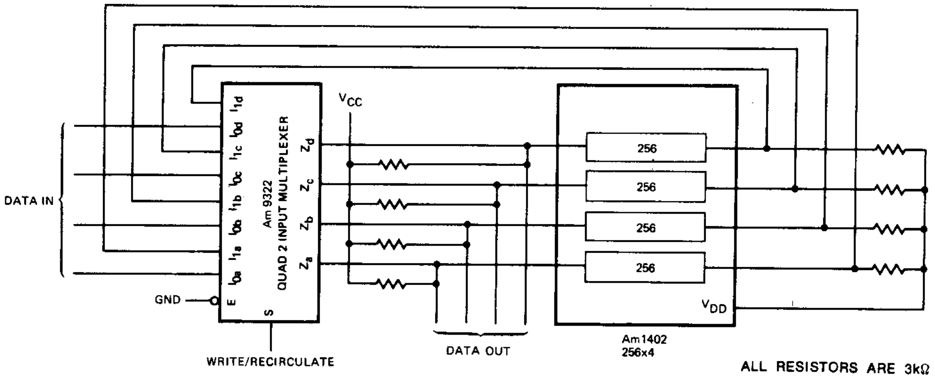
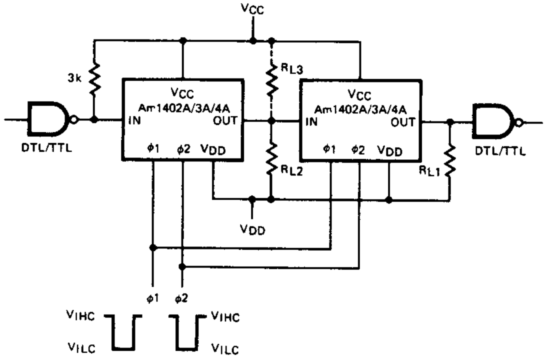
APPLICATIONS

256-Bit Delay

Write Recirculate Logic



DTL/TTL To MOS To DTL/TTL Interface



R_L Load Resistor Values for Different V_{DD} Supplies

	V_{CC} = 5 V V_{DD} = −5 V	V_{CC} = 5 V V_{DD} = −9 V
R_{L1}	3.0 k	4.7 k
R_{L2}	4.7 k	6.2 k
R_{L3}	Not required	3.9 k

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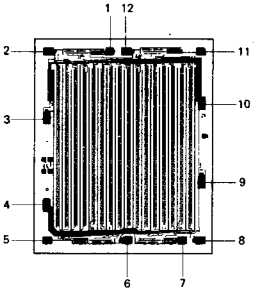
PAD	1402A/2802 PIN	1402A/2802 SIGNAL	1403A/2803 PIN	1403A/2803 SIGNAL	1404A/2804 PIN	1404A/2804 SIGNAL
1	1	OUT 1				
2	3	IN 1	2	IN 1	2	IN
3	4	φ 1	3	φ 1	3	φ 1
4	5	V_{CC}	4	V_{CC}	4	V_{CC}
5	6	OUT 2	5	OUT 2	5	OUT
6	8	IN 2				
7	9	OUT 3				
8	10	IN 3	6	IN 2	7	φ 2
9	11	φ 2	7	φ 2		
10	12	V_{DD}	8	V_{DD}		
11	14	OUT 4	1	OUT 1	8	V_{DD}
12	16	IN 4				

Metallization and Pad Layout



DIE SIZE .109" X .131"