
HD74CDC587

3.3-V Phase-lock Loop Clock Driver with 3-state Outputs

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Description

The HD74CDC587 is a high-performance, low-skew, low-jitter, phase-locked loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the clock output signals to the clock input (CLKIN) signal. The HD74CDC587 operates at 3.3-V V_{CC} and provides LVTTTL- or SSTL_3- compatible inputs and outputs. The HD74CDC587 operates at frequencies from 50 MHz up to 150 MHz, and is ideally suited for high speed microprocessor and synchronous DRAM applications.

A dedicated feedback output (FBOUT) is used to synchronize the output clocks in frequency and phase to the CLKIN reference. Four banks of four outputs (1Yn, 2Yn, 3Yn, 4Yn) are configured to operate at the same frequency ($1\times$) as the CLKIN. For proper operation, all SELn ($n = 0, 1, 2, 3$) inputs must be externally tied to logic low.

The output enable (\overline{OE}) input provides control for the Y output banks. When \overline{OE} is high, the outputs are in a high impedance state. When \overline{OE} is low, the outputs switch at ($1\times$) the CLKIN frequency. In addition, \overline{RESET} provides a master reset for the HD74CDC587 counter circuitry. This allows the outputs to be reset to a known state. TEST provides a bypass of the integrated PLL and divider circuitry. When TEST is high, the input clock bypasses the PLL and is buffered directly to the outputs.

The loop filter components of the PLL are integrated on the HD74CDC587. This reduces the need for external loop components and provides an easily implemented PLL circuit. FBOUT should be connected to the feedback input (FBIN) for normal operation of the PLL.

The voltage-controlled oscillator (VCO) of the integrated PLL has an operating range of 100 MHz to 300 MHz. The VCO is designed to operate at twice ($2\times$) the CLKIN frequency. This allows the HD74CDC587 to achieve output frequencies from 50 MHz to 150 MHz with a duty cycle of 50% $\pm 10\%$ ensured.

Independent analog V_{CC} (AV_{CC}) and ground (AGND) connections are provided for VCO stability.

CLKIN and FBIN can be configured to switch at SSTL_3 input levels by connecting V_{REF} to a nominal reference voltage of 1.5 V. If V_{REF} is strapped to GND, CLKIN and FBIN switch at normal TTL input thresholds.

Because the HD74CDC587 is based on PLL technology, it requires a stabilization time to active phase lock of the FBIN to the reference input clock. This stabilization time is required following power up and application of a fixed-frequency, fixed-phase signal at CLKIN. In addition, a stabilization time may be

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required following changes to the SELn inputs, TEST inputs, or a change in frequency of the CLKIN signal.

Features

- Low output skew and jitter for clock distribution and synchronization
- Internal loop filter eliminates the need for external RC network
- Dedicated external feedback output and input for phase synchronization with the clock input
- Applications for synchronous DRAM, high speed microprocessors, and SSTL_3
- LVTTTL-or SSTL_3-compatible inputs and outputs
- Meets SSTL_3 class 1 and 2 specifications

Function Table ^{*1} (PLL enabled)

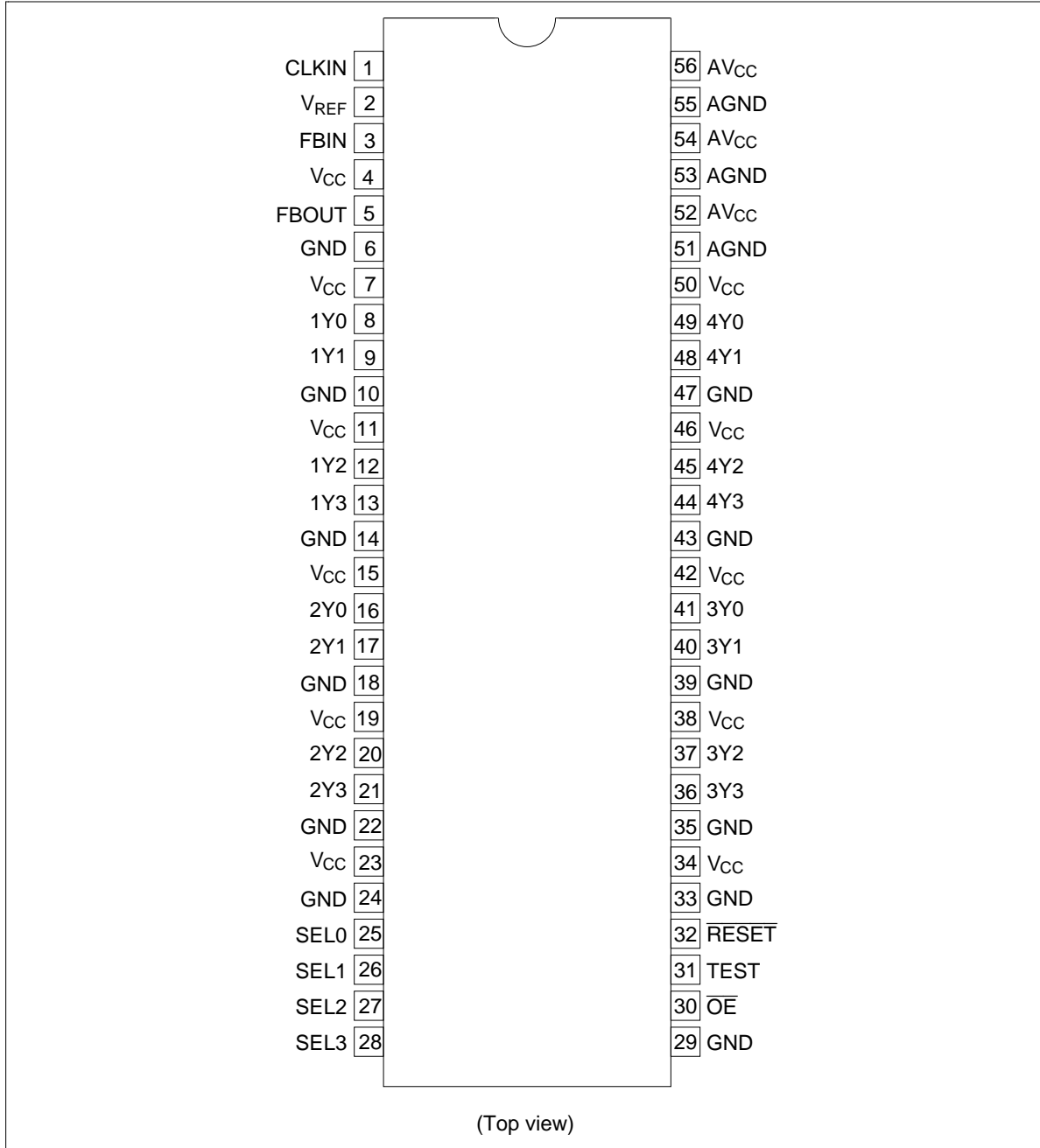
| Inputs ^{*2} | | | Outputs ^{*3} | | | | |
|----------------------|---------------------|---------------------|-----------------------|---------|---------|---------|---------|
| \overline{OE} | F _{IN} min | F _{IN} max | FBOUT | 1Y(0:3) | 2Y(0:3) | 3Y(0:3) | 4Y(0:3) |
| H | 50 MHz | 150 MHz | 1× | Hi Z | Hi Z | Hi Z | Hi Z |
| L | 50 MHz | 150 MHz | 1× | 1× | 1× | 1× | 1× |

H : High level

L : Low level

- Notes:
1. All SELn (n = 0, 1, 2, 3) inputs must be externally tied low for proper operation of the device.
 2. \overline{RESET} should be applied when the input and output frequencies change.
 3. Thermal considerations may need to be observed; depending on V_{CC}, temperature, number of outputs loaded, and loading conditions.

Pin Arrangement



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Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|-----------|----------------------|------------------|------------|
| Supply voltage | V_{CC} | -0.5 to 4.6 | V | |
| Input voltage ¹ | V_I | -0.5 to 7.0 | V | |
| Output voltage ¹ | V_O | -0.5 to $V_{CC}+0.5$ | V | |
| Current into any output in the low state | I_O | 48 | mA | |
| Input clamp current | I_{IK} | -20 | mA | $V_I < 0$ |
| Output clamp current | I_{OK} | -50 | mA | $V_O < 0$ |
| Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) ² | P_T | 1 | W | TSSOP |
| Storage temperature | T_{stg} | -65 to +150 | $^\circ\text{C}$ | |

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

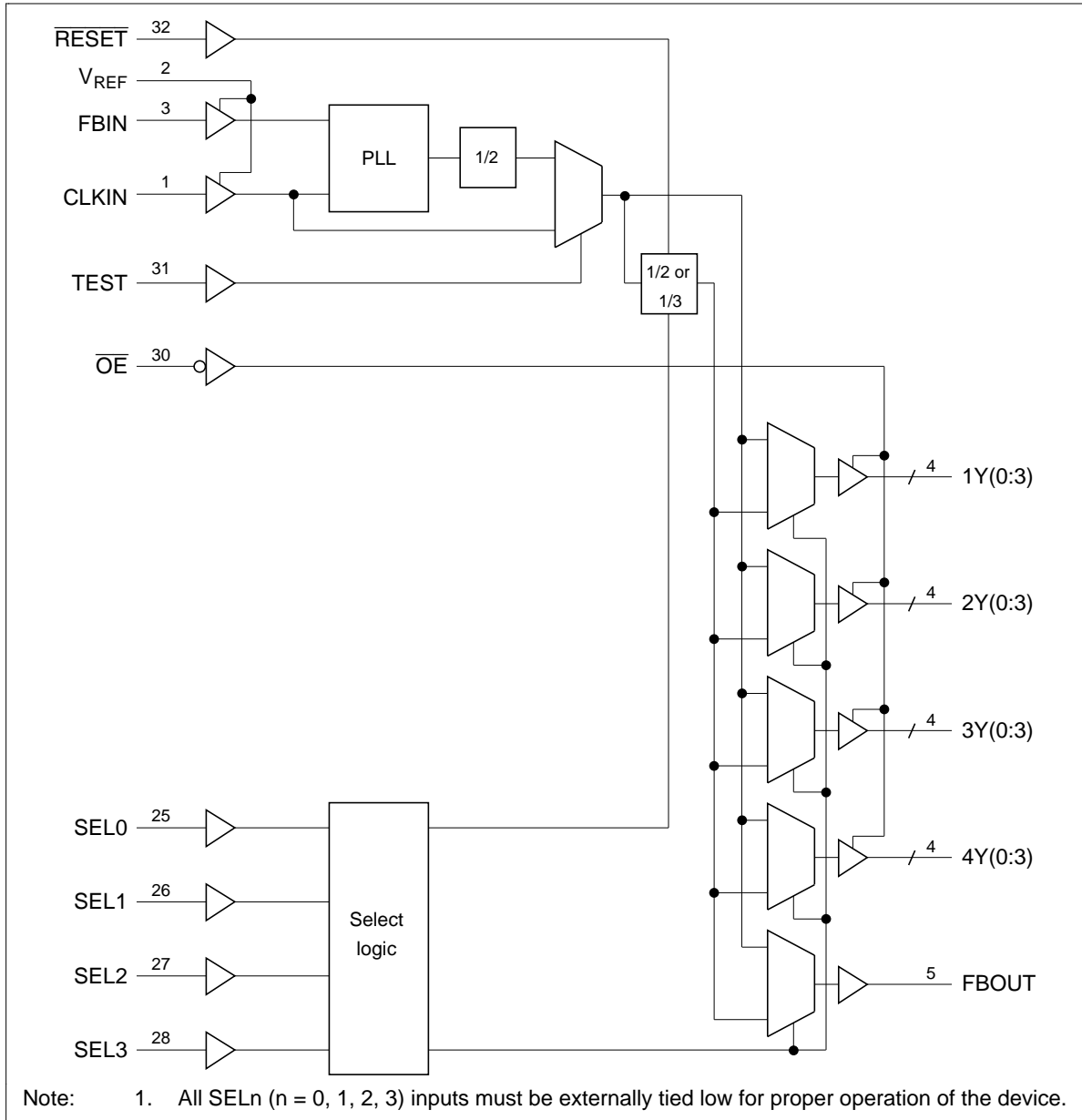
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit | Conditions |
|------------------------|-----------|-----|-----|-----|------------------|------------|
| Supply voltage | V_{CC} | 3.0 | — | 3.6 | V | |
| SSTL reference voltage | V_{REF} | 1.3 | 1.5 | 1.7 | V | |
| Input voltage | V_I | 0 | — | 5.5 | V | |
| Output current | I_{OH} | — | — | -20 | mA | |
| | I_{OL} | — | — | 20 | | |
| Operating temperature | T_a | 0 | — | 70 | $^\circ\text{C}$ | |

Note: Unused inputs must be held high or low to prevent them from floating.

Logic Diagram



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Pin Functions

| Pin name | No. | I/O | Description |
|--|--|-----|---|
| CLKIN | 1 | I | Clock input. CLKIN provides the clock signal to be distributed by the HD74CDC587 clock driver circuit. CLKIN is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLKIN must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLKIN signal is applied, a stabilization time is required for the PLL to obtain phase-lock of its feedback signal to its reference signal. |
| FBIN | 3 | I | Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN should be wired to FBOUT. The integrated PLL adjusts the output clocks to obtain zero phase delay between FBIN and CLKIN. |
| V _{REF} | 2 | I | Voltage reference. V _{REF} is the reference voltage required for SSTL operation. A nominal voltage of 1.5 V should be applied when SSTL operation of CLKIN and FBIN is required. If V _{REF} is strapped to GND, CLKIN and FBIN operate at TTL switching levels. |
| \overline{OE} | 30 | I | Output enable. \overline{OE} is the output enable for all of the Y outputs. When \overline{OE} is low, all Y outputs are enabled. When \overline{OE} is high, all Y outputs are in the high impedance state. FBOUT is not disabled by \overline{OE} ; therefore, the PLL is not disrupted when the Y outputs are placed into the high impedance state. |
| TEST | 31 | I | Test input. TEST is used to bypass the PLL circuitry for factory testing of the device. When TEST is low, all outputs operate using the PLL circuitry. When TEST is high, the device is placed in a test mode that bypasses the PLL circuitry. |
| \overline{RESET} | 32 | I | Reset input. \overline{RESET} is used to reset the counter circuit that divides the VCO output frequency. Y outputs configured as 1× of the input signal may be reset to a known state. \overline{RESET} is a negative edge triggered signal. When a high to low edge occurs at \overline{RESET} , the counter that divides the VCO output signal is asynchronously cleared to a low level. For normal operation, a high level signal should be maintained on the \overline{RESET} input. |
| SEL(0:3) | 28–25 | I | Select input. All SEL(0:3) inputs must be permanently tied to logic low for normal operation. |
| 1Y(0:3) 2Y(0:3) 3Y(0:3) 4Y(0:3) | 8, 9, 12, 13 16, 17, 20, 21 36, 37, 40, 41 44, 45, 48, 49 | O | Clock outputs. All outputs operate at 1× the input clock (CLKIN) frequency. The duty cycle of the Y output signals is nominally 50%, independent of the duty cycle of CLKIN. |
| FBOUT | 5 | O | Feedback output. FBOUT is synchronized in phase and frequency to the input clock. FBOUT is not a 3-state output and is not disabled when \overline{OE} is asserted low. A stabilization time is required on power up and the application of a fixed frequency, fixed-phase signal at CLKIN. In addition, a stabilization time may be required after changes are made to the SEL(0:3) inputs, the TEST input, or changes to the input frequency at CLKIN. |

Electrical Characteristics (Ta = 25°C)

| Item | Symbol | Min | Typ ¹ | Max | Unit | Test Conditions |
|-------------------------------------|-----------------|-------------------------|------------------|-------------------------|------|--|
| Input clamp voltage | V _{IK} | — | — | -1.2 | V | V _{CC} = 3 V, I _I = -18 mA |
| Input voltage | V _{IH} | V _{REF} +200mV | — | — | V | CLK, FBIN |
| | | 2.0 | — | — | | CLK, FBIN (V _{REF} = GND) |
| | | 2.0 | — | — | | Other inputs |
| | V _{IL} | — | — | V _{REF} -200mV | | CLK, FBIN |
| | | — | — | 0.8 | | CLK, FBIN (V _{REF} = GND) |
| | | — | — | 0.8 | | Other inputs |
| Output voltage | V _{OH} | V _{CC} -0.2 | — | — | V | V _{CC} = Min to Max ² , I _{OH} = -100 μA |
| | | 2.2 | — | — | | V _{CC} = 3 V, I _{OH} = -16 mA |
| | | 2.1 | — | — | | V _{CC} = 3 V, I _{OH} = -20 mA |
| | V _{OL} | — | — | 0.2 | | V _{CC} = 3 V, I _{OL} = 100 μA |
| | | — | — | 0.5 | | V _{CC} = 3 V, I _{OL} = 16 mA |
| | | — | — | 0.6 | | V _{CC} = 3 V, I _{OL} = 20 mA |
| Input current | I _{IN} | — | — | ±10 | μA | V _{CC} = 0 or Max ² , V _I = 3.6 V, V _{REF} = GND |
| | | — | — | ±1 | | V _{CC} = 3.6 V, V _I = V _{CC} or GND, V _{REF} = GND |
| | | — | — | ±1 | | V _{CC} = 3.6 V, V _I = 2.1 V or 0.9 V, V _{REF} = 1.5 V |
| High impedance state output current | I _{OZ} | — | — | 10 | μA | V _{CC} = 3.6 V, V _O = 3 V |
| | | — | — | -10 | | V _{CC} = 3.6 V, V _O = 0 |
| Supply current | I _{CC} | — | — | 1 | mA | V _{CC} = 3.6 V, I _O = 0, TEST = 3.6 V, V _I = V _{CC} or GND, V _{REF} = GND |
| | | — | — | 6 | | V _{CC} = 3.6 V, I _O = 0, TEST = 3.6 V, V _I = 2.1 V or 0.9 V, V _{REF} = 1.5 V |
| Input capacitance | C _{IN} | — | 4 | — | pF | V _I = V _{CC} or GND, V _{REF} = GND |
| | | — | 4 | — | | V _I = 2.1 V or 0.9 V, V _{REF} = 1.5 V |
| Output capacitance | C _O | — | 8 | — | pF | V _O = 3 V or 0, V _{REF} = GND |
| | | — | 8 | — | | V _O = 2.1 V or 0.9 V, V _{REF} = 1.5 V |

Notes: 1. All typical values are at V_{CC} = 3.3 V.

2. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

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Switching Characteristics

LVTTL ($V_{REF} = GND$, $C_L = 30$ pF)

| Item | Symbol | Min | Typ | Max | Unit | From (Input) | To (Output) |
|--------------------------|-----------|------|-----|------|------|--------------|-------------|
| Maximum clock frequency | f_{max} | 150 | — | — | MHz | | |
| Phase error time | t_{pe} | -225 | — | +225 | ps | CLKIN↑ | FBIN↑ |
| Between output pins skew | t_{sk} | — | — | 300 | ps | | FBOUT / Y |
| Jitter | | -100 | — | +100 | ps | CLKIN↑ | Y↑ |
| Duty cycle | | 40 | — | 60 | % | | Y |
| Output rise / fall time | t_{TLH} | — | — | 2 | ns | | FBOUT / Y |
| | t_{THL} | — | — | 2 | | | FBOUT / Y |

Note: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

SSTL_3 ($V_{REF} = V_{TT} = 1.5$ V, $C_L = 30$ pF)

| Item | Symbol | Min | Typ | Max | Unit | From (Input) | To (Output) |
|--------------------------|-----------|------|-----|------|------|--------------|-------------|
| Maximum clock frequency | f_{max} | 150 | — | — | MHz | | |
| Phase error time | t_{pe} | -300 | — | +300 | ps | CLKIN↑ | FBIN↑ |
| Between output pins skew | t_{sk} | — | — | 300 | ps | | FBOUT / Y |
| Jitter | | -75 | — | +75 | ps | CLKIN↑ | Y↑ |
| Duty cycle | | 40 | — | 60 | % | | Y |
| Output rise / fall time | t_{TLH} | — | — | 1 | ns | | FBOUT / Y |
| | t_{THL} | — | — | 1 | | | FBOUT / Y |

Note: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

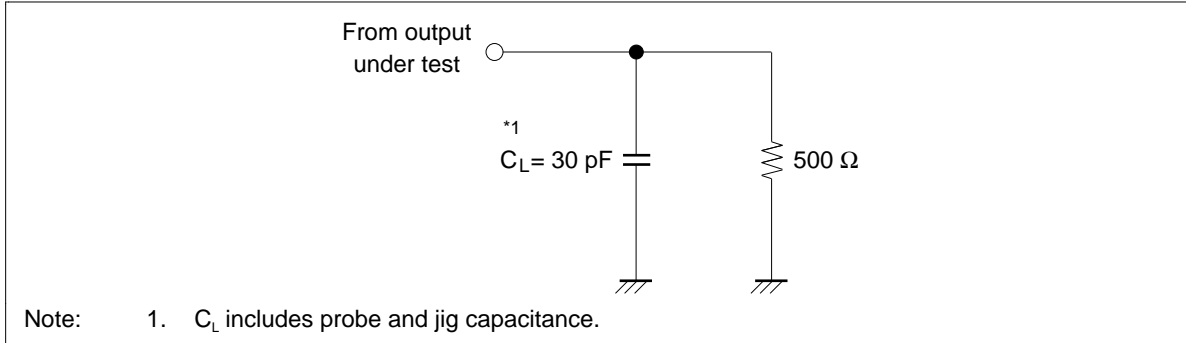
Timing requirements

| Item | Symbol | Min | Max | Unit | Test Conditions |
|---------------------------------|--------------------|------------|------------|-------------|---|
| Input clock frequency | f_{clock} | 50 | 150 | MHz | |
| Input clock duty cycle | | 40 | 60 | % | |
| Stabilization time ¹ | | — | 5 | ms | $\overline{\text{OE}}$ (negative edge) or $\overline{\text{RESET}}$ (positive edge) |
| | | — | 5 | | After power up and CLKIN |

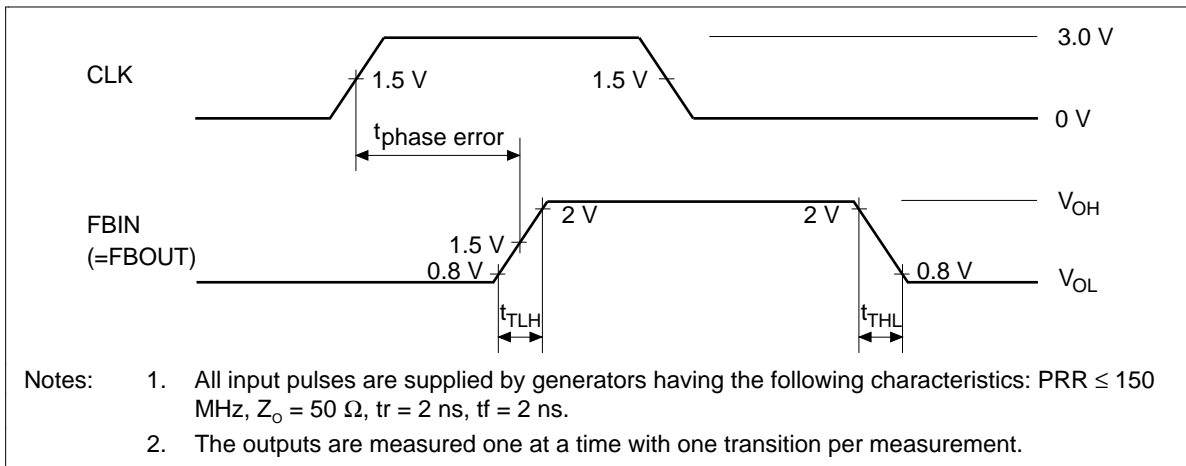
Note: 1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLKIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

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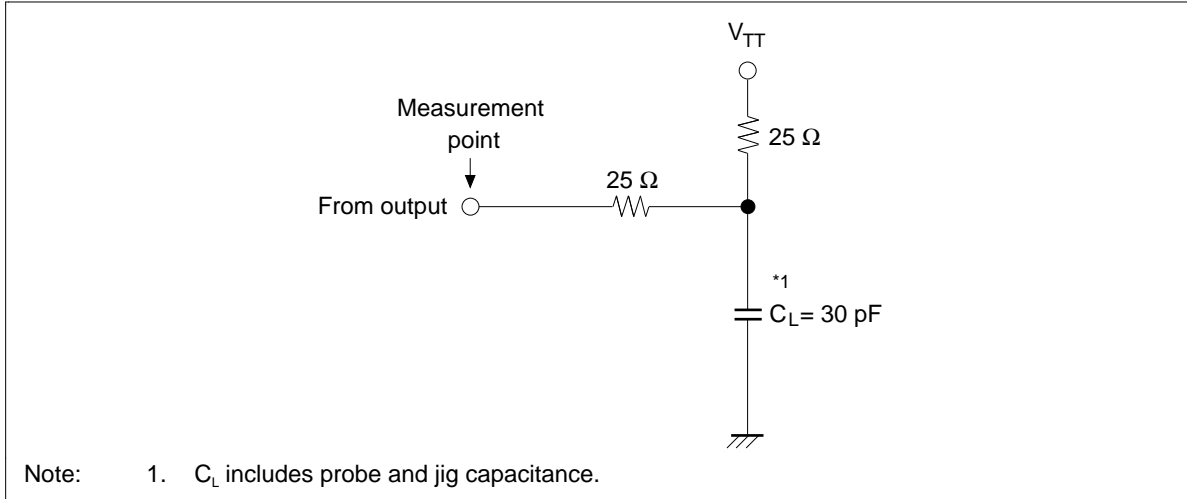
Test Circuit (LVTTTL)



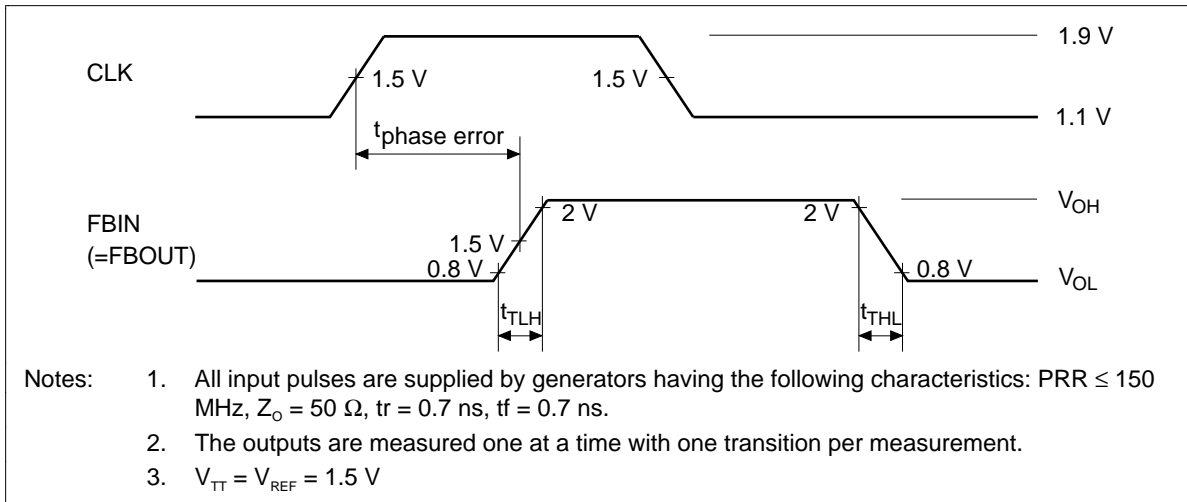
Waveforms



Test Circuit (SSTL_3)



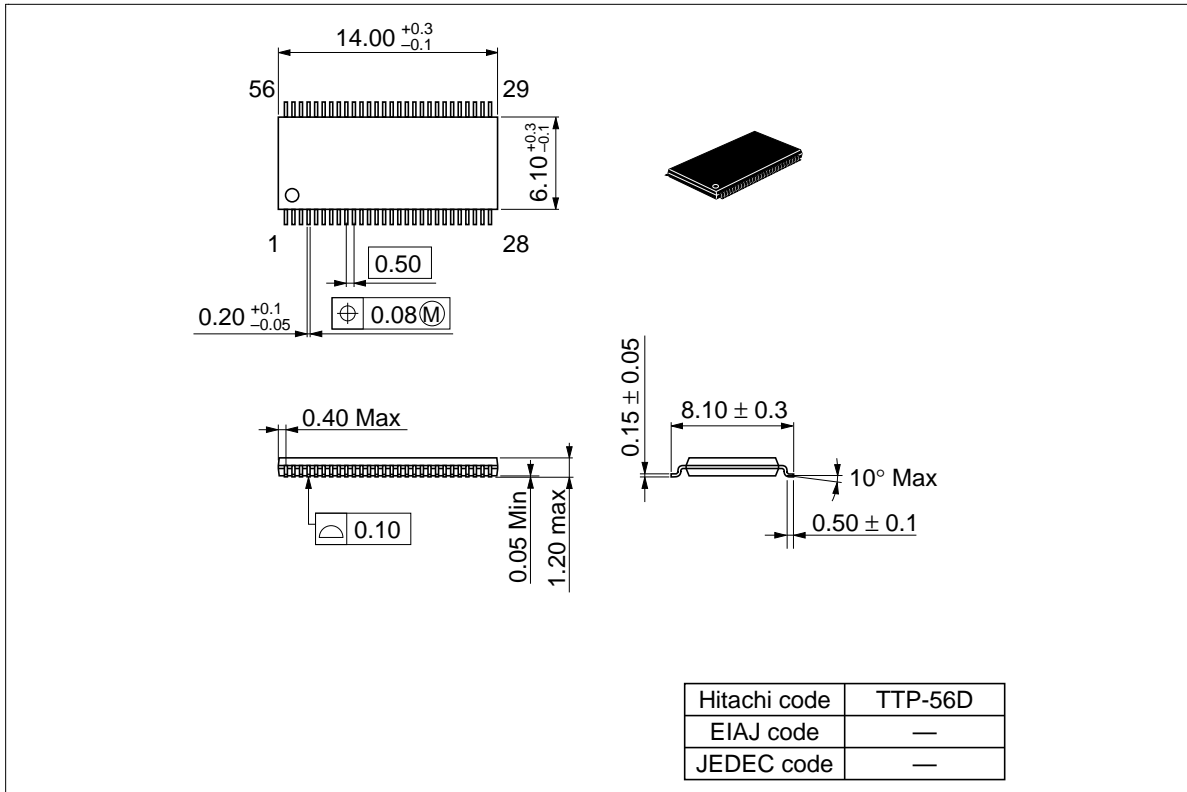
Waveforms



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Package Dimensions

Unit : mm



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