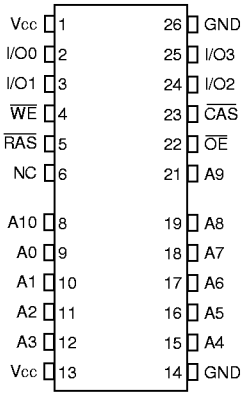
4Mx4 CMOS EDO Dynamic RAM 3.3V *PRELIMINARY**

PIN CONFIGURATION

300 MIL SOJ
TOP VIEW



PIN DESCRIPTION

A0-10	Address Inputs
I/O0-3	Data Input/Outputs
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
VCC	Power Supply
GND	Ground
NC	Not Connected

PLASTIC PLUS™ FEATURES

- Fast Access Time (t_{RAC}): 60, 70ns
- Power Supply: 3.3V ±0.3V
- Packaging
  - 24/26 Plastic SOJ (MJ)
- Industrial and Military Temperature Ranges
- 5V Tolerant Inputs and I/Os
- Three-State Data Output
- Extended Data Out (EDO) Page Mode Access Cycle.
- TTL-Compatible Inputs and Outputs
- $\overline{RAS}$-Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2K Cycle Refresh = 32ms
- Low Active Power Dissipation
- Low Standby Power Dissipation

* *This data sheet describes a product under development, not fully characterized, and is subject to change without notice.*

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T_A	-55	+125	°C
Storage Temperature	T_{STG}	-55	+150	°C
Short Circuit Output Current	Ios		50	mA
Power Dissipation	P_T		1	W
Supply Voltage Range*	V_{CC}	-1.0	5.5	V
Voltage Range on any Pin*	V_T	-1.0	5.5	V

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposed to absolute-maximum-rated conditions for extended periods may affect device reliability.

* All voltage values are with respect to GND.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{CC}	3.0	3.6	V
Input High Voltage	V_{IH}	2.0	Vcc + 1.0	V
Input Low Voltage*	V_{IL}	-0.5	+0.8	V
Operating Temp. (Mil.)	T_A	-55	+125	°C
Operating Temp. (Ind.)	T_A	-40	+85	°C

* The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

CAPACITANCE

(T_A = 25°C)

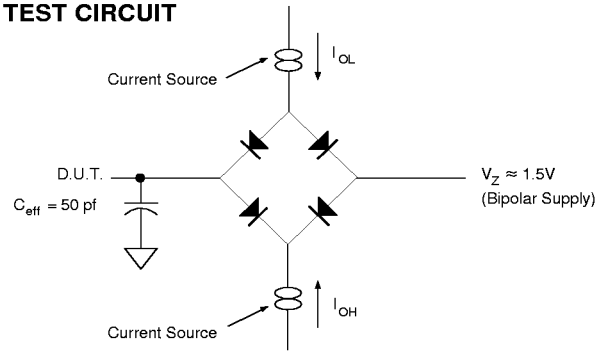
Parameter	Symbol	Max	Unit
Address Input Capacitance	$C_{I(A)}$	5	pF
$\overline{RAS}$ and $\overline{CAS}$ Input Capacitance	$C_{I(RC)}$	7	pF
$\overline{OE}$ Input Capacitance	$C_{I(OE)}$	7	pF
$\overline{WE}$ Input Capacitance	$C_{I(WE)}$	7	pF
I/O Capacitance	C_{IO}	7	pF

This parameter is guaranteed by design but not tested.

TRUTH TABLE

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Address		Data In/Out
						t_R	t_C	I/O_{1-4}
Standby		H	H→X	X	X	X	X	High-Z
Read		L	L	H	L	ROW	COL	Data-Out
Early Write		L	L	L	X	ROW	COL	Data-In
Read Write		L	L	H→L	L→H	ROW	COL	Data-Out, Data-In
EDO-Page-Mode Read	1st cycle	L	H→L	H	L	ROW	COL	Data-Out
	2nd cycle	L	H→L	H	L	n/a	COL	Data-Out
EDO-Page-Mode Early-Write	1st cycle	L	H→L	L	X	ROW	COL	Data-In
	2nd cycle	L	H→L	L	X	n/a	COL	Data-In
	Any cycle	L	L→H	L	X	n/a	COL	Data-Out
EDO-Page-Mode Read-Write	1st cycle	L	H→L	H→L	L→H	ROW	COL	Data-Out, Data-In
	2nd cycle	L	H→L	H→L	L→H	n/a	COL	Data-Out, Data-In
$\overline{RAS}$-Only Refresh		L	H	X	X	ROW	n/a	High-Z
Hidden Refresh (Read)		L→H→L	L	H	L	ROW	COL	Data-Out
Hidden Refresh (Write)		L→H→L	L	L	X	ROW	COL	Data-In
CBR Refresh		H→L	L	H	X	X	X	High-Z
Self Refresh		H→L	L	H	X	X	X	High-Z

AC TEST CIRCUIT



AC TEST CONDITIONS

Parameter	Typ	Unit
Input Pulse Levels	V_{IL} = 0, V_{IH} = 3.0	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:
V_Z is programmable from -2V to +7V.
I_{OL} & I_{OH} programmable from 0 to 16mA.
Tester Impedance Z_0 = 75 Ω.
V_Z is typically the midpoint of V_{OH} and V_{OL}.
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
ATE tester includes jig capacitance.

DC CHARACTERISTICS

(V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Test Condition	Symbol	Min	Max	Units
High Level Output Voltage	I_{OH} = -2.0mA	V_{OH}	2.4		V
Low Level Output Voltage	I_{OL} = 2.0mA	V_{OL}		0.4	V
Input Current (Leakage)	V_I = 0V to +5.5V All others = 0V	I_I	-2	2	µA
Output current (Leakage)	VO = 0V to Vcc, CAS high	I_O	-10	10	µA
Average Read or Write Cycle Current	minimum cycle	I_{CC1}		110	mA
Standby Current	TTL, $\overline{RAS}$ and $\overline{CAS}$ high	I_{CC2}		2	mA
	CMOS, $\overline{RAS}$ and $\overline{CAS}$ high	I_{CC2}		1	mA
Average EDO Page Current	$\overline{RAS}$ low, $\overline{CAS}$ cycling	I_{CC4}		100	mA

AC CHARACTERISTICS

(Notes: 1, 2, 4-7, 12) (V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-60		-70		Units
		Min	Max	Min	Max	
Column Address Access Time	t_{AA}		30		35	ns
Column Address Setup to $\overline{CAS}$ Precharge	t_{ACH}	15		15		ns
Column Address Hold Time (Reference to $\overline{RAS}$)	t_{AR}	45		55		ns
Column Address Setup Time	t_{ASC}	0		0		ns
Row Address Setup Time	t_{ASR}	0		0		ns
Column Address to $\overline{WE}$ Delay Time (8)	t_{AWD}	49		65		ns
Access Time from $\overline{CAS}$ (9)	t_{CAC}		15		20	ns
Column Address Hold Time	t_{CAH}	10		15		ns
$\overline{CAS}$ Pulse Width	t_{CAS}	10	10,000	15	10,000	ns
$\overline{CAS}$ Hold Time (CBR Refresh) (3)	t_{CHR}	10		15		ns
$\overline{CAS}$ to Output in Low-Z	t_{CLZ}	0		0		ns
Data Output hold after next $\overline{CAS}$ Low	t_{COH}	3		5		ns
$\overline{CAS}$ Precharge Time (10)	t_{CP}	10		10		ns
Access Time from $\overline{CAS}$ Precharge	t_{CPA}		35		40	ns
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	5		5		ns
$\overline{CAS}$ Hold Time	t_{CSH}	45		55		ns
$\overline{CAS}$ Setup Time (CBR Refresh)	t_{CSR}	5		5		ns
$\overline{CAS}$ to $\overline{WE}$ Delay Time (8)	t_{CWD}	35		40		ns
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	10		15		ns
Data-In Hold Time (11)	t_{DH}	10		12		ns
Data-In Setup Time (11)	t_{DS}	0		0		ns
Output Disable	t_{OD}	0	15	0	15	ns
Output Enable (12)	t_{OE}		15		20	ns
$\overline{OE}$ Hold Time from $\overline{WE}$ during Read-Modify-Write Cycle (13)	t_{OEH}	10		12		ns
$\overline{OE}$ High hold from $\overline{CAS}$ High (13)	t_{OEHC}	10		10		ns
$\overline{OE}$ High Pulse Width	t_{OEP}	5		10		ns
$\overline{OE}$ Low to $\overline{CAS}$ High Setup Time	t_{OES}	5		5		ns
Output Buffer Turn-Off Delay (15)	t_{OFF}	0	15	0	15	ns

NOTES: See full list on page 5.

AC CHARACTERISTICS

(Notes: 1, 2, 4-7, 12) (V_{CC} = 3.3V, GND = 0V, T_A = -55°C to +125°C)

Parameter	Symbol	-60		-70		Units
		Min	Max	Min	Max	
$\overline{OE}$ Setup Prior to $\overline{RAS}$ during Hidden Refresh Cycle	t_{ORD}	0		0		ns
EDO-Page-Mode Read or Write Cycle Time	t_{PC}	25		35		ns
EDO-Page-Mode Read-Write Cycle Time	t_{PRWC}	56		85		ns
Access Time from $\overline{RAS}$ (16)	t_{RAC}		60		70	ns
$\overline{RAS}$ to Column Address Delay Time (16)	t_{RAD}	12		15		ns
Row Address Hold Time	t_{RAH}	10		10		ns
$\overline{RAS}$ Pulse Width	t_{RAS}	60	10,000	70	10,000	ns
$\overline{RAS}$ Pulse Width (EDO Page Mode)	t_{RASP}	60	125,000	70	125,000	ns
Random Read or Write Cycle Time	t_{RC}	104		130		ns
$\overline{RAS}$ to $\overline{CAS}$ Delay Time (17)	t_{RCD}	14	50	16	50	ns
Read Command Hold Time (referenced to $\overline{CAS}$) (18)	t_{RCH}	0		0		ns
Read Command Setup Time	t_{RCS}	0		0		ns
Refresh Period (2,048 cycles)	t_{REF}		32		32	ms
$\overline{RAS}$ Precharge Time	t_{RP}	40		50		ns
$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	t_{RPC}	5		5		ns
Read Command Hold Time (referenced to $\overline{RAS}$) (18)	t_{RRH}	0		0		ns
$\overline{RAS}$ Hold Time	t_{RSH}	15		15		ns
Read Write Cycle Time	t_{RWC}	140		180		ns
$\overline{RAS}$ to $\overline{WE}$ Delay Time (8)	t_{RWD}	79		90		ns
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	15		15		ns
Transition Time (rise or fall)	t_T	2	50	2	50	ns
Write Command Hold Time	t_{WCH}	10		12		ns
Write Command Hold Time (referenced to $\overline{RAS}$)	t_{WCR}	45		56		ns
$\overline{WE}$ Command Setup Time (8)	t_{WCS}	0		0		ns
Output Disable Delay from $\overline{WE}$	t_{WHZ}	0	15	0	16	ns
Write Command Pulse Width	t_{WP}	5		12		ns
$\overline{WE}$ Pulse to Disable at $\overline{CAS}$ High	t_{WPZ}	10		12		ns
$\overline{WE}$ Hold Time (CBR Refresh)	t_{WRH}	10		10		ns
$\overline{WE}$ Hold Time (CBR Refresh)	t_{WRP}	10		10		ns

NOTES: See full list on next page.

NOTES:

1. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range is ensured.
2. An initial pause of 100µs is required after power-up, followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-only or CBR with $\overline{WE}$ High), before proper device operation is ensured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the t_{REF} refresh requirement is exceeded.
3. Enables on-chip refresh and address counters.
4. AC characteristics assume t_T = 2.5ns.
5. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
6. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
7. Measured with a load equivalent to two TTL gates and 100pF; and V_{OL} = 0.8V and V_{OH} = 2V.
8. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to Early Write cycles. t_{RWD}, t_{AWD} and t_{CWD} apply to Read-Modify-Write cycles. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an Early Write cycle and the data output will remain an open circuit throughout the entire cycle. *If $t_{WCS} < t_{WCS}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CWD} \geq t_{CWD}$ (min), the cycle is a Read-Modify-Write and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data-out is indeterminate. $\overline{OE}$ held High and $\overline{WE}$ taken Low after $\overline{CAS}$ goes Low results in a Late Write ($\overline{OE}$-controlled) cycle. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not applicable in a Late Write cycle.
9. Requires that t_{AA} and t_{RAC} are not violated.
10. If $\overline{CAS}$ is Low at the falling edge of $\overline{RAS}$, O will be maintained from the previous cycle. To initiate a new cycle and clear the data-out buffer, $\overline{CAS}$ must be pulsed High for t_{CP}.
11. These parameters are referenced to $\overline{CAS}$ leading edge in Early Write cycles and $\overline{WE}$ leading edge in Late Write or Read-Modify-Write cycles.
12. If $\overline{OE}$ is tied permanently Low, Late Write or Read-Modify-Write operations are not permissible and should not be attempted. Additionally, $\overline{WE}$ must be pulsed during $\overline{CAS}$ High time in order to place I/O buffers in High-Z.
13. Late Write and Read-Modify-Write cycle must have both t_{OD} and t_{OEH} met ($\overline{OE}$ High during Write cycle) in order to ensure that the output buffers will be open during the Write cycle. The I/Os will provide the previously read data if $\overline{CAS}$ remains Low and $\overline{OE}$ is taken back Low after t_{OEH} is met. If $\overline{CAS}$ goes High prior to $\overline{OE}$ going back Low, thel/Os will remain open.
14. Requires that t_{AA} and t_{CAC} are not violated.
15. t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}. It is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.
16. The t_{RAD} (max) limit is no longer specified. t_{RAD} (max) was specified as a reference point only. If t_{RAD} was greater than the specified t_{RAD} (max) limit, then access time was controlled exclusively by t_{AA} (t_{RAC} and t_{CAC} no longer applied). With or without the t_{RAD} (max) limit, t_{AA} and t_{CAC} must always be met.
17. The t_{RCD} (max) limit is no longer specified. t_{RCD} (max) was specified as a reference point only. If t_{RCD} was greater than the specified t_{RCD} (max) limit, then access time was controlled exclusively by t_{CAC} (t_{RAC} (min) no longer applied). With or without the t_{RCD} limit, t_{AA}, t_{RAC} and t_{CAC} must always be met.
18. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.

GENERAL DESCRIPTION

The WPDE4M4V-XMJX is a randomly accessed, solid-state memory containing 16,777,216 bits organized in a x4 configuration. $\overline{RAS}$ is used to latch the row address. Once the page has been opened by $\overline{RAS}$, $\overline{CAS}$ is used to latch the column address. Read and Write cycles are selected with the $\overline{WE}$ input.

A logic High on $\overline{WE}$ dictates Read mode, while a logic Low on $\overline{WE}$ dictates Write mode. During a Write cycle, data-in (I) is latched by the falling edge of $\overline{WE}$ or $\overline{CAS}$, whichever occurs last. An Early Write occurs when $\overline{WE}$ is taken Low prior to $\overline{CAS}$ falling. A Late Write or Read-Modify-Write occurs when $\overline{WE}$ falls after $\overline{CAS}$ is taken Low. During Early Write cycles, the data outputs (O) will remain High-Z regardless of the state of $\overline{OE}$. During Late Write or Read-Modify-Write cycles, $\overline{OE}$ must be taken High to disable the data outputs prior to applying input data. If a Late Write or Read-Modify-Write is attempted while keeping $\overline{OE}$ Low, no write will occur, and the data outputs will drive read data from the accessed location.

The four data inputs and the four data outputs are routed through four pins using common I/O, and pin direction is controlled by $\overline{WE}$ and $\overline{OE}$.

PAGE ACCESS

Page operations allow faster data operations (Read, Write or Read-Modify-Write) within a row address defined page boundary. The Page cycle is always initiated with a row address strobed-in by $\overline{RAS}$, followed by a column address strobed-in by $\overline{CAS}$. $\overline{CAS}$ may be toggled-in by holding $\overline{RAS}$ Low and strobing-in different column addresses, thus executing faster memory cycles. Returning $\overline{RAS}$ High terminates the Page Mode of operation.

EDO PAGE MODE

The 4M x 4 EDO DRAM provides EDO Page Mode, which is an accelerated Fast Page Mode cycle. The primary advantage of EDO is the availability of data-out even after $\overline{CAS}$ returns High. EDO allows $\overline{CAS}$ precharge time (t_{CP}) to occur without the output data going invalid. This elimination of $\overline{CAS}$ output control allows pipeline Reads.

Fast Page Mode DRAMs have traditionally turned the output buffers off (High-Z) with the rising edge of $\overline{CAS}$. EDO Page Mode DRAMs operate like Fast Page Mode DRAMs, except data will remain valid or become valid after $\overline{CAS}$ goes High during Reads, provided $\overline{RAS}$ and $\overline{OE}$ are held Low. If $\overline{OE}$ is pulsed while $\overline{RAS}$ and $\overline{CAS}$ are Low, data will toggle from valid data to High-Z and back to the same valid data. If $\overline{OE}$ is toggled or pulsed after $\overline{CAS}$ goes High while $\overline{RAS}$ remains Low, data will transition to and remain High-Z. $\overline{WE}$ can also perform the function of disabling the output devices under certain conditions.

During an application, if the I/O outputs are wire OR'd $\overline{OE}$ must be used to disable idle banks of DRAMs. Alternatively, pulsing $\overline{WE}$ to the idle banks during $\overline{CAS}$ high time will also High-Z the outputs. Independent of $\overline{OE}$ control, the outputs will disable after t_{OFF}, which is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, whichever occurs last.

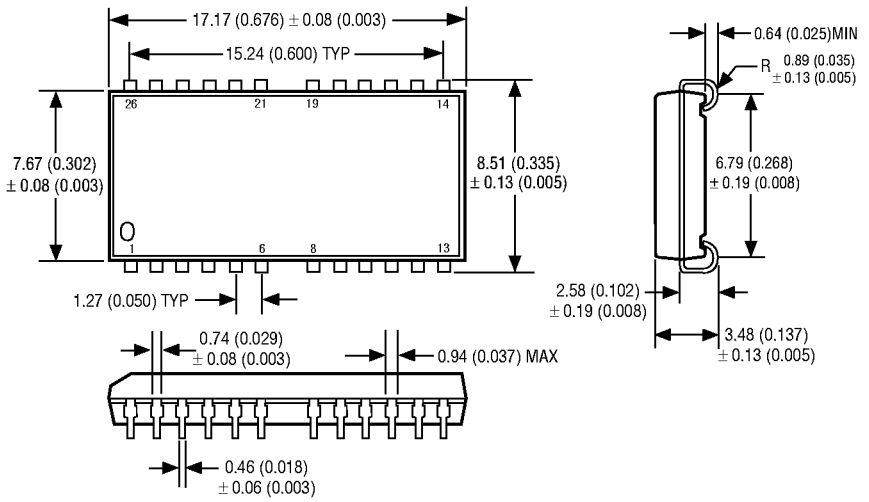
REFRESH

Preserve correct memory cell data by maintaining power and executing any $\overline{RAS}$ cycle (Read, Write) or $\overline{RAS}$ refresh cycle ($\overline{RAS}$-only, CBR or Hidden) so that all 2,048 combinations of $\overline{RAS}$ addresses are executed within t_{REF} (max), regardless of sequence. The CBR cycle will invoke the internal refresh counter for automatic $\overline{RAS}$ addressing.

STANDBY

Returning $\overline{RAS}$ and $\overline{CAS}$ High terminates a memory cycle and decreases chip current to a reduced standby level. The chip is preconditioned for the next cycle during the $\overline{RAS}$ High time.

PACKAGE DIMENSION: 24/26 PIN, 300 MIL PLASTIC SOJ



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

W P D E 4M 4 V X - XX MJ X X

SHIPPING METHODS:
Blank = Rails (PLCC, SOJ, and DIP) or Trays (BGA and TSOP)
R = Tape and Reel

DEVICE GRADE:
M = Military Temperature -55°C to +125°C
I = Industrial Temperature -40°C to +85°C

PACKAGE:
MJ = 24/26 Plastic SOJ (300 mil)

ACCESS TIME (ns)

IMPROVEMENT MARK
B = Burn-in
T = Temperature Cycle
C = Burn-in and Temp Cycle

Low Voltage Supply 3.3V ± 0.3V

ORGANIZATION, 4M x 4

E = Extended Data Out Mode (EDO)

DRAM

PLASTIC PLUS™

WHITE MICROELECTRONICS