



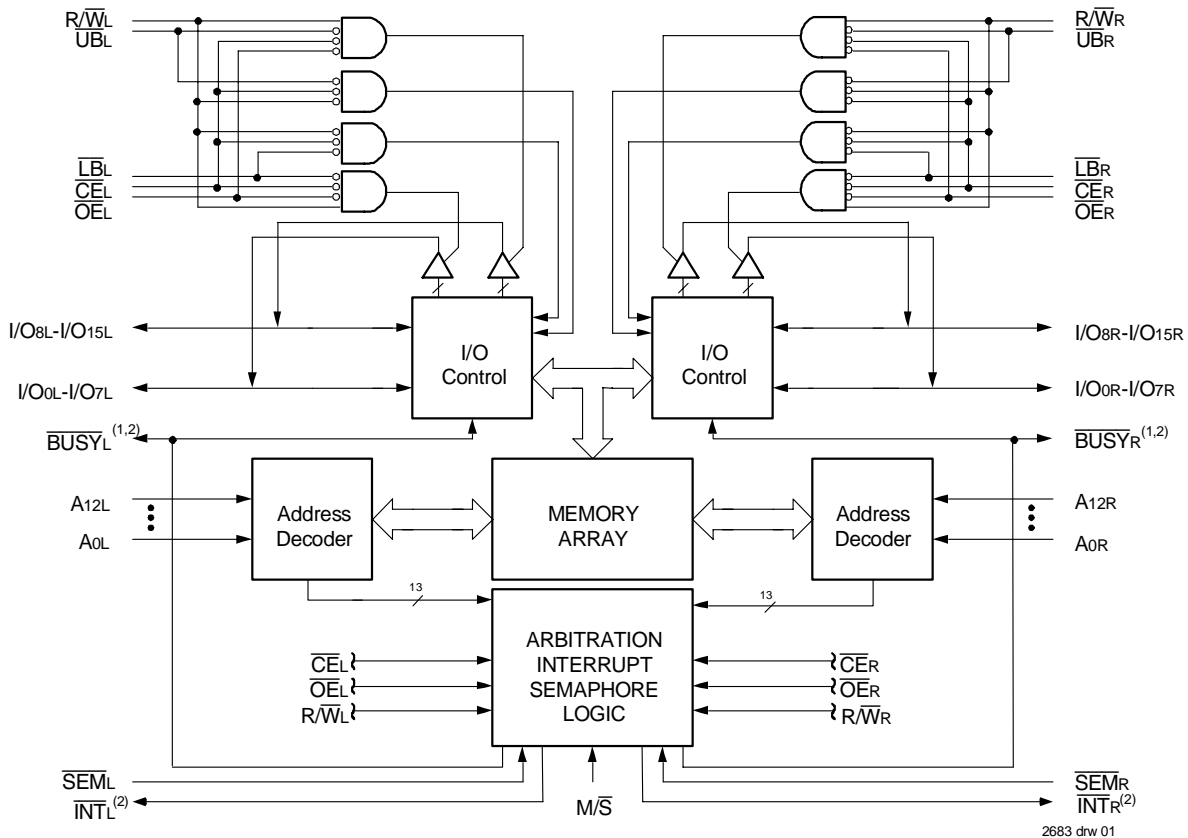
HIGH-SPEED 8K x 16 DUAL-PORT STATIC RAM

IDT7025S/L

Features

- ◆ True Dual-Ported memory cells which allow simultaneous reads of the same memory location
 - ◆ High-speed access
 - Military: 20/25/35/55/70ns (max.)
 - Industrial: 55ns (max.)
 - Commercial: 15/17/20/25/35/55ns (max.)
 - ◆ Low-power operation
 - IDT7025S
Active: 750mW (typ.)
Standby: 5mW (typ.)
 - IDT7025L
Active: 750mW (typ.)
Standby: 1mW (typ.)
 - ◆ Separate upper-byte and lower-byte control for multiplexed bus compatibility
- ◆ IDT7025 easily expands data bus width to 32 bits or more using the Master/Slave select when cascading more than one device
 - ◆ $\overline{M/S} = H$ for \overline{BUSY} output flag on Master
 $\overline{M/S} = L$ for \overline{BUSY} input on Slave
 - ◆ Interrupt Flag
 - ◆ On-chip port arbitration logic
 - ◆ Full on-chip hardware support of semaphore signaling between ports
 - ◆ Fully asynchronous operation from either port
 - ◆ Battery backup operation—2V data retention
 - ◆ TTL-compatible, single 5V ($\pm 10\%$) power supply
 - ◆ Available in 84-pin PGA, Flatpack, PLCC, and 100-pin Thin Quad Flatpack
 - ◆ Industrial temperature range (-40°C to $+85^{\circ}\text{C}$) is available for selected speeds

Functional Block Diagram



NOTES:

1. (MASTER): \overline{BUSY} is output; (SLAVE): \overline{BUSY} is input.
2. \overline{BUSY} outputs and \overline{INT} outputs are non-tri-stated push-pull.

OCTOBER 2008

Description

The IDT7025 is a high-speed 8K x 16 Dual-Port Static RAM. The IDT7025 is designed to be used as a stand-alone 128K-bit Dual-Port RAM or as a combination MASTER/SLAVE Dual-Port RAM for 32-bit or more word systems. Using the IDT MASTER/SLAVE Dual-Port RAM approach in 32-bit or wider memory system applications results in full-speed, error-free operation without the need for additional discrete logic.

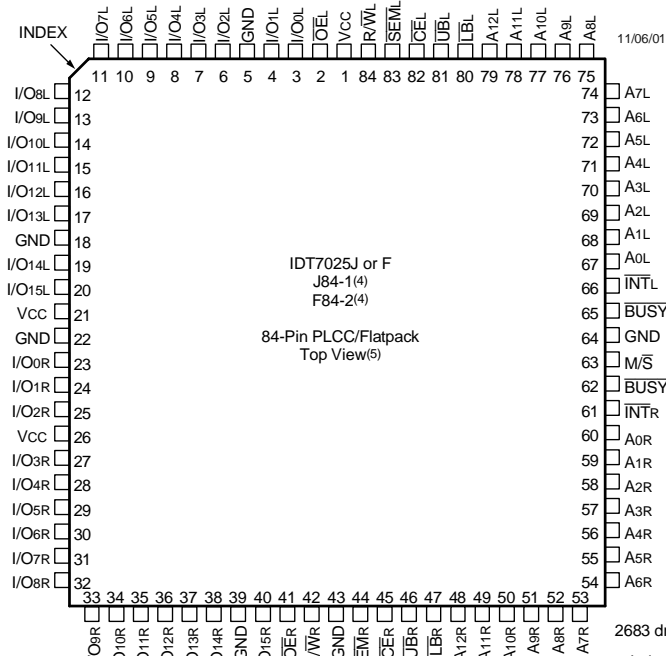
This device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature controlled by Chip Enable (\overline{CE}) permits the on-chip circuitry of each

port to enter a very low standby power mode.

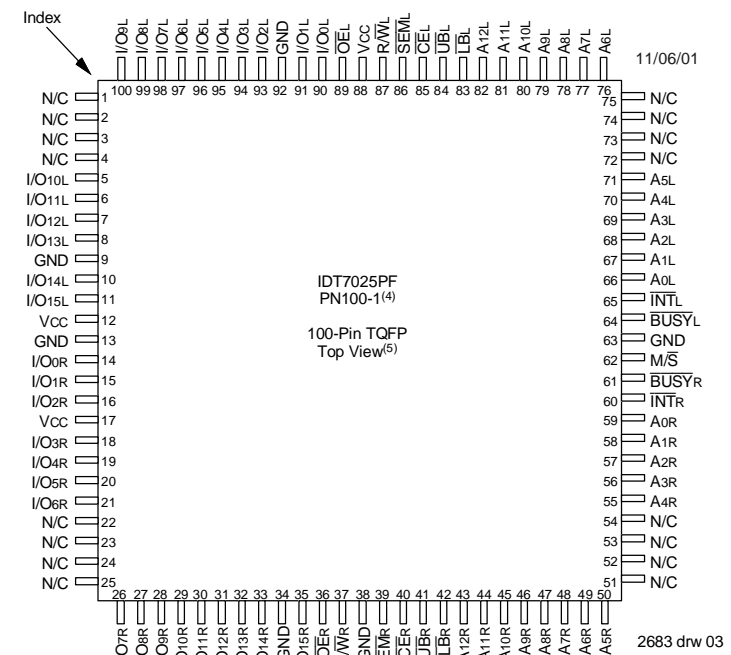
Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 750mW of power. Low-power (L) versions offer battery backup data retention capability with typical power consumption of 500 μ W from a 2V battery.

The IDT7025 is packaged in a ceramic 84-pin PGA, an 84-pin Flatpack, PLCC, and a 100-pin TQFP. Military grade product is manufactured in compliance with the latest revision of MIL-PRF-38535 QML, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

Pin Configurations^(1,2,3)



2683 drw 02



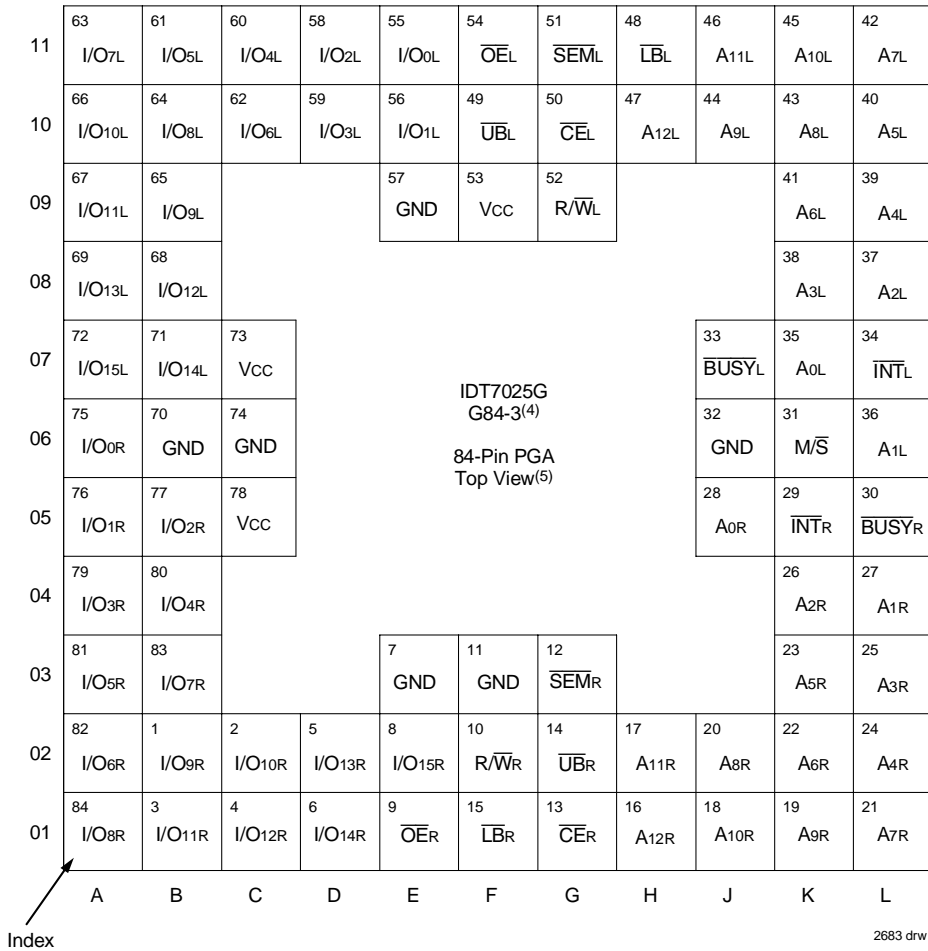
2683 drw 03

NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. J84-1 package body is approximately 1.15 in x 1.15 in x .17 in.
F84-2 package body is approximately 1.17 in x 1.17 in x .11 in.
PN100-1 package body is approximately 14mm x 14mm x 1.4mm.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Configurations^(1,2,3) (con't.)

11/06/01



2683 drw 04

NOTES:

1. All Vcc pins must be connected to power supply.
2. All GND pins must be connected to ground supply.
3. Package body is approximately 1.12 in x 1.12 in x .16 in.
4. This package code is used to reference the package diagram.
5. This text does not indicate orientation of the actual part-marking.

Pin Names

| |
|---|
| C |
| R |
| C |
| A |
| V |
| S |
| U |
| L |
| I |
| E |
| |
| |

Truth Table I: Non-Contention Read/Write Control

| Inputs ⁽¹⁾ | | | | | | Outputs | | Mode |
|-----------------------|------------------|-----------------|-----------------|-----------------|------------------|---------------------|---------------------|--------------------------|
| \overline{CE} | R/\overline{W} | \overline{OE} | \overline{UB} | \overline{LB} | \overline{SEM} | I/O ₈₋₁₅ | I/O ₀₋₇ | |
| H | X | X | X | X | H | High-Z | High-Z | Deselected |
| X | X | X | H | H | H | High-Z | High-Z | Both Bytes Deselected |
| L | L | X | L | H | H | DATA _{IN} | High-Z | Write to Upper Byte Only |
| L | L | X | H | L | H | High-Z | DATA _{IN} | Write to Lower Byte Only |
| L | L | X | L | L | H | DATA _{IN} | DATA _{IN} | Write to Both Bytes |
| L | H | L | L | H | H | DATA _{OUT} | High-Z | Read Upper Byte Only |
| L | H | L | H | L | H | High-Z | DATA _{OUT} | Read Lower Byte Only |
| L | H | L | L | L | H | DATA _{OUT} | DATA _{OUT} | Read Both Bytes |
| X | X | H | X | X | X | High-Z | High-Z | Outputs Disabled |

NOTE:

1. $A_{0L} - A_{12L} \neq A_{0R} - A_{12R}$.

2683 tbl 02

Truth Table II: Semaphore Read/Write Control⁽¹⁾

| Inputs | | | | | | Outputs | | Mode |
|-----------------|------------------|-----------------|-----------------|-----------------|------------------|---------------------|---------------------|--|
| \overline{CE} | R/\overline{W} | \overline{OE} | \overline{UB} | \overline{LB} | \overline{SEM} | I/O ₈₋₁₅ | I/O ₀₋₇ | |
| H | H | L | X | X | L | DATA _{OUT} | DATA _{OUT} | Read Semaphore Flag Data Out |
| X | H | L | H | H | L | DATA _{OUT} | DATA _{OUT} | Read Semaphore Flag Data Out |
| H | ↑ | X | X | X | L | DATA _{IN} | DATA _{IN} | Write I/O ₀ into Semaphore Flag |
| X | ↑ | X | H | H | L | DATA _{IN} | DATA _{IN} | Write I/O ₀ into Semaphore Flag |
| L | X | X | L | X | L | — | — | Not Allowed |
| L | X | X | X | L | L | — | — | Not Allowed |

NOTES:

1. There are eight semaphore flags written to via I/O₀ and read from I/O₀ - I/O₁₅. These eight semaphores are addressed by A₀ - A₂.

2683 tbl 03

Absolute Maximum Ratings⁽¹⁾

| Symbol | Rating | Commercial & Industrial | Military | Unit |
|----------------------------------|--------------------------------------|-------------------------|--------------|------|
| V _{TERM} ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| T _{BIAS} | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| T _{STG} | Storage Temperature | -65 to +150 | -65 to +150 | °C |
| I _{OUT} | DC Output Current | 50 | 50 | mA |

2683 tbl 04

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{TERM} must not exceed V_{CC} + 10% for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20 mA for the period over V_{TERM} ≥ V_{CC} + 10%.

Capacitance⁽¹⁾ (T_A = +25°C, f = 1.0mhz)

| Symbol | Parameter | Conditions ⁽²⁾ | Max. | Unit |
|------------------|--------------------|---------------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 3dV | 9 | pF |
| C _{OUT} | Output Capacitance | V _{OUT} = 3dV | 10 | pF |

2683 tbl 07

NOTES:

- This parameter is determined by device characterization but is not production tested. For TQFP package only.
- 3dV references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

Maximum Operating Temperature and Supply Voltage⁽¹⁾

| Grade | Ambient Temperature | GND | V _{CC} |
|------------|---------------------|-----|-----------------|
| Military | -55°C to +125°C | 0V | 5.0V ± 10% |
| Commercial | 0°C to +70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |

2683 tbl 05

NOTES:

- This is parameter T_A. This is the "instant on" case temperature.

Recommended DC Operating Conditions

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|-----------------|--------------------|---------------------|------|--------------------|------|
| V _{CC} | Supply Voltage | 4.5 | 5.0 | 5.5 | V |
| GND | Ground | 0 | 0 | 0 | V |
| V _{IH} | Input High Voltage | 2.2 | — | 6.0 ⁽²⁾ | V |
| V _{IL} | Input Low Voltage | -0.5 ⁽¹⁾ | — | 0.8 | V |

2683 tbl 06

NOTES:

- V_{IL} ≥ -1.5V for pulse width less than 10ns.
- V_{TERM} must not exceed V_{CC} + 10%.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Conditions | 7025S | | 7025L | | Unit |
|-----------------|--------------------------------------|---|-------|------|-------|------|------|
| | | | Min. | Max. | Min. | Max. | |
| I _L | Input Leakage Current ⁽¹⁾ | V _{CC} = 5.5V, V _{IN} = 0V to V _{CC} | — | 10 | — | 5 | μA |
| I _O | Output Leakage Current | V _{OUT} = 0V to V _{CC} | — | 10 | — | 5 | μA |
| V _{OL} | Output Low Voltage | I _{OL} = +4mA | — | 0.4 | — | 0.4 | V |
| V _{OH} | Output High Voltage | I _{OH} = -4mA | 2.4 | — | 2.4 | — | V |

2683 tbl 08

NOTE:

- At V_{CC} ≤ 2.0V input leakages are undefined.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾ (V_{CC} = 5.0V ± 10%)

| Symbol | Parameter | Test Condition | Version | 7025X15 Com'l Only | | 7025X17 Com'l Only | | 7025X20 Com'l, Ind & Military | | 7025X25 Com'l & Military | | Unit | |
|------------------|---|--|-----------|---------------------|------|---------------------|------|-------------------------------|------|--------------------------|------|------|----|
| | | | | Typ. ⁽²⁾ | Max. | Typ. ⁽²⁾ | Max. | Typ. ⁽²⁾ | Max. | Typ. ⁽²⁾ | Max. | | |
| I _{CC} | Dynamic Operating Current (Both Ports Active) | $\overline{CE} = V_{IL}$, Outputs Disabled $\overline{SEM} = V_{IH}$ $f = f_{MAX}^{(3)}$ | COM'L | S | 170 | 310 | 170 | 310 | 160 | 290 | 155 | 265 | mA |
| | | | | L | 170 | 260 | 170 | 260 | 160 | 240 | 155 | 220 | |
| | | | MIL & IND | S | — | — | — | — | 160 | 370 | 155 | 340 | |
| | | | | L | — | — | — | — | 160 | 320 | 155 | 280 | |
| I _{SB1} | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L = \overline{CE}_R = V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$ $f = f_{MAX}^{(3)}$ | COM'L | S | 20 | 60 | 20 | 60 | 20 | 60 | 16 | 60 | mA |
| | | | | L | 20 | 50 | 20 | 50 | 20 | 50 | 16 | 50 | |
| | | | MIL & IND | S | — | — | — | — | 20 | 90 | 16 | 80 | |
| | | | | L | — | — | — | — | 20 | 70 | 16 | 65 | |
| I _{SB2} | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{A^*} = V_{IL}$ and $\overline{CE}_{B^*} = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$ | COM'L | S | 105 | 190 | 105 | 190 | 95 | 180 | 90 | 170 | mA |
| | | | | L | 105 | 160 | 105 | 160 | 95 | 150 | 90 | 140 | |
| | | | MIL & IND | S | — | — | — | — | 95 | 240 | 90 | 215 | |
| | | | | L | — | — | — | — | 95 | 210 | 90 | 180 | |
| I _{SB3} | Full Standby Current (Both Ports - CMOS Level Inputs) | \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(4)}$ $\overline{SEM}_R = \overline{SEM}_L \geq V_{CC} - 0.2V$ | COM'L | S | 1.0 | 15 | 1.0 | 15 | 1.0 | 15 | 1.0 | 15 | mA |
| | | | | L | 0.2 | 5 | 0.2 | 5 | 0.2 | 5 | 0.2 | 5 | |
| | | | MIL & IND | S | — | — | — | — | 1.0 | 30 | 1.0 | 30 | |
| | | | | L | — | — | — | — | 0.2 | 10 | 0.2 | 10 | |
| I _{SB4} | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{A^*} \leq 0.2V$ and $\overline{CE}_{B^*} \geq V_{CC} - 0.2V^{(5)}$ $\overline{SEM}_R = \overline{SEM}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$ | COM'L | S | 100 | 170 | 100 | 170 | 90 | 155 | 85 | 145 | mA |
| | | | | L | 100 | 140 | 100 | 140 | 90 | 130 | 85 | 120 | |
| | | | MIL & IND | S | — | — | — | — | 90 | 225 | 85 | 200 | |
| | | | | L | — | — | — | — | 90 | 200 | 85 | 170 | |

2683 tbl 09a

| Symbol | Parameter | Test Condition | Version | 7025X35 Com'l & Military | | 7025X55 Com'l, Ind & Military | | 7025X70 Military Only | | Unit | |
|------------------|---|--|-----------|--------------------------|------|-------------------------------|------|-----------------------|------|------|----|
| | | | | Typ. ⁽²⁾ | Max. | Typ. ⁽²⁾ | Max. | Typ. ⁽²⁾ | Max. | | |
| I _{CC} | Dynamic Operating Current (Both Ports Active) | $\overline{CE} = V_{IL}$, Outputs Disabled $\overline{SEM} = V_{IH}$ $f = f_{MAX}^{(3)}$ | COM'L | S | 150 | 250 | 150 | 250 | — | — | mA |
| | | | | L | 150 | 210 | 150 | 210 | — | — | |
| | | | MIL & IND | S | 150 | 300 | 150 | 300 | 140 | 300 | |
| | | | | L | 150 | 250 | 150 | 250 | 140 | 250 | |
| I _{SB1} | Standby Current (Both Ports - TTL Level Inputs) | $\overline{CE}_L = \overline{CE}_R = V_{IH}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$ $f = f_{MAX}^{(3)}$ | COM'L | S | 13 | 60 | 13 | 60 | — | — | mA |
| | | | | L | 13 | 50 | 13 | 50 | — | — | |
| | | | MIL & IND | S | 13 | 80 | 13 | 80 | 10 | 80 | |
| | | | | L | 13 | 65 | 13 | 65 | 10 | 65 | |
| I _{SB2} | Standby Current (One Port - TTL Level Inputs) | $\overline{CE}_{A^*} = V_{IL}$ and $\overline{CE}_{B^*} = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$ $\overline{SEM}_R = \overline{SEM}_L = V_{IH}$ | COM'L | S | 85 | 155 | 85 | 155 | — | — | mA |
| | | | | L | 85 | 130 | 85 | 130 | — | — | |
| | | | MIL & IND | S | 85 | 190 | 85 | 190 | 80 | 190 | |
| | | | | L | 85 | 160 | 85 | 160 | 80 | 160 | |
| I _{SB3} | Full Standby Current (Both Ports - CMOS Level Inputs) | \overline{CE}_L and $\overline{CE}_R \geq V_{CC} - 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$, $f = 0^{(4)}$ $\overline{SEM}_R = \overline{SEM}_L \geq V_{CC} - 0.2V$ | COM'L | S | 1.0 | 15 | 1.0 | 15 | — | — | mA |
| | | | | L | 0.2 | 5 | 0.2 | 5 | — | — | |
| | | | MIL & IND | S | 1.0 | 30 | 1.0 | 30 | 1.0 | 30 | |
| | | | | L | 0.2 | 10 | 0.2 | 10 | 0.2 | 10 | |
| I _{SB4} | Full Standby Current (One Port - CMOS Level Inputs) | $\overline{CE}_{A^*} \leq 0.2V$ and $\overline{CE}_{B^*} \geq V_{CC} - 0.2V^{(5)}$ $\overline{SEM}_R = \overline{SEM}_L \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ Active Port Outputs Disabled, $f = f_{MAX}^{(3)}$ | COM'L | S | 80 | 135 | 80 | 135 | — | — | mA |
| | | | | L | 80 | 110 | 80 | 110 | — | — | |
| | | | MIL & IND | S | 80 | 175 | 80 | 175 | 75 | 175 | |
| | | | | L | 80 | 150 | 80 | 150 | 75 | 150 | |

2683 tbl 09b

NOTES:

- 'X' in part number indicates power rating (S or L)
- V_{CC} = 5V, T_A = +25°C, and are not production tested. I_{CC} dc = 120mA (TYP)
- At f = f_{MAX}, address and I/O's are cycling at the maximum frequency read cycle of 1/trc, and using "AC Test Conditions" of input levels of GND to 3V.
- f = 0 means no address or control lines change.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".

Data Retention Characteristics Over All Temperature Ranges (L Version Only)

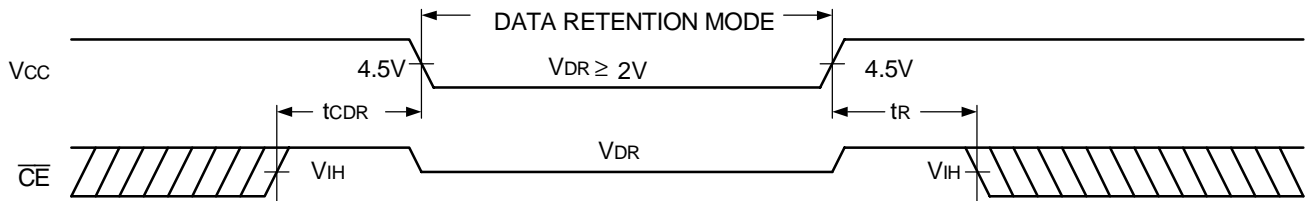
| Symbol | Parameter | Test Condition | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|---------------------------------|--------------------------------------|--|--------------------------------|---------------------|------|------|
| V _{DR} | V _{CC} for Data Retention | V _{CC} = 2V | 2.0 | — | — | V |
| I _{CCDR} | Data Retention Current | $\overline{CE} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$ | MIL. & IND. — | 100 | 4000 | μA |
| | | | COM'L. | 100 | 1500 | |
| t _{CDR} ⁽²⁾ | Chip Deselect to Data Retention Time | $\overline{SEM} \geq V_{HC}$ | 0 | — | — | ns |
| t _R ⁽³⁾ | Operation Recovery Time | | t _{RC} ⁽²⁾ | — | — | ns |

2683 tbl 10

NOTES:

1. T_A = +25°C, V_{CC} = 2V, and are not production tested.
2. t_{RC} = Read Cycle Time
3. This parameter is guaranteed by device characterization, but is not production tested.
4. At V_{CC} ≤ 2.0V input leakages are undefined.

Data Retention Waveform



2683 drw 05

AC Test Conditions

| | |
|-------------------------------|-----------------|
| Input Pulse Levels | GND to 3.0V |
| Input Rise/Fall Times | 5ns Max. |
| Input Timing Reference Levels | 1.5V |
| Output Reference Levels | 1.5V |
| Output Load | Figures 1 and 2 |

2683 tbl 11

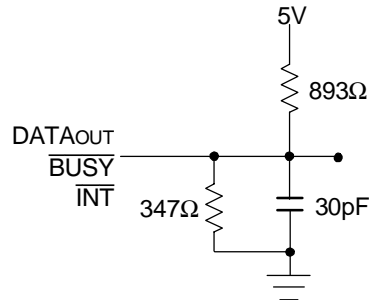
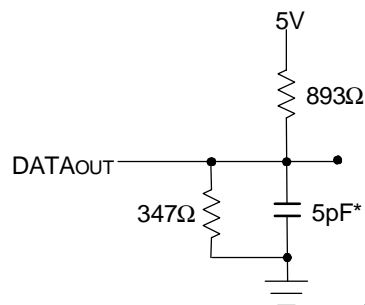


Figure 1. AC Output Test Load



2683 drw 06

Figure 2. Output Test Load
(for t_{LZ}, t_{HZ}, t_{WZ}, t_{OW})
* including scope and jig.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽⁴⁾

| Symbol | Parameter | 7025X15 Com'l Only | | 7025X17 Com'l Only | | 7025X20 Com'l, Ind & Military | | 7025X25 Com'l & Military | | Unit |
|-------------------|---|-----------------------|------|-----------------------|------|-------------------------------------|------|--------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| READ CYCLE | | | | | | | | | | |
| t _{RC} | Read Cycle Time | 15 | — | 17 | — | 20 | — | 25 | — | ns |
| t _{AA} | Address Access Time | — | 15 | — | 17 | — | 20 | — | 25 | ns |
| t _{ACE} | Chip Enable Access Time ⁽³⁾ | — | 15 | — | 17 | — | 20 | — | 25 | ns |
| t _{ABE} | Byte Enable Access Time ⁽³⁾ | — | 15 | — | 17 | — | 20 | — | 25 | ns |
| t _{AOE} | Output Enable Access Time ⁽³⁾ | — | 10 | — | 10 | — | 12 | — | 13 | ns |
| t _{OH} | Output Hold from Address Change | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t _{LZ} | Output Low-Z Time ^(1,2) | 3 | — | 3 | — | 3 | — | 3 | — | ns |
| t _{HZ} | Output High-Z Time ^(1,2) | — | 10 | — | 10 | — | 12 | — | 15 | ns |
| t _{PU} | Chip Enable to Power Up Time ^(1,2) | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| t _{PD} | Chip Disable to Power Down Time ^(1,2) | — | 15 | — | 17 | — | 20 | — | 25 | ns |
| t _{OP} | Semaphore Flag Update Pulse (\overline{OE} or \overline{SEM}) | 10 | — | 10 | — | 10 | — | 10 | — | ns |
| t _{SAA} | Semaphore Address Access ⁽³⁾ | — | 15 | — | 17 | — | 20 | — | 25 | ns |

2683 tbl 12a

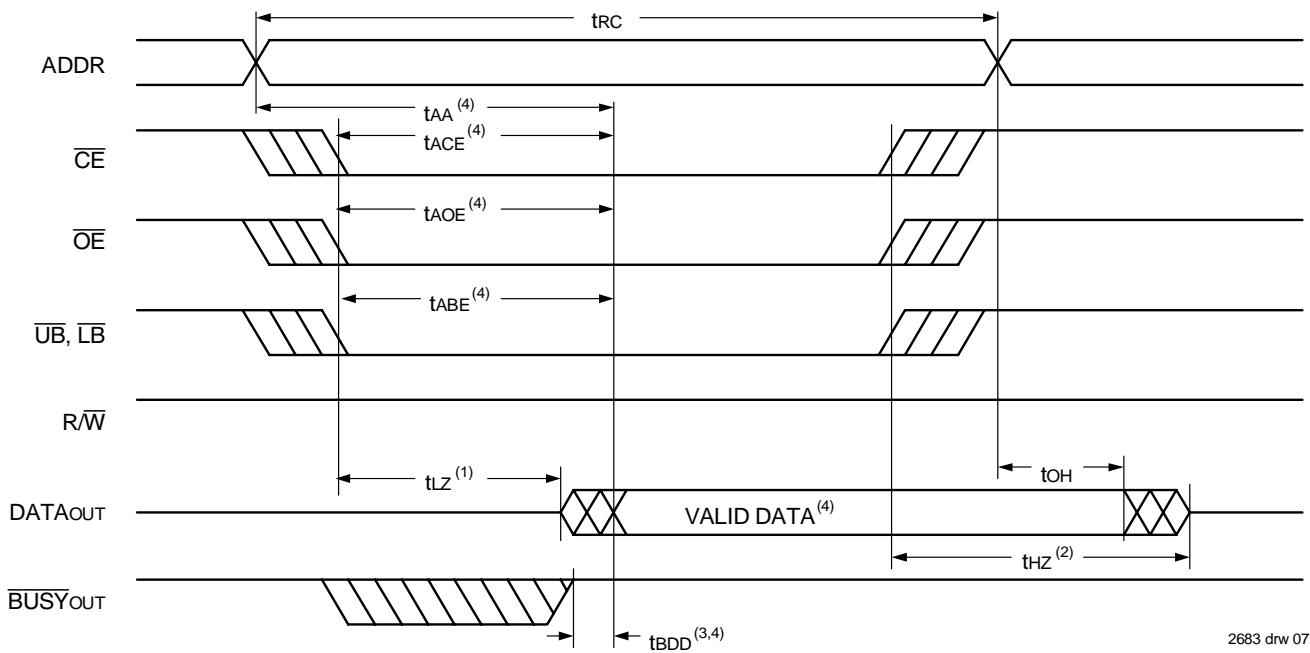
| Symbol | Parameter | 7025X35 Com'l & Military | | 7025X55 Com'l, Ind & Military | | 7025X70 Military Only | | Unit | |
|-------------------|---|--------------------------------|------|-------------------------------------|------|--------------------------|------|------|----|
| | | Min. | Max. | Min. | Max. | Min. | Max. | | |
| READ CYCLE | | | | | | | | | |
| t _{RC} | Read Cycle Time | — | 35 | — | 55 | — | 70 | — | ns |
| t _{AA} | Address Access Time | — | 35 | — | 55 | — | 70 | — | ns |
| t _{ACE} | Chip Enable Access Time ⁽³⁾ | — | 35 | — | 55 | — | 70 | — | ns |
| t _{ABE} | Byte Enable Access Time ⁽³⁾ | — | 35 | — | 55 | — | 70 | — | ns |
| t _{AOE} | Output Enable Access Time ⁽³⁾ | — | 20 | — | 30 | — | 35 | — | ns |
| t _{OH} | Output Hold from Address Change | 3 | — | 3 | — | 3 | — | — | ns |
| t _{LZ} | Output Low-Z Time ^(1,2) | 3 | — | 3 | — | 3 | — | — | ns |
| t _{HZ} | Output High-Z Time ^(1,2) | — | 15 | — | 25 | — | 30 | — | ns |
| t _{PU} | Chip Enable to Power Up Time ^(1,2) | 0 | — | 0 | — | 0 | — | — | ns |
| t _{PD} | Chip Disable to Power Down Time ^(1,2) | — | 35 | — | 50 | — | 50 | — | ns |
| t _{OP} | Semaphore Flag Update Pulse (\overline{OE} or \overline{SEM}) | 15 | — | 15 | — | 15 | — | — | ns |
| t _{SAA} | Semaphore Address Access ⁽³⁾ | — | 35 | — | 55 | — | 70 | — | ns |

2683 tbl 12b

NOTES:

1. Transition is measured 0mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{CE} = V_{IL}$, \overline{UB} or $\overline{LB} = V_{IL}$, and $\overline{SEM} = V_{IH}$. To access semaphore, $\overline{CE} = V_{IH}$ or \overline{UB} & $\overline{LB} = V_{IH}$, and $\overline{SEM} = V_{IL}$.
4. 'X' in part number indicates power rating (S or L).

Waveform of Read Cycles⁽⁵⁾

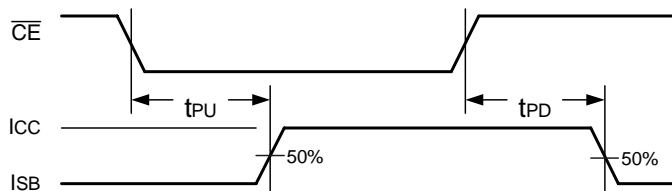


2683 drw 07

NOTES:

1. Timing depends on which signal is asserted last, \overline{OE} , \overline{CE} , \overline{LB} , or \overline{UB} .
2. Timing depends on which signal is deasserted first, \overline{CE} , \overline{OE} , \overline{LB} , or \overline{UB} .
3. t_{BDD} delay is required only in case where opposite port is completing a write operation to the same address location for simultaneous read operations \overline{BUSY} has no relation to valid output data.
4. Start of valid data depends on which timing becomes effective last t_{ABE} , t_{AOE} , t_{ACE} , t_{AA} or t_{BDD} .
5. $\overline{SEM} = V_{IH}$.

Timing of Power-Up Power-Down



2683 drw 08

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage⁽⁵⁾

| Symbol | Parameter | 7025X15 Com'l Only | | 7025X17 Com'l Only | | 7025X20 Com'l, Ind & Military | | 7025X25 Com'l & Military | | Unit |
|--------------------|--|--------------------|------|--------------------|------|-------------------------------|------|--------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE | | | | | | | | | | |
| tWC | Write Cycle Time | 15 | — | 17 | — | 20 | — | 25 | — | ns |
| tEW | Chip Enable to End-of-Write ⁽³⁾ | 12 | — | 12 | — | 15 | — | 20 | — | ns |
| tAV | Address Valid to End-of-Write | 12 | — | 12 | — | 15 | — | 20 | — | ns |
| tAS | Address Set-up Time ⁽⁶⁾ | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWP | Write Pulse Width | 12 | — | 12 | — | 15 | — | 20 | — | ns |
| tWR | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tDW | Data Valid to End-of-Write | 10 | — | 10 | — | 15 | — | 15 | — | ns |
| tHZ | Output High-Z Time ^(1,2) | — | 10 | — | 10 | — | 12 | — | 15 | ns |
| tDH | Data Hold Time ⁽⁴⁾ | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWZ | Write Enable to Output in High-Z ^(1,2) | — | 10 | — | 10 | — | 12 | — | 15 | ns |
| tOW | Output Active from End-of-Write ^(1,2,4) | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tSWRD | $\overline{\text{SEM}}$ Flag Write to Read Time | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| tSPS | $\overline{\text{SEM}}$ Flag Contention Window | 5 | — | 5 | — | 5 | — | 5 | — | ns |

2683 tbl 13a

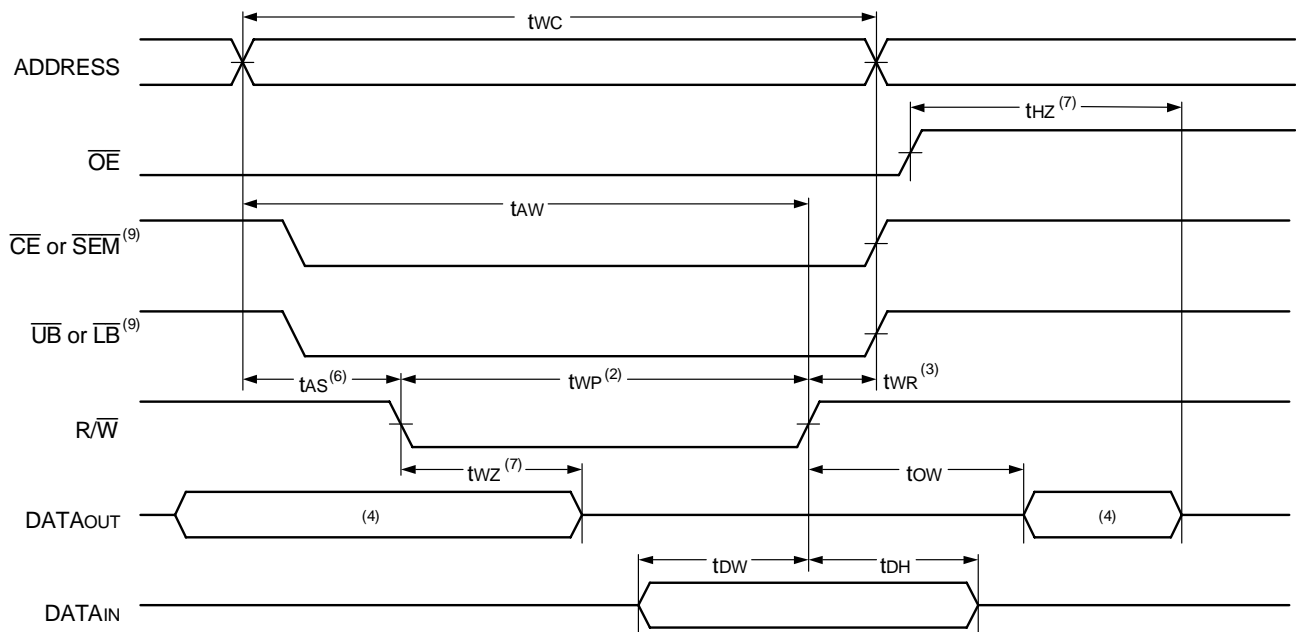
| Symbol | Parameter | 7025X35 Com'l & Military | | 7025X55 Com'l, Ind & Military | | 7025X70 Military Only | | Unit |
|--------------------|--|--------------------------|------|-------------------------------|------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| WRITE CYCLE | | | | | | | | |
| tWC | Write Cycle Time | 35 | — | 55 | — | 70 | — | ns |
| tEW | Chip Enable to End-of-Write ⁽³⁾ | 30 | — | 45 | — | 50 | — | ns |
| tAV | Address Valid to End-of-Write | 30 | — | 45 | — | 50 | — | ns |
| tAS | Address Set-up Time ⁽⁶⁾ | 0 | — | 0 | — | 0 | — | ns |
| tWP | Write Pulse Width | 25 | — | 40 | — | 50 | — | ns |
| tWR | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| tDW | Data Valid to End-of-Write | 15 | — | 30 | — | 40 | — | ns |
| tHZ | Output High-Z Time ^(1,2) | — | 15 | — | 25 | — | 30 | ns |
| tDH | Data Hold Time ⁽⁴⁾ | 0 | — | 0 | — | 0 | — | ns |
| tWZ | Write Enable to Output in High-Z ^(1,2) | — | 15 | — | 25 | — | 30 | ns |
| tOW | Output Active from End-of-Write ^(1,2,4) | 0 | — | 0 | — | 0 | — | ns |
| tSWRD | $\overline{\text{SEM}}$ Flag Write to Read Time | 5 | — | 5 | — | 5 | — | ns |
| tSPS | $\overline{\text{SEM}}$ Flag Contention Window | 5 | — | 5 | — | 5 | — | ns |

2683 tbl 13b

NOTES:

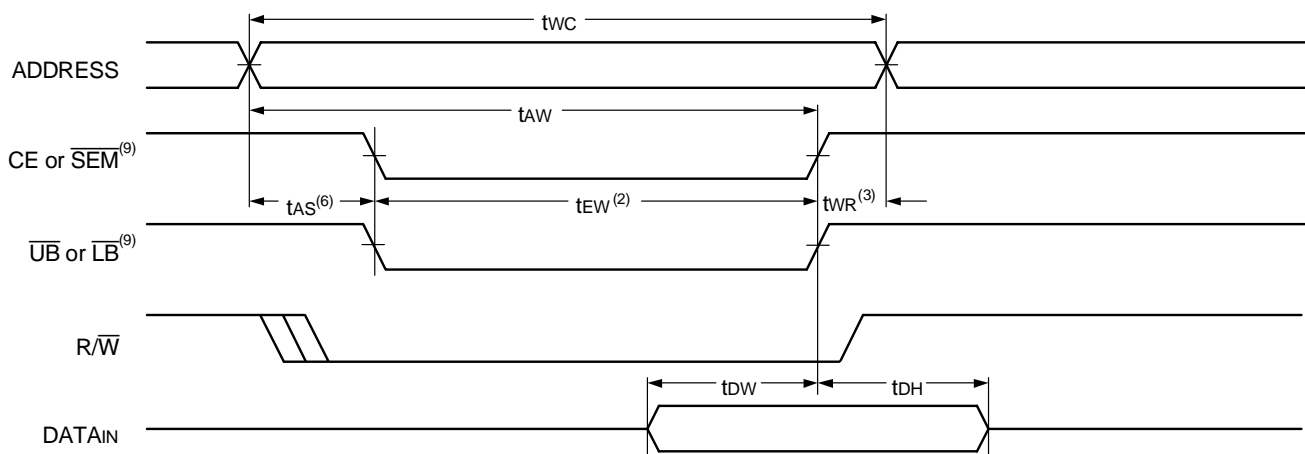
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. To access RAM, $\overline{\text{CE}} = \text{V}_{\text{IL}}$, $\overline{\text{UB}}$ or $\overline{\text{LB}} = \text{V}_{\text{IL}}$, $\overline{\text{SEM}} = \text{V}_{\text{IH}}$. To access semaphore, $\overline{\text{CE}} = \text{V}_{\text{IH}}$ or $\overline{\text{UB}} \& \overline{\text{LB}} = \text{V}_{\text{IH}}$, and $\overline{\text{SEM}} = \text{V}_{\text{IL}}$. Either condition must be valid for the entire tEW time.
4. The specification for tDH must be met by the device supplying write data to the RAM under all operating conditions. Although tDH and tOW values will vary over voltage and temperature, the actual tDH will always be smaller than the actual tOW.
5. 'X' in part number indicates power rating (S or L).

Timing Waveform of Write Cycle No. 1, R/\overline{W} Controlled Timing^(1,5,8)



2683 drw 09

Timing Waveform of Write Cycle No. 2, \overline{CE} , \overline{UB} , \overline{LB} Controlled Timing^(1,5)

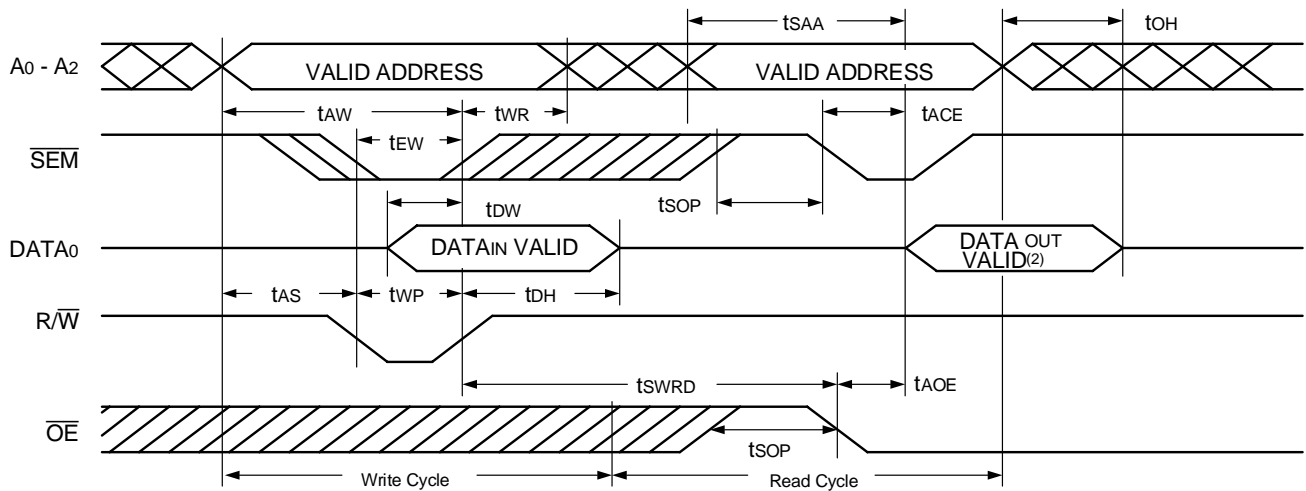


2683 drw 10

NOTES:

1. R/\overline{W} or \overline{CE} or \overline{UB} & \overline{LB} = V_{IH} during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of a \overline{UB} or \overline{LB} = V_{IL} and a \overline{CE} = V_{IL} and a R/\overline{W} = V_{IL} for memory array writing cycle.
3. t_{WR} is measured from the earlier of \overline{CE} or R/\overline{W} (or \overline{SEM} or R/\overline{W}) going to V_{IH} to the end-of-write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the \overline{CE} or \overline{SEM} LOW = V_{IL} transition occurs simultaneously with or after the R/\overline{W} = V_{IL} transition, the outputs remain in the HIGH impedance state.
6. Timing depends on which enable signal is asserted last, \overline{CE} , R/\overline{W} , or byte control.
7. This parameter is guaranteed by device characterization, but is not production tested. Transition is measured 0mV from steady state with Output Test Load (Figure 2).
8. If \overline{OE} = V_{IL} during R/\overline{W} controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off and data to be placed on the bus for the required t_{DW} . If \overline{OE} = V_{IH} during an R/\overline{W} controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP} .
9. To access RAM, \overline{CE} = V_{IL} , \overline{UB} or \overline{LB} = V_{IL} , and \overline{SEM} = V_{IH} . To access Semaphore, \overline{CE} = V_{IH} or \overline{UB} & \overline{LB} = V_{IH} , and \overline{SEM} = V_{IL} . t_{EW} must be met for either condition.

Timing Waveform of Semaphore Read after Write Timing, Either Side⁽¹⁾

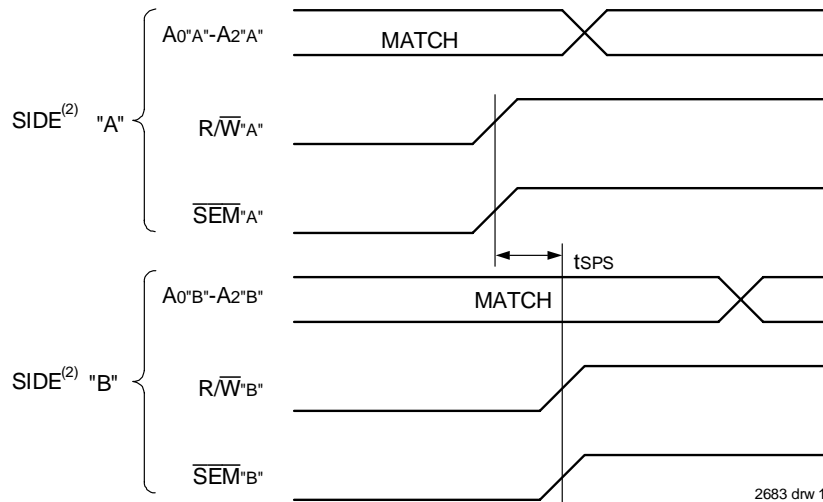


2683 drw 11

NOTE:

1. $\overline{CE} = V_{IH}$ or $\overline{UB} \& \overline{LB} = V_{IH}$ for the duration of the above timing (both write and read cycle).
2. "DATAout VALID" represents all I/O's (I/O0-I/O15) equal to the semaphore value.

Timing Waveform of Semaphore Write Contention^(1,3,4)



2683 drw 12

NOTES:

1. $DOR = DOL = V_{IL}$, $\overline{CEr} = \overline{CEl} = V_{IH}$, or both $\overline{UB} \& \overline{LB} = V_{IH}$.
2. All timing is the same for left and right port. Port "A" may be either left or right port. Port "B" is the opposite from port "A".
3. This parameter is measured from R/W^A or \overline{SEM}^A going HIGH to R/W^B or \overline{SEM}^B going HIGH.
4. If tSPS is not satisfied, there is no guarantee which side will obtain the semaphore flag.

AC Electrical Characteristics Over the Operating Temperature Supply Voltage Range⁽⁶⁾

| Symbol | Parameter | 7025X15 Com'l Ony | | 7025X17 Com'l Only | | 7025X20 Com'l, Ind & Military | | 7025X25 Com'l & Military | | Unit |
|---|--|----------------------|------|-----------------------|------|-------------------------------------|------|--------------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| BUS\bar{Y} TIMING ($M/\bar{S} = V_{IH}$) | | | | | | | | | | |
| tBAA | $\bar{B}US\bar{Y}$ Access Time from Address Match | — | 15 | — | 17 | — | 20 | — | 20 | ns |
| tBDA | $\bar{B}US\bar{Y}$ Disable Time from Address Not Matched | — | 15 | — | 17 | — | 20 | — | 20 | ns |
| tBAC | $\bar{B}US\bar{Y}$ Access Time from Chip Enable LOW | — | 15 | — | 17 | — | 20 | — | 20 | ns |
| tBDC | $\bar{B}US\bar{Y}$ Disable Time from Chip Enable HIGH | — | 15 | — | 17 | — | 17 | — | 17 | ns |
| tAPS | Arbitration Priority Set-up Time ⁽²⁾ | 5 | — | 5 | — | 5 | — | 5 | — | ns |
| tBDD | $\bar{B}US\bar{Y}$ Disable to Valid Data ⁽³⁾ | — | 18 | — | 18 | — | 30 | — | 30 | ns |
| tWH | Write Hold After $\bar{B}US\bar{Y}$ ⁽⁶⁾ | 12 | — | 13 | — | 15 | — | 17 | — | ns |
| BUS\bar{Y} TIMING ($M/\bar{S} = V_{IL}$) | | | | | | | | | | |
| tWB | $\bar{B}US\bar{Y}$ Input to Write ⁽⁴⁾ | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWH | Write Hold After $\bar{B}US\bar{Y}$ ⁽⁶⁾ | 12 | — | 13 | — | 15 | — | 17 | — | ns |
| PORT-TO-PORT DELAY TIMING | | | | | | | | | | |
| tWDD | Write Pulse to Data Delay ⁽¹⁾ | — | 30 | — | 30 | — | 45 | — | 50 | ns |
| tDDD | Write Data Valid to Read Data Delay ⁽¹⁾ | — | 25 | — | 25 | — | 35 | — | 35 | ns |

2683 tbl 14a

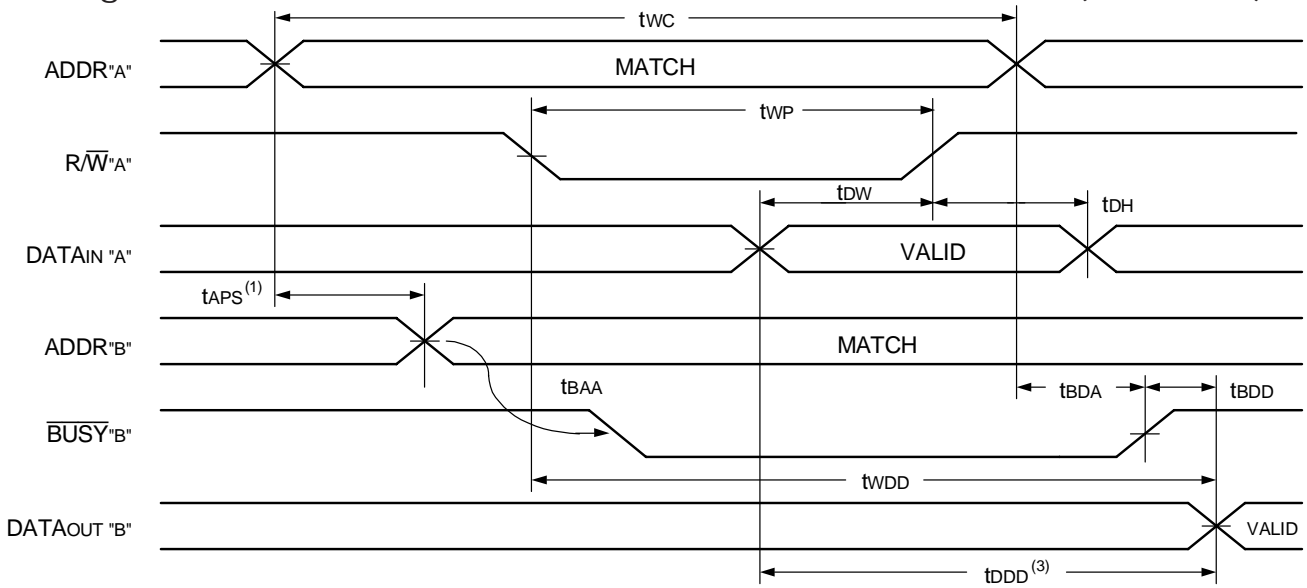
| Symbol | Parameter | 7025X35 Com'l & Military | | 7025X55 Com'l, Ind & Military | | 7025X70 Military Only | | Unit |
|---|--|--------------------------------|------|-------------------------------------|------|--------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| BUS\bar{Y} TIMING ($M/\bar{S} = V_{IH}$) | | | | | | | | |
| tBAA | $\bar{B}US\bar{Y}$ Access Time from Address Match | — | 20 | — | 45 | — | 45 | ns |
| tBDA | $\bar{B}US\bar{Y}$ Disable Time from Address Not Matched | — | 20 | — | 40 | — | 40 | ns |
| tBAC | $\bar{B}US\bar{Y}$ Access Time from Chip Enable LOW | — | 20 | — | 40 | — | 40 | ns |
| tBDC | $\bar{B}US\bar{Y}$ Disable Time from Chip Enable HIGH | — | 20 | — | 35 | — | 35 | ns |
| tAPS | Arbitration Priority Set-up Time ⁽²⁾ | 5 | — | 5 | — | 5 | — | ns |
| tBDD | $\bar{B}US\bar{Y}$ Disable to Valid Data ⁽³⁾ | — | 35 | — | 40 | — | 45 | ns |
| tWH | Write Hold After $\bar{B}US\bar{Y}$ ⁽⁶⁾ | 25 | — | 25 | — | 25 | — | ns |
| BUS\bar{Y} TIMING ($M/\bar{S} = V_{IL}$) | | | | | | | | |
| tWB | $\bar{B}US\bar{Y}$ Input to Write ⁽⁴⁾ | 0 | — | 0 | — | 0 | — | ns |
| tWH | Write Hold After $\bar{B}US\bar{Y}$ ⁽⁶⁾ | 25 | — | 25 | — | 25 | — | ns |
| PORT-TO-PORT DELAY TIMING | | | | | | | | |
| tWDD | Write Pulse to Data Delay ⁽¹⁾ | — | 60 | — | 80 | — | 95 | ns |
| tDDD | Write Data Valid to Read Data Delay ⁽¹⁾ | — | 45 | — | 65 | — | 80 | ns |

2683 tbl 14b

NOTES:

- Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write Port-to-Port Read and $\bar{B}US\bar{Y}$ ($M/\bar{S} = V_{IH}$)".
- To ensure that the earlier of the two ports wins.
- tBDD is a calculated parameter and is the greater of 0ns, tWDD – tWP (actual) or tDDD – tDW (actual).
- To ensure that the write cycle is inhibited on Port "B" during contention with Port "A".
- To ensure that a write cycle is completed on Port "B" after contention with Port "A".
- 'X' in part number indicates power rating (S or L).

Timing Waveform of Write Port-to-Port Read and **BUSY**^(2,4,5) ($M/\bar{S} = V_{IH}$)

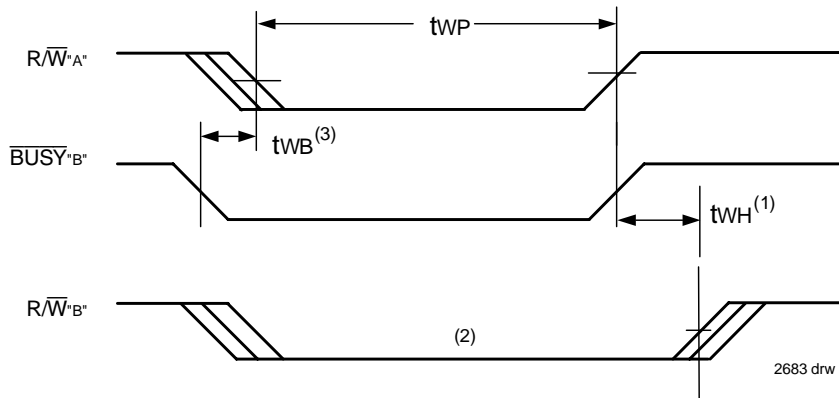


NOTES:

1. To ensure that the earlier of the two ports wins. tAPS is ignored for $M/\bar{S} = V_{IL}$ (slave).
2. $\bar{CE}_L = \bar{CE}_R = V_{IL}$.
3. $\bar{OE} = V_{IL}$ for the reading port.
4. If $M/\bar{S} = V_{IL}$ (SLAVE), then \bar{BUSY} is an input. Therefore in this example $\bar{BUSY}'_A = V_{IH}$ and \bar{BUSY}'_B input is shown.
5. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the opposite port from Port "A".

2683 drw 13

Timing Waveform of Write with **BUSY**

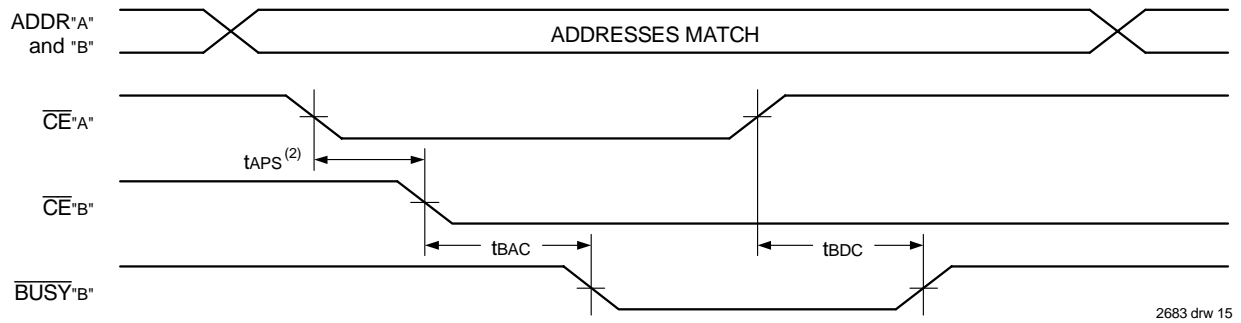


2683 drw 14

NOTES:

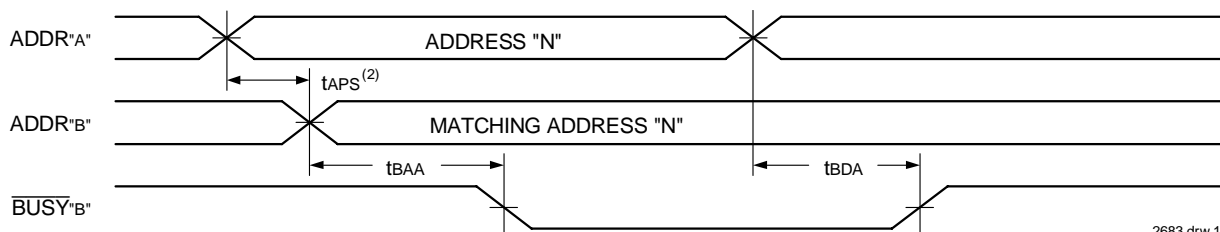
1. tWH must be met for both \bar{BUSY} input (slave) output master.
2. \bar{BUSY} is asserted on port "B" Blocking R/\bar{W}'_B , until \bar{BUSY}'_B goes HIGH.
3. tWB is only for the 'Slave' Version.

Waveform of **BUSY** Arbitration Controlled by **CE** Timing⁽¹⁾ ($M/\bar{S} = V_{IH}$)



2683 drw 15

Waveform of **BUSY** Arbitration Cycle Controlled by Address Match Timing⁽¹⁾ ($M/\bar{S} = V_{IH}$)



2683 drw 16

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. If tAPS is not satisfied, the **BUSY** signal will be asserted on one side or another but there is no guarantee on which side **BUSY** will be asserted.

AC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range⁽¹⁾

| Symbol | Parameter | 7025X15 Com'l Only | | 7025X17 Com'l Only | | 7025X20 Com'l, Ind & Military | | 7025X25 Com'l & Military | | Unit |
|-------------------------|----------------------|--------------------|------|--------------------|------|-------------------------------|------|--------------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. | |
| INTERRUPT TIMING | | | | | | | | | | |
| tAS | Address Set-up Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tWR | Write Recovery Time | 0 | — | 0 | — | 0 | — | 0 | — | ns |
| tNS | Interrupt Set Time | — | 15 | — | 15 | — | 20 | — | 20 | ns |
| tNR | Interrupt Reset Time | — | 15 | — | 15 | — | 20 | — | 20 | ns |

2683 tbl 15a

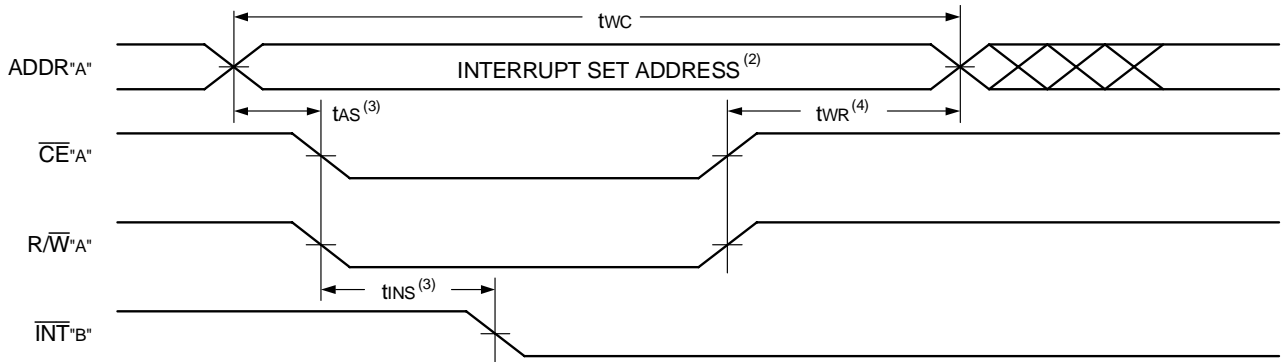
| Symbol | Parameter | 7025X35 Com'l & Military | | 7025X55 Com'l, Ind & Military | | 7025X70 Military Only | | Unit |
|-------------------------|----------------------|--------------------------|------|-------------------------------|------|-----------------------|------|------|
| | | Min. | Max. | Min. | Max. | Min. | Max. | |
| INTERRUPT TIMING | | | | | | | | |
| tAS | Address Set-up Time | 0 | — | 0 | — | 0 | — | ns |
| tWR | Write Recovery Time | 0 | — | 0 | — | 0 | — | ns |
| tNS | Interrupt Set Time | — | 25 | — | 40 | — | 50 | ns |
| tNR | Interrupt Reset Time | — | 25 | — | 40 | — | 50 | ns |

2683 tbl 15b

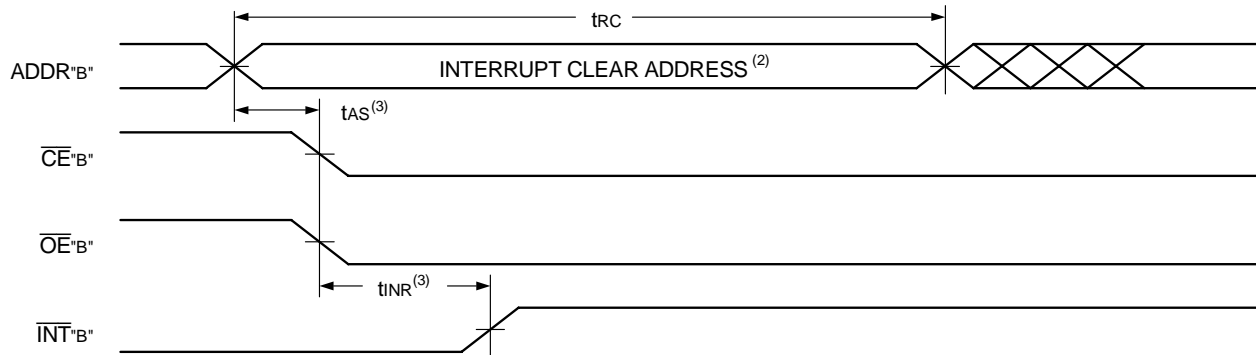
NOTES:

1. 'X' in part number indicates power rating (S or L).

Waveform of Interrupt Timing⁽¹⁾



2683 drw 17



2683 drw 18

NOTES:

1. All timing is the same for left and right ports. Port "A" may be either the left or right port. Port "B" is the port opposite from "A".
2. See Interrupt Flag Truth Table.
3. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is asserted last.
4. Timing depends on which enable signal (\overline{CE} or R/\overline{W}) is de-asserted first.

Truth Tables

Truth Table I — Interrupt Flag⁽¹⁾

| Left Port | | | | | Right Port | | | | | Function |
|------------------|-------------------|-------------------|-----------------------------------|--------------------|------------------|-------------------|-------------------|-----------------------------------|--------------------|-------------------------------------|
| R/W _L | \overline{CE}_L | \overline{OE}_L | A _{0L} -A _{12L} | \overline{INT}_L | R/W _R | \overline{CE}_R | \overline{OE}_R | A _{0R} -A _{12R} | \overline{INT}_R | |
| L | L | X | 1FFF | X | X | X | X | X | L ⁽²⁾ | Set Right \overline{INT}_R Flag |
| X | X | X | X | X | X | L | L | 1FFF | H ⁽³⁾ | Reset Right \overline{INT}_R Flag |
| X | X | X | X | L ⁽³⁾ | L | L | X | 1FFE | X | Set Left \overline{INT}_L Flag |
| X | L | L | 1FFE | H ⁽²⁾ | X | X | X | X | X | Reset Left \overline{INT}_L Flag |

2689 tbl 16

NOTES:

1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$.
2. If $\overline{BUSY}_L = V_{IL}$, then no change.
3. If $\overline{BUSY}_R = V_{IL}$, then no change.
4. \overline{INT}_R and \overline{INT}_L must be initialized at power-up.

Truth Table II — Address **BUSY** Arbitration

| Inputs | | | Outputs | | Function |
|-------------------|-------------------|--|---------------------------|---------------------------|------------------------------|
| \overline{CE}_L | \overline{CE}_R | A _{0L} -A _{12L} A _{0R} -A _{12R} | $\overline{BUSY}_L^{(1)}$ | $\overline{BUSY}_R^{(1)}$ | |
| X | X | NO MATCH | H | H | Normal |
| H | X | MATCH | H | H | Normal |
| X | H | MATCH | H | H | Normal |
| L | L | MATCH | (2) | (2) | Write Inhibit ⁽³⁾ |

2683 tbl 17

NOTES:

1. Pins \overline{BUSY}_L and \overline{BUSY}_R are both outputs when the part is configured as a master. \overline{BUSY} are inputs when configured as a slave. \overline{BUSY}_x outputs on the IDT7025 are push pull, not open drain outputs. On slaves the \overline{BUSY} asserted internally inhibits write.
2. "L" if the inputs to the opposite port were stable prior to the address and enable inputs of this port. "H" if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either \overline{BUSY}_L or $\overline{BUSY}_R = \text{LOW}$ will result. \overline{BUSY}_L and \overline{BUSY}_R outputs cannot be LOW simultaneously.
3. Writes to the left port are internally ignored when \overline{BUSY}_L outputs are driving LOW regardless of actual logic level on the pin. Writes to the right port are internally ignored when \overline{BUSY}_R outputs are driving LOW regardless of actual logic level on the pin.

Truth Table III — Example of Semaphore Procurement Sequence^(1,2,3)

| Functions | D ₀ - D ₁₅ Left | D ₀ - D ₁₅ Right | Status |
|------------------------------------|---------------------------------------|--|--|
| No Action | 1 | 1 | Semaphore free |
| Left Port Writes "0" to Semaphore | 0 | 1 | Left port has semaphore token |
| Right Port Writes "0" to Semaphore | 0 | 1 | No change. Right side has no write access to semaphore |
| Left Port Writes "1" to Semaphore | 1 | 0 | Right port obtains semaphore token |
| Left Port Writes "0" to Semaphore | 1 | 0 | No change. Left port has no write access to semaphore |
| Right Port Writes "1" to Semaphore | 0 | 1 | Left port obtains semaphore token |
| Left Port Writes "1" to Semaphore | 1 | 1 | Semaphore free |
| Right Port Writes "0" to Semaphore | 1 | 0 | Right port has semaphore token |
| Right Port Writes "1" to Semaphore | 1 | 1 | Semaphore free |
| Left Port Writes "0" to Semaphore | 0 | 1 | Left port has semaphore token |
| Left Port Writes "1" to Semaphore | 1 | 1 | Semaphore free |

2683 tbl 18

NOTES:

1. This table denotes a sequence of events for only one of the eight semaphores on the IDT7025.
2. There are eight semaphore flags written to via I/O₀ and read from all I/O's. These eight semaphores are addressed by A₀ - A₂.
3. $\overline{CE} = V_{IH}$, $\overline{SEM} = V_{IL}$, to access the semaphores. Refer to the Semaphore Read/Write Truth Table.

Functional Description

The IDT7025 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT7025 has an automatic power down feature controlled by \overline{CE} . The \overline{CE} controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE} = V_{IH}$). When a port is enabled, access to the entire memory array is permitted.

Interrupts

If the user chooses the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag (\overline{INT}_L) is asserted when the right port writes to memory location 1FFE

(HEX), where a write is defined as the $\overline{CE}_R = R/\overline{W}_R = V_{IL}$ per Truth Table I. The left port clears the interrupt by an address location 1FFE access when $\overline{CE}_L = \overline{OE}_L = V_{IL}$, R/\overline{W}_L is a "don't care". Likewise, the right port interrupt flag (\overline{INT}_R) is asserted when the left port writes to memory location 1FFF (HEX) and to clear the interrupt flag (\overline{INT}_R), the right port must access the memory location 1FFF. The message (16 bits) at 1FFE or 1FFF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 1FFE and 1FFF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table I for the interrupt operation.

that semaphore's status or remove its request for that semaphore to perform another task and occasionally attempt again to gain control of the token via the set and test sequence. Once the right side has relinquished the token, the left side should succeed in gaining control.

The semaphore flags are active LOW. A token is requested by writing a zero into a semaphore latch and is released when the same side writes a one to that latch.

The eight semaphore flags reside within the IDT7025 in a separate memory space from the Dual-Port RAM. This address space is accessed by placing a LOW input on the \overline{SEM} pin (which acts as a chip select for the semaphore flags) and using the other control pins (Address, \overline{OE} , and R/W) as they would be used in accessing a standard Static RAM. Each of the flags has a unique address which can be accessed by either side through address pins A0–A2. When accessing the semaphores, none of the other address pins has any effect.

When writing to a semaphore, only data pin Do is used. If a LOW level is written into an unused semaphore location, that flag will be set to a zero on that side and a one on the other side (see Truth Table III). That semaphore can now only be modified by the side showing the zero. When a one is written into the same location from the same side, the flag will be set to a one for both sides (unless a semaphore request from the other side is pending) and then can be written to by both sides. The fact that the side which is able to write a zero into a semaphore subsequently locks out writes from the other side is what makes semaphore flags useful in interprocessor communications. (A thorough discussion on the use of this feature follows shortly.) A zero written into the same location from the other side will be stored in the semaphore request latch for that side until the semaphore is freed by the first side.

When a semaphore flag is read, its value is spread into all data bits so that a flag that is a one reads as a one in all data bits and a flag containing a zero reads as all zeros. The read value is latched into one side's output register when that side's semaphore select (\overline{SEM}) and output enable (\overline{OE}) signals go active. This serves to disallow the semaphore from changing state in the middle of a read cycle due to a write cycle from the other side. Because of this latch, a repeated read of a semaphore in a test loop must cause either signal (\overline{SEM} or \overline{OE}) to go inactive or the output will never change.

A sequence WRITE/READ must be used by the semaphore in order to guarantee that no system level contention will occur. A processor requests access to shared resources by attempting to write a zero into a semaphore location. If the semaphore is already in use, the semaphore request latch will contain a zero, yet the semaphore flag will appear as one, a fact which the processor will verify by the subsequent read (see Truth Table III). As an example, assume a processor writes a zero to the left port at a free semaphore location. On a subsequent read, the processor will verify that it has written successfully to that location and will assume control over the resource in question. Meanwhile, if a processor on the right side attempts to write a zero to the same semaphore flag it will fail, as will be verified by the fact that a one will be read from that semaphore on the right side during subsequent read. Had a sequence of READ/WRITE been used instead, system contention problems could have occurred during the gap between the read and write cycles.

It is important to note that a failed semaphore request must be followed by either repeated reads or by writing a one into the same location. The reason for this is easily understood by looking at the simple logic diagram of the semaphore flag in Figure 4. Two semaphore request latches feed

into a semaphore flag. Whichever latch is first to present a zero to the semaphore flag will force its side of the semaphore flag LOW and the other side HIGH. This condition will continue until a one is written to the same semaphore request latch. Should the other side's semaphore request latch have been written to a zero in the meantime, the semaphore flag will flip over to the other side as soon as a one is written into the first side's request latch. The second side's flag will now stay LOW until its semaphore request latch is written to a one. From this it is easy to understand that, if a semaphore is requested and the processor which requested it no longer needs the resource, the entire system can hang up until a one is written into that semaphore request latch.

The critical case of semaphore timing is when both sides request a single token by attempting to write a zero into it at the same time. The semaphore logic is specially designed to resolve this problem. If simultaneous requests are made, the logic guarantees that only one side receives the token. If one side is earlier than the other in making the request, the first side to make the request will receive the token. If both requests arrive at the same time, the assignment will be arbitrarily made to one port or the other.

One caution that should be noted when using semaphores is that semaphores alone do not guarantee that access to a resource is secure. As with any powerful programming technique, if semaphores are misused or misinterpreted, a software error can easily happen.

Initialization of the semaphores is not automatic and must be handled via the initialization program at power-up. Since any semaphore request flag which contains a zero must be reset to a one, all semaphores on both sides should have a one written into them at initialization from both sides to assure that they will be free when needed.

Using Semaphores—Some Examples

Perhaps the simplest application of semaphores is their application as resource markers for the IDT7025's Dual-Port RAM. Say the 8K x 16 RAM was to be divided into two 4K x 16 blocks which were to be dedicated at any one time to servicing either the left or right port. Semaphore 0 could be used to indicate the side which would control the lower section of memory, and Semaphore 1 could be defined as the indicator for the upper section of memory.

To take a resource, in this example the lower 4K of Dual-Port RAM, the processor on the left port could write and then read a zero in to Semaphore 0. If this task were successfully completed (a zero was read back rather than a one), the left processor would assume control of the lower 4K. Meanwhile the right processor was attempting to gain control of the resource after the left processor, it would read back a one in response to the zero it had attempted to write into Semaphore 0. At this point, the software could choose to try and gain control of the second 4K section by writing, then reading a zero into Semaphore 1. If it succeeded in gaining control, it would lock out the left side.

Once the left side was finished with its task, it would write a one to Semaphore 0 and may then try to gain access to Semaphore 1. If Semaphore 1 was still occupied by the right side, the left side could undo its semaphore request and perform other tasks until it was able to write, then read a zero into Semaphore 1. If the right processor performs a similar task with Semaphore 0, this protocol would allow the two processors to swap 4K blocks of Dual-Port RAM with each other.

The blocks do not have to be any particular size and can even be

Ordering Information

| XXXXX | A | 999 | A | A | |
|-------------|-------|-------|---------|----------------------------|-----------------------------------|
| Device Type | Power | Speed | Package | Process/ Temperature Range | |
| | | | | Blank | Commercial (0°C to +70°C) |
| | | | | I ⁽¹⁾ | Industrial (-40°C to +85°C) |
| | | | | B | Military (-55°C to +125°C) |
| | | | | | Compliant to MIL-PRF-38535 QML |
| | | | | PF | 100-pin TQFP (PN100-1) |
| | | | | G | 84-pin PGA (G84-3) |
| | | | | J | 84-pin PLCC (J84-1) |
| | | | | F | 84-pin Flatpack (F84-2) |
| | | | | 15 | Commercial Only |
| | | | | 17 | Commercial Only |
| | | | | 20 | Commercial, Industrial & Military |
| | | | | 25 | Commercial & Military |
| | | | | 35 | Commercial & Military |
| | | | | 55 | Commercial, Industrial & Military |
| | | | | 70 | Military Only |
| | | | | S | Standard Power |
| | | | | L | Low Power |
| | | | | 7025 | 128K (8K x 16) Dual-Port RAM |

} Speed in nanoseconds

NOTE:

- Industrial range is available on selected PLCC packages in standard power. For other speeds, packages and powers contact your sales office.

2683 drw 21

Datasheet Document History

- 1/13/99: Initiated datasheet document history
Converted to new format
Cosmetic and typographical corrections
Pages 2 and 3 Added additional notes to pin configurations
- 5/19/99: Page 11 Fixed typographical error
- 6/3/99: Changed drawing format
Page 1 Corrected DSC number
- 4/4/00: Replaced IDT logo
Page 7 Fixed typo in Data Retention chart
Changed ±500mV to 0mV in notes
- 5/22/00: Page 5 Increased storage temperature parameter
Clarified TA parameter
Page 6 DC Electrical parameters—changed wording from "open" to "disabled"
- 9/13/01: Page 2 & 3 Added date revision for pin configurations
Page 6 Added Industrial temp to the column heading for 20ns to DC Electrical Characteristics
Pages 8, 10, 13&15 Added Industrial temp to the column headings for 20ns to AC Electrical Characteristics
Pages 5, 6, 8, 10, 13&15 Removed Industrial temp footnote from all tables
Page 21 Added Industrial temp to 20ns in ordering information
- 10/21/08: Page 22 Removed "IDT" from orderable part number



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
408-284-2794
DualPortHelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.