VLSI TECHNOLOGY, INC.

VL65NC02

CMOS 8-BIT MICROPROCESSOR

FEATURES

- CMOS silicon-gate technology
- Low power
  - – 1.1 mA/MHz
- Software compatible with the NMOS 6502
- Single 5 V power supply required
- 8-bit parallel processing
- True indexing capability
- Programmable stack pointer
- Interrupt capability
- Non-maskable interrupt
- 8-bit bidirectional data bus
- Addressable memory range of up to 64K bytes
- Ready input
- Direct memory access (DMA) capability
- Clock speeds up to 4 MHz
- Pipelined architecture
- On-chip clock options:
  - –External single-input clock
  - –On-board clock, single external crystal

DESCRIPTION

The VL65NC02 is an 8-bit microprocessor device produced using CMOS silicon-gate technology. This device provides advanced system architecture for enhancements in system performance, speed, and value over its NMOS counterparts, the 65XX family of microprocessor devices. The VL65NC02 is the CMOS equivalent of the NMOS 6502, and contains some enhancements. This CMOS type may exhibit different intermediate cycle information from that resident in the NMOS 6502. Intermediate cycle information is not specified, and should not be used.

The VL65NC02 provides 64K bytes of addressable memory and an interrupt input, as well as options for on-chip oscillators and drivers. It is bus and software compatible with the 65XX CPU family.

CLOCK GENERATOR

The clock generator develops all internal clock signals and (where applicable) external clock signals associated with the device. It is the clock generator that drives the timing control unit and the external timing for slave mode operations.

TIMING CONTROL

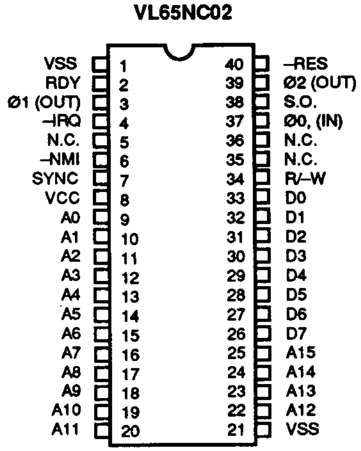
The timing control unit keeps track of the instruction cycle being monitored. The unit is set to zero each time an instruction fetch is executed and is advanced at the beginning of each phase-one clock pulse for as many cycles as are required to complete the instruction. Each data transfer that takes place between the registers depends upon decoding the contents of both the instruction register and the timing control unit.

PROGRAM COUNTER

The 16-bit program counter provides the addresses that step the microprocessor through sequential instructions in a program.

Each time the microprocessor fetches an instruction from program memory, the lower byte of the program counter (PCL) is placed on the low-order bits of the address bus and the higher byte of the program counter (PCH) is placed on the high-order 8 bits. The counter is incremented each time an instruction or data is fetched from program memory.

PIN DIAGRAM



ORDER INFORMATION

Part Number	Clock Frequency	Package
VL65NC02-01PC	1 MHz	Plastic DIP
VL65NC02-01CC		Ceramic DIP
VL65NC02-02PC	2 MHz	Plastic DIP
VL65NC02-02CC		Ceramic DIP
VL65NC02-03PC	3 MHz	Plastic DIP
VL65NC02-03CC		Ceramic DIP
VL65NC02-04PC	4 MHz	Plastic DIP
VL65NC02-04CC		Ceramic DIP

Note: Operating temperature range is 0°C to +70°C.

BLOCK DIAGRAM

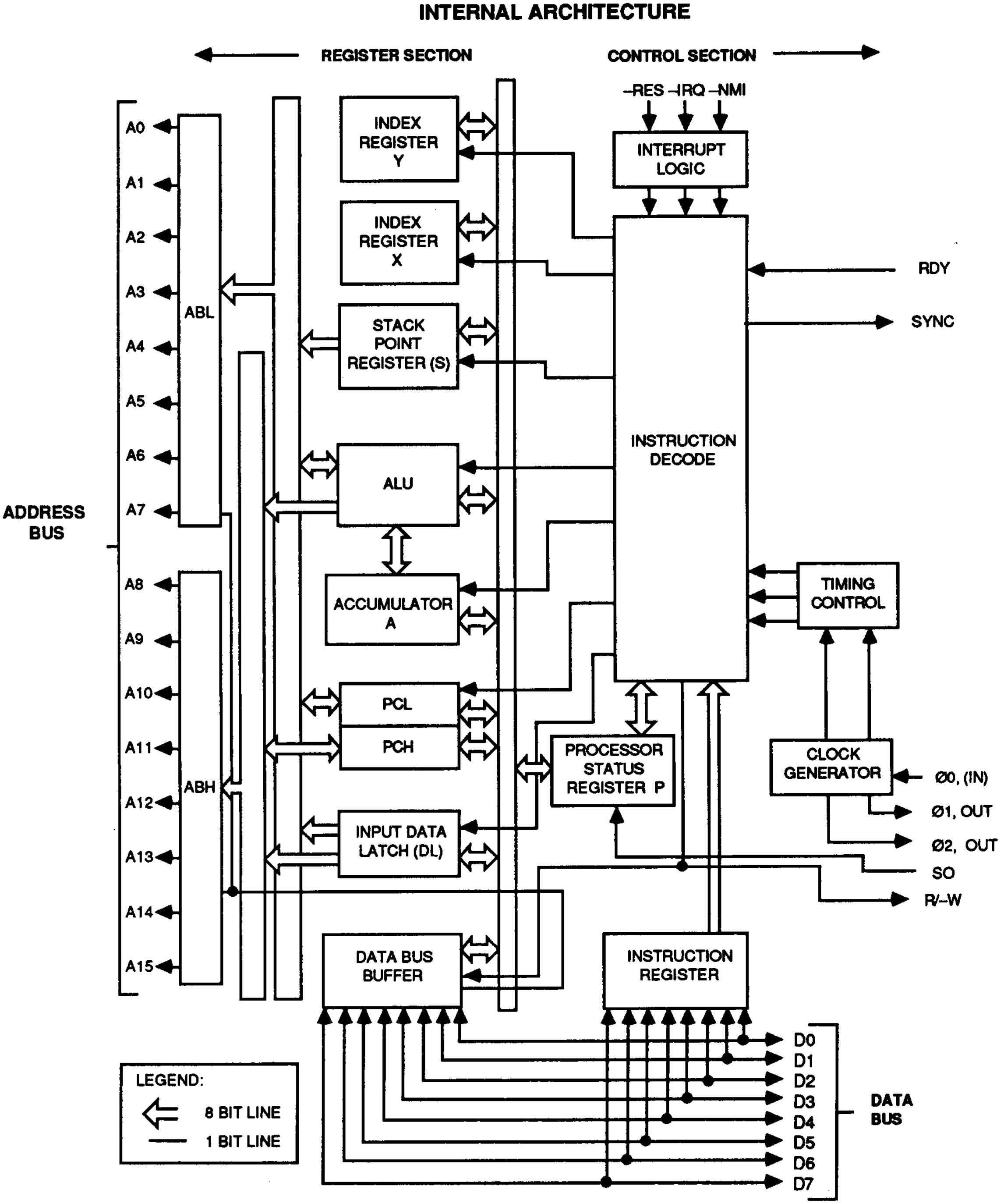


TABLE 1. HARDWARE ENHANCEMENTS

The VL65NC02 microprocessor has been designed with several hardware and software enhancements over the NMOS 6502 device, while maintaining software compatability. In addition to the increased speed and lower power consumption inherent in CMOS technology, the VL65NC02 has the following characteristics:

- Two new addressing modes
- Seven software/operational enhancements
- Two hardware enhancements:
  - Eight new instructions, 64 total
  - 27 new opcodes, 178 total

VL65NC02 Enhancements
Pin compatible with NMOS 6502
64K addressable bytes of memory
–IRQ interrupt
TTL-level single phase clock input
RC time base clock input
Crystal time base clock input
Two-phase output clock
SYNC and RDY signals
–NMI interrupt signal

SIGNAL DESCRIPTIONS

Signal Name	Pin Number	Signal Description
Ø0 (IN), Ø1 (OUT), Ø2 (OUT)	37, 3, 39	Clock Signals - The VL65NC02 requires an external Ø0 clock. Ø0 is a TTL-level input that is used to generate the internal clocks of the VL65NC02. Two full-level output clocks are generated by the VL65NC02. The Ø2 clock is in phase with Ø0. The Ø1 clock output is 180° out of phase with Ø0. When Ø0 is stopped, the CPU is in the standby mode.
–IRQ	4	Interrupt Request - This TTL-compatible input requests that an interrupt sequence begin within the microprocessor. The –IRQ is sampled during Ø2 operation; if the interrupt flag in the processor status register is zero, the current instruction is completed and the interrupt sequence begins during Ø1. The program counter and processor status register are stored in the stack. The microprocessor then sets the interrupt mask flag high so that no further –IRQs may occur. At the end of this cycle, the program counter low byte is loaded from address FFFE, and program counter high byte from location FFFF, thus transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3 kΩ external resistor should be used for proper wire-OR operation.
–NMI	6	Non-Maskable Interrupt - A negative-going edge on this input requests that a non-maskable interrupt sequence be generated within the microprocessor. The –NMI is sampled during Ø2; the current instruction is completed and the interrupt sequence begins during Ø1. The program counter is loaded with the interrupt vector from locations FFFA (low byte) and FFFB (high byte), thereby transferring program control to the non-maskable interrupt routine. Since this interrupt is non-maskable, another –NMI can occur before the first is finished. Care should be taken when using –NMI to avoid this.

SIGNAL DESCRIPTIONS (Cont.)

Signal Name	Pin Number	Signal Description
RDY	2	Ready - This input allows the user to single-cycle the microprocessor on all cycles, including write cycles. A negative transition to the low state, during or coincident with Ø1, halts the microprocessor with the output address lines reflecting the current address being fetched. This condition remains through a subsequent Ø2 in which the ready signal is low. This feature allows microprocessor interfacing with low-speed memory as well as direct memory access (DMA).
R/–W	34	Read/Write - This signal is normally in the high state, indicating that the microprocessor is reading data from memory or I/O bus. In the low state, the data bus has valid data from the microprocessor to be stored at the addressed memory location.
–SO	38	Set Overflow - A negative transition on this line sets the overflow bit (V) in the processor status register. The signal is sampled prior to the leading edge of Ø2 by the processor control time (tRWS).
–RES	40	Reset - This input resets the microprocessor. Reset must be held low for at least two clock cycles after VCC reaches operating voltage from a power-down. A positive transition on this pin causes an initialization sequence to begin. Likewise, after the system has been operating, a low on this line of at least two cycles ceases microprocessing activity, followed by initialization after the positive edge on –RES. When a positive edge is detected, there is an initialization sequence lasting six clock cycles. Then, the interrupt mask flag is set, the decimal mode is cleared, and the program counter is loaded with the restart vector from locations FFFC (low byte) and FFFD (high byte). This is the start location for program control. This input should be high in normal operation.
SYNC	7	Synchronize - This output line identifies those cycles during which the microprocessor is fetching the instruction operation code (op code). The SYNC line goes high during Ø1 of an opcode fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the Ø1 clock pulse in which SYNC went high, the processor stops in its current state and remains in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.
A0 - A15	9 - 25	Address Bus - A0-A15 forms a 16-bit address bus for memory and I/O exchanges on the data bus. The output of each address line is TTL-compatible, capable of driving one standard TTL load and 130 pF.
D0 - D7	33 - 26	Data Bus - The data lines constitute an 8-bit bidirectional data bus used for data exchanges to and from the device and peripherals. The outputs are three-state buffers capable of driving one TTL load and 130 pF.
VCC	8	5 V ± 5% power supply
VSS	1,21	Digital ground

INSTRUCTION AND REGISTER DECODE

Instructions fetched from memory are gated onto the internal data bus. These instructions are latched into the instruction register, then decoded, along with timing and interrupt signals, to generate control signals for the various registers.

ARITHMETIC/LOGIC UNIT

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the program counter). The ALU has no internal memory and is used only to perform logical and transient numerical operations.

ACCUMULATOR

The accumulator is a general-purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

INDEX REGISTER

There are two 8-bit index registers (X and Y) that may be used to count program steps or to provide an index value to be used in generating an effective address.

When executing an instruction that specifies indexed addressing, the CPU fetches the op code and the base address, and modifies the address by adding the index register to it prior to performing the desired operation. Pre- or post-indexing of indirect addresses is possible (see addressing modes).

STACK POINTER

The stack pointer is an 8-bit register used to control the addressing of the variable-length stack on page one. The stack pointer is automatically incremented and decremented under control of the microprocessor to perform stack manipulations under direction of either the program or interrupts (–NMI and –IRQ). The stack allows simple implementation of nested sub-routines and mulitple-level interrupts. The stack pointer should be initialized before any interrupts or stack operations occur.

PROCESSOR STATUS REGISTER

The 8-bit processor status register contains seven status flags. Some of the flags are controlled by the program, others may be controlled by the program and the CPU. The VL65NC02 instruction set contains a number of conditional branch instructions that are designed to allow testing of these flags.

HARDWARE ENHANCEMENTS

The VL65NC02 microprocessor incorporates several hardware enhancements over its NMOS counterpart, the 6502. These hardware enhancements are:

- The NMOS device would ignore the assertion of a Ready (RDY) during a write operation. The CMOS family stops the processor during Ø2 clock if RDY is asserted during a write operation.
- On the NMOS device, unused input-only pins (–IRQ, –NMI, RDY, –RES, and –SO) must be connected to a low impedance signal to avoid noise problems. These unused pins on the CMOS devices are internally connected by a high-impedance to VCC (approximately 250 kΩ).

OPERATIONAL ENHANCEMENTS

Tables 1 lists the operational enhancements that have been added to the VL65NC02 device.

TABLE 2. NO OPERATION (NOP) TIMING FOR UNDEFINED OPCODES

Opcode	Number of Bytes Expected (Total- Including Opcode):	Number of Cycles:
X2	2	2
X3	1	1
X7	1	1
XB	1	1
XF	1	1
44	2	3
54	2	4
D4	2	4
F4	2	4
5C	3	8
DC	3	4
FC	3	4

Note: "X" indicates a "Don't Care".

TABLE 3. INSTRUCTION SET SUMMARY

		IMMEDIATE			ABSOLUTE			ZERO PAGE			(4) IMPLIED			(IND, X)			(1) (IND), Y			ZPG,X			(1) ABS,X			(1) ABS,Y			RELATIVE (2)			INDIRECT			ZPG,Y			PROCESSOR STATUS CODE	
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7 6 4 3 2 1 0 N V B D I Z C	MNEMONIC
ADC	A + M + C → A (3)	69	2	2	6D	4	3	65	3	2				61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3				72	5	2				N V • • • Z C	ADC
AND	A∧M → A	29	2	2	2D	4	3	25	3	2				21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3				32	5	2				N • • • • Z •	AND
ASL	C ← $\boxed{7 \quad 0}$ ← 0				0E	6	3	06	5	2	0A	2	1							16	6	2	1E	6	3													N • • • • Z C	ASL
BCC	BRANCH IF C=0 (2)																												90	2	2							• • • • • • •	BCC
BCS	BRANCH IF C=1 (2)																												B0	2	2							• • • • • • •	BCS
BEQ	BRANCH IF Z=1 (2)																												F0	2	2							• • • • • • •	BEQ
BIT	A ∧ M (5)	89	2	2	2C	4	3	24	3	2										34	4	2	3C	4	3													M_7 M_6 • • • Z •	BIT
BMI	BRANCH IF N=1 (2)																												30	2	2							• • • • • • •	BMI
BNE	BRANCH IF Z=0 (2)																												D0	2	2							• • • • • • •	BNE
BPL	BRANCH IF N=0 (2)																												10	2	2							• • • • • • •	BPL
BRA	BRANCH ALWAYS (2)																												80	2	2							• • • • • • •	BRA
BRK	BREAK										00	7	1																									• • 1 0 1 • •	BRK
BVC	BRANCH IF V=0 (2)																												50	2	2							• • • • • • •	BVC
BVS	BRANCH IF V=1 (2)																												70	2	2							• • • • • • •	BVS
CLC	0 → C										18	2	1																									• • • • • • 0	CLC
CLD	0 → D										D8	2	1																									• • • 0 • • •	CLD
CLI	0 → I										58	2	1																									• • • • 0 • •	CLI
CLV	0 → V										B8	2	1																									• 0 • • • • •	CLV
CMP	A-M	C9	2	2	CD	4	3	C5	3	2				C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3				D2	5	2				N • • • • Z C	CMP
CPX	X-M	E0	2	2	EC	4	3	E4	3	2																												N • • • • Z C	CPX
CPY	Y-M	C0	2	2	CC	4	3	C4	3	2																												N • • • • Z C	CPY
DEC	DECREMENT				CE	6	3	C6	5	2	3A	2	1							D6	6	2	DE	6	3													N • • • • Z •	DEC
DEX	X-1 → X										CA	2	1																									N • • • • Z •	DEX
DEY	Y-1 → Y										88	2	1																									N • • • • Z •	DEY
EOR	A ∀ M → A	49	2	2	4D	4	3	45	3	2				41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3				52	5	2				N • • • • Z •	EOR
INC	INCREMENT				EE	6	3	E6	5	2	1A	2	1							F6	6	2	FE	6	3													N • • • • Z •	INC
INX	X + 1 → X										E8	2	1																									N • • • • Z •	INX
INY	Y + 1 → Y										C8	2	1																									N • • • • Z •	INY
JMP	JUMP TO NEW LOC				4C	3	3							7C	6	3																6C	6	3				• • • • • • •	JMP
JSR	JUMP SUB				20	6	3																															• • • • • • •	JSR
LDA	M → A	A9	2	2	AD	4	3	A5	3	2				A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3				B2	5	2				N • • • • Z •	LDA
LDX	M → X	A2	2	2	AE	4	3	A6	3	2																BE	4	3							B6	4	2	N • • • • Z •	LDX
LDY	M → Y	A0	2	2	AC	4	3	A4	3	2										B4	4	2	BC	4	3													N • • • • Z •	LDY
LSR	0 → $\boxed{7 \quad 0}$ → C				4E	6	3	46	5	2	4A	2	1							56	6	2	5E	6	3													0 • • • • Z C	LSR
NOP	NO OPERATION										EA	2	1																									• • • • • • •	NOP
ORA	AVM → A	09	2	2	0D	4	3	05	3	2				01	6	2	11	5	2	15	4	2	1D	4	3	19	4	3				12	5	2				N • • • • Z •	ORA
PHA	A → Ms S-1 → S										48	3	1																									• • • • • • •	PHA
PHP	P → Ms S-1 → S										08	3	1																									• • • • • • •	PHP
PHX	X → Ms S-1 → S										DA	3	1																									• • • • • • •	PHX
PHY	Y → Ms S-1 → S										5A	3	1																									• • • • • • •	PHY
PLA	S+1 → S Ms → A										68	4	1																									N • • • • Z •	PLA
PLP	S+1 → S Ms → P										28	4	1																									N V 1 D I Z C	PLP
PLX	S+1 → S Ms → X										FA	4	1																									N • • • • Z •	PLX
PLY	S+1 → S Ms → Y										7A	4	1																									N • • • • Z •	PLY
ROL	← $\boxed{7 \quad 0}$ ← C				2E	6	3	26	5	2	2A	2	1							36	6	2	3E	6	3													N • • • • Z C	ROL
ROR	→ C → $\boxed{7 \quad 0}$				6E	6	3	66	5	2	6A	2	1							76	6	2	7E	6	3													N • • • • Z C	ROR
RTI	RTRN INT										40	6	1																									N V 1 D I Z C	RTI
RTS	RTRN SUB										60	6	1																									• • • • • • •	RTS
SBC	A-M-$\bar{C}$ → A (3)	E9	2	2	ED	4	3	E5	3	2				E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3				F2	5	2				N V • • • Z C	SBC
SEC	1 → C										38	2	1																									• • • • • • 1	SEC
SED	1 → D										F8	2	1																									• • • 1 • • •	SED
SEI	1 → I										78	2	1																									• • • • 1 • •	SEI
STA	A → M				8D	4	3	85	3	2				81	6	2	91	6	2	95	4	2	9D	5	3	99	5	3				92	5	2				• • • • • • •	STA
STP	STOP (1 → ϕ2)										DB	3	1																									• • • • • • •	STP
STX	X → M				8E	4	3	86	3	2																									96	4	2	• • • • • • •	STX
STY	Y → M				8C	4	3	84	3	2										94	4	2																• • • • • • •	STY
STZ	00 → M				9C	4	3	64	3	2										74	4	2	9E	5	3													• • • • • • •	STZ
TAX	A → X										AA	2	1																									N • • • • Z •	TAX
TAY	A → Y										A8	2	1																									N • • • • Z •	TAY
TRB	$\bar{A}$∧M → M (6)				1C	6	3	14	5	2																												• • • • • Z •	TRB
TSB	AVM → M (6)				0C	6	3	04	5	2																												• • • • • Z •	TSB
TSX	S → X										BA	2	1																									N • • • • Z •	TSX
TXA	X → A										8A	2	1																									N • • • • Z •	TXA
TXS	X → S										9A	2	1																									• • • • • • •	TXS
TYA	Y → A										98	2	1																									N • • • • Z •	TYA
WAI	0 → RDY										CB	3	1																									• • • • • • •	WAI

TABLE 4. INSTRUCTION SET SUMMARY ABBREVIATIONS

X	Index X	∧	And
Y	Index Y	V	Or
A	Accumulator	⊻	Exclusive Or
M	Memory per Effective Address	n	Number of Cycles
Ms	Memory per stack Pointer	#	Number of Bytes
+	Add	M6	Memory Bit 6
–	Subtract	M7	Memory Bit 7

Add 1 to "n" if decimal mode, if page boundary is crossed (except STA and STZ), or if branch on same page (add 2 if page different). Accumulator address os included in implied address. "N" and "V" flags are unchanged in immediate mode. "Z" flag includes A^M result (same as BIT instruction).

ADDRESSING MODES

The VL65NC02 CPU has 15 addressing modes (two more than the NMOS-equivalent family). In the following discussion of these addressing modes, a bracketed expression follows the title of the mode. This expression is the term used in the Instruction Set Opcode Matrix, Table 8, to make it easier to identify the actual addressing mode used by the instruction.

ACCUMULATOR ADDRESSING

[Accum]- This form of addressing is represented by a one-byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING

[IMM] - In immediate addressing, the second byte of the instruction contains the operand, with no further memory addressing required.

ABSOLUTE ADDRESSING

[Absolute] - In absolute addressing, the second byte of the instruction specifies the eight low-order bits of the effective address, while the third byte specifies the eight high-order bits. Thus, the absolute addressing mode allows access to the entire 64K bytes of addressable memory.

ZERO PAGE ADDRESSING

[ZP] - The zero page instructions allow for shorter code and execution times by fetching only the second byte of the instruction and assuming a zero high address byte. Careful use of the zero-page can result in a significant increase in code efficiency.

INDEXED ZERO PAGED ADDRESSING

[ZP, X, or Y] - (X, Y Indexing) - This form of addressing is used with the index register and is referred to as "zero-page, X" or "zero-page, Y". The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "zero-page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "zero-page" addressing nature of this mode, no carry is added to the high-order eight bits of memory and crossing of page boundaries does not occur.

INDEXED ABSOLUTE ADDRESSING

[ABS, X, or Y] - (X, Y Indexing) - This form of addressing is used in conjunction with X and Y index register and is referred to as "absolute, X" and "absolute, Y". The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields, resulting in reduced coding and execution time.

INDEXED ABSOLUTE INDIRECT

[(IND), X] - (JMP (IND), X) - The contents of the second and third instruction bytes are added to the X register. The 16-bit result is a memory address containing the effective address.

IMPLIED ADDRESSING

[Implied] - In the implied addressing mode, the address containing the operand is implicity stated in the operation code of the instruction.

RELATIVE ADDRESSING

[Relative] - Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand, which is an "offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The 8-bit offset provides a branching range of -128 to +127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING

[(IND, X)] - In indexed indirect addressing, referred to as indirect, X, the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents are the low-order eight bits of the effective address. The next memory location in page zero contains the high-order eight bits of the effective address. Both memory locations specifying the high-and low-order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING

[(IND), Y] - In indirect indexed addressing, referred to as indirect, Y, the second byte of the instruction points to a memory location in page zero. The contents of this memory location are added to the contents of the Y index register, the result being the low-order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high-order eight bits of the effective address.

ABSOLUTE INDIRECT

[Indirect] - The second byte of the instruction contains the low-order eight bits of a memory location. The high-order eight bits of that memory location are contained in the third byte of the instruction. The contents of the fully specified memory location are the low-order byte of the effective address. The next memory location contains the high-order byte of the effective address, which is loaded into the 16 bits of the program counter, (JMP (IND) only).

INDIRECT

[(IND)] - The second byte of the instruction contains a zero page address serving as the indirect pointer. This is not available on the NMOS 6500 family.

INSTRUCTION SET

Table 5 lists the instruction set for the CMOS CPU family in alphabetic order according to mnemonic. Table 6 lists the hexadecimal codes for each of the instructions that are new to the CMOS family and were not available in the NMOS 6502 device family. Table 7 lists those instructions that were available on the NMOS family, but have been assigned new addressing modes in the CMOS CPU family.

TABLE 5. INSTRUCTION SET LISTING (ALPHABETIC)

Mnemonic	Function	Mnemonic	Function
(2) ADC	Add Memory to Accumulator with Carry	NOP	No Operation
(2) AND	"AND" Memory with Accumulator		
ASL	Shift Left One Bit (Memory or Accumulator)	(2) ORA	"OR" Memory with Accumulator
(1)(3) BBR	Branch on Bit Reset	PHA	Push Accumulator on Stack
(1)(3) BBS	Branch on Bit Set	PHP	Push Processor Status on Stack
BCC	Branch on Carry Clear	(1) PHX	Push X Register on Stack
BCS	Branch on Carry Set	(1) PHY	Push Y Register on Stack
BEQ	Branch on Result Zero	PLA	Pull Accumulator from Stack
(2) BIT	Test Bits in Memory with Accumulator	PLP	Pull Processor Status from Stack
BMI	Branch on Result Minus	(1) PLX	Pull X Register from Stack
BNE	Branch on Result not Zero	(1) PLY	Pull Y Register from Stack
BPL	Branch on Result Plus		
(1) BRA	Branch Always	(1)(3) RMB	Reset Memory Bit
BRK	Force Break	ROL	Rotate One Bit Left (Memory or Accumulator)
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Right (Memory or Accumulator)
BVS	Branch on Overflow Set	RTI	Return from Interrupt
		RTS	Return from Subroutine
CLC	Clear Carry Flag		
CLD	Clear Decimal Mode	(2) SBC	Subtract Memory from Accumulator with Borrow
CLI	Clear Interrupt Disable Bit	SEC	Set Carry Flag
CLV	Clear Overflow Flag	SED	Set Decimal Mode
(2) CMP	Compare Memory and Accumulator	SEI	Set Interrupt Disable Status
CPX	Compare Memory and Index X	(1)(3) SMB	Set Memory Bit
CPY	Compare Memory and Index Y	(2) STA	Store Accumulator in Memory
		STX	Store Index X in Memory
(2) DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One	(1) STZ	Store Zero
DEY	Decrement Index Y by One		
		TAX	Transfer Accumulator to Index X
(2) EOR	"Exclusive-OR" Memory with Accumulator	TAY	Transfer Accumulator to Index Y
		(1) TRB	Test and Reset Bits
(2) INC	Increment Memory by One	(1) TSB	Test and Set Bits
INX	Increment Index X by One	TSX	Transfer Stack Pointer to Index X
INY	Increment Index Y by One	TXA	Transfer Index X to Accumulator
		TXS	Transfer Index X to Stack Register
(2) JMP	Jump to New Location	TYA	Transfer Index Y to Accumulator
JSR	Jump to New Location Saving Return Address		
(2) LDA	Load Accumulator with Memory		
LDX	Load Index X with Memory		
LDY	Load Index Y with Memory		
LSR	Shift One Bit Right (Memory or Accumulator)		

Notes:

1. CMOS instruction not available on NMOS Family.
2. Previous NMOS instruction with additional addressing mode(s) added to the CMOS family.
3. 65C02 instruction not available on VL65NC02.

TABLE 6. HEXADECIMAL CODES (NEW CMOS FAMILY INSTRUCTIONS)

Hex	Mnemonic	Description
80	BRA	Branch Relative Always (Relative)
3A	DEC	Decrement Accumulator (Accum)
1A	INC	Increment Accumulator (Accum)
DA	PHX	Push X on Stack (Implied)
5A	PHY	Push Y on Stack (Implied)
FA	PLX	Pull X from Stack (Implied)
7A	PLY	Pull Y from Stack (Implied)
9C	STZ	Store Zero (Absolute)
9E	STZ	Store Zero (ABS, X)
64	STZ	Store Zero (ZP)
74	STZ	Store Zero (ZP, X)
1C	TRB	Test and Reset Memory Bits with Accumulator (Absolute)
14	TRB	Test and Reset Memory Bits with Accumulator (ZP)
0C	TSB	Test and Set Memory Bits with Accumulator (Absolute)
04	TSB	Test and Set Memory Bits with Accumulator (ZP)
89	BIT	Test Immediate with Accumulator (IMM)
0F-7F(1)	BBR	Branch on Bit Reset (Bit Manipulation, ZP)
8F-FF(1)	BBS	Branch on Bit Set (Bit Manipulation, ZP)
07-77(1)	RMB	Reset Memory Bit (Bit Manipulation, ZP)
87-F7(1)	SMB	Set Memory Bit (Bit Manipulation, ZP)

Note:

1. Most significant digit change only. Instruction not available on 65C02.

TABLE 7. HEXADECIMAL CODES (INSTRUCTIONS WITH NEW CMOS ADDRESSING MODES)

Hex	Mnemonic	Description
72	ADC	Add Memory to Accumulator with Carry [(ZP)]
32	AND	AND Memory with Accumulator [(ZP)]
3C	BIT	Test Memory Bits with Accumulator [ABS, X]
34	BIT	Test Memory Bits with Accumulator [ZP, X]
D2	CMP	Compare Memory and Accumulator [(ZP)]
52	EOR	Exclusive-OR Memory with Accumulator [(ZP)]
7C	JMP	Jump (New addressing mode) [(IND),X]
B2	LDA	Load Accumulator with Memory [(ZP)]
12	ORA	OR Memory with Accumulator [(ZP)]
F2	SBC	Subtract Memory from Accumulator with Borrow [(ZP)]
92	STA	Store Accumulator in Memory [(ZP)]

TABLE 8. INSTRUCTION SET OPCODE MATRIX

The following matrix shows the 210 op codes associated with the VL65NC02 microprocessor. The matrix identifies the hexadecimal code, the addressing mode, and the number of machine cycles associated with each op code.

MSD / LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK Implied 1 7	ORA (IND, X) 2 6			TSB ZP 2 5	ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2		TSB ABS 3 6	ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*	ORA (IND) 2 5		TRB ZP 2 5	ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*	INC Accum 1 2		TRB ABS 3 6	ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR ABS 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND), Y 2 5*	AND (IND) 2 5		BIT ZP, X 2 4	AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*	DEC Accum 1 2		BIT ABS, X 3 4*	AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*	EOR (IND) 2 5			EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*	PHY Implied 1 3			EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6†			STZ ZP 2 3	ADC ZP 2 3†	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2†	ROR Accum 1 2		JMP (ABS) 3 6	ADC ABS 3 4†	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND), Y 2 5*†	ADC (IND) 2 5†		STZ ZP, X 2 4	ADC ZP, X 2 4†	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*†	PLY Implied 1 4		JMP (ABS, X) 3 6	ADC ABS, X 3 4*†	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8	BRA Relative 2 3*	STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2	BIT IMM 2 2	TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND), Y 2 6	STA (IND) 2 5		STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2		STZ ABS 3 4	STA ABS, X 3 5	STZ ABS, X 3 5	BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*	LDA (IND) 2 5		LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*	CMP (IND) 2 5			CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*	PHX Implied 1 3			CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6†			CPX ZP 2 3	SBC ZP 2 3†	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2†	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4†	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*†	SBC (IND) 2 5†			SBC ZP, X 2 4†	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*†	PLX Implied 1 4			SBC ABS, X 3 4*†	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

☐ — New Opcode

	0	
0	BRK Implied 1 7	—OP Code —Addressing Mode —Instruction Bytes; Machine Cycles

†Add 1 to N if in decimal mode.

*Add 1 to N if page boundary is crossed.

**Add 1 to N if branch occurs to same page;
Add 2 to N if branch occurs to different page.

Note: All of the op codes in column 7 and column F are interpreted as a NOP in the 65NC02.

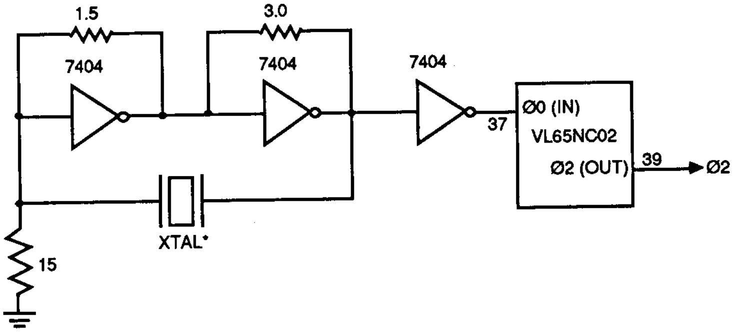
CRYSTAL/CLOCK CONSIDERATIONS

Figure 1 shows a time base generation scheme for 4 MHz operation of the VL65NC02 that has been tested and proven reliable for normal environments. As with any clock oscillator circuit, stray capacitance due to board layout can cause unpredictable results requiring "fine tuning" of the circuit. Figure 2 shows a possible external clock scheme for standby mode. Table 9 identifies nominal crystal parameters for five crystal frequencies.

	Frequency (MHz)					
Parameter	3.58	4.0	6.0	8.0	10.0	Units
RS	60	50	30-50	20-40	10-30	Ω
C0	3.5	6.5	4-6	4-6	3-5	pF
C1	0.15	0.025	0.01-0.02	0.01-0.02	0.01-0.02	pF
Q	740K	730K	720K	720K	720K	

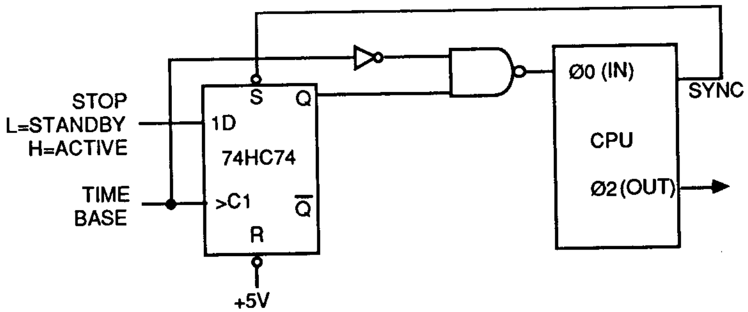
Note: AT-cut crystal parameters only. Others may be used.

FIGURE 1. TIME BASE GENERATOR



Note: CTS Knights MP Series or equivalent.

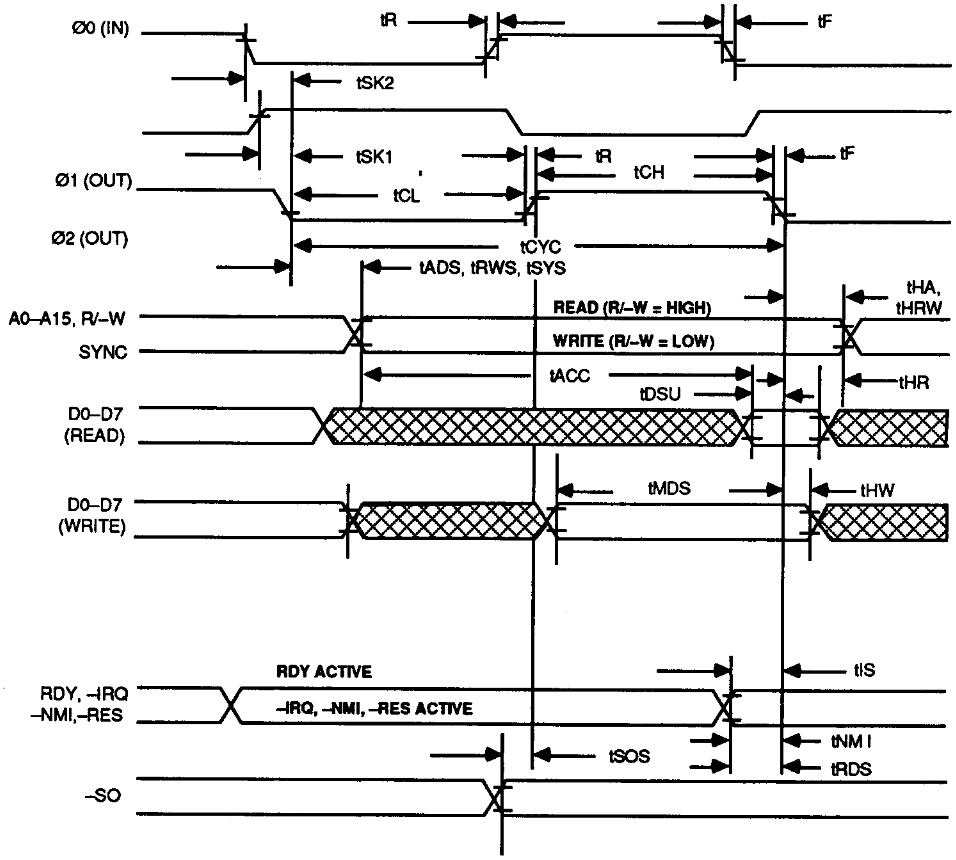
FIGURE 2. STANDBY MODE



STOPPING THE CLOCK-STANDBY MODE

Caution must be exercised when configuring the VL65NC02 in the standby mode (i.e., Ø0 (IN) clock stopped). The input clock can be held in the high state indefinitely; however, if the input clock is held in the low state longer than five µs, internal register and data status can be lost. Figure 2 shows a circuit that stops the Ø0 (IN) clock in the high state during standby mode.

FIGURE 3. TIMING DIAGRAM



Note: All timing is referenced from a high level of 2.4 volts and a low level of 0.5 volts.

AC CHARACTERISTICS: TA = 0°C to +70°C, VCC = 5 V ±5%

CLOCK TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tCYC	Ø2 Cycle Time	1000	Note(1)	500	Note(1)	333	Note(1)	250	Note(1)	ns
tCL	Ø2 Low Pulse Width	430	5000	210	5000	150	5000	100	5000	ns
tCH	Ø2 High Pulse Width	450	-	220	-	160	-	110	-	ns
tSK2	Ø0 to Ø2 Low Skew	-	50	-	50	-	40	-	30	ns
tSK1	Ø2 LOW to Ø1 High Skew	- 20	20	- 20	20	- 20	20	- 20	20	ns
tR, tF	Clock Rise and Fall Times	-	25	-	20	-	15	-	12	ns

READ/WRITE TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tRWS	R/–W Setup Time	-	125	-	100	-	75	-	60	ns
tHRW	R/–W Hold Time	15	-	15	-	15	-	15	-	ns
tADS	Address Setup Time	-	125	-	100	-	75	-	60	ns
tHA	Address Hold Time	15	-	15	-	15	-	15	-	ns
tACC	Read Access Time	775	-	340	-	215	-	160	-	ns
tDSU	Read Data Setup Time	100	-	60	-	40	-	30	-	ns
tHR	Read Data Hold Time	10	-	10	-	10	-	10	-	ns
tMDS	Write Data Delay Time	-	200	-	110	-	85	-	55	ns
tHW	Write Data Hold Time	30	-	30	-	30	-	30	-	ns

CONTROL SIGNAL TIMING

Symbol	Parameter	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
tSYS	SYNC Delay	-	125	-	100	-	75	-	60	ns
tRDS	RDY Setup Time	200	-	110	-	80	-	60	-	ns
tSOS	–SO Setup Time	75	-	50	-	40	-	30	-	ns
tIS	–IRQ,–RES Setup Time	200	-	110	-	80	-	60	-	ns
tNMI	–NMI Setup Time	200	-	150	-	100	-	70	-	ns

Notes:

1. VL65NC02 minimum operating frequency is limited by Ø2 low pulse width. The processor can be stopped with Ø2 held high.

ABSOLUTE MAXIMUM RATINGS

Ambient Operating Temperature:	
– Commercial	0°C to +70°C
– Industrial	-40°C to +85°C
Storage Temperature	-65°C to +150°C
Supply Voltage to Ground Potential	-0.3 to +7.0 V
Applied Output Voltage	-0.3 to VCC + 0.3 V
Applied Input Voltage	-0.3 to VCC + 0.3 V

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS: TA = 0°C to +70°C, VCC = +5.0 V ± 5% (Notes 1, 2, 3)

Symbol	Parameter		Min	Typ	Max	Units	Test Conditions
VIH	Input High Voltage	Ø0 (IN)	2.4	-	VCC + 0.3	V	
		All Other Inputs	2.0	-	VCC + 0.3	V	
VIL	Input Low Voltage	Ø0 (IN)	-0.3	-	+ 0.4	V	
		All Other Inputs	-0.3	-	+ 0.8	V	
IIN	Input Leakage Current	Ø0 (IN)	-	-	1.0	µA	VIN = 0 V to +5.25 V VCC = 0 V
		–NMI, –IRQ, RDY, –RES, –SO	-	-	-50	µA	
ITSI	Three-State (Off-State) Input Curr ent D7 - D0		-	-	10	µA	VIN = 0.4 V to +2.4 V VCC = +5.25 V
VOH	Output High Voltage SYNC, D7-D0, A15-A0, R/–W, Ø1, Ø2		2.4	-	-	V	VCC = +4.75 V ILOAD = -100 µA
VOL	Output Low Voltage SYNC, D7-D0, A15-A0, R/–W, Ø1, Ø2		-	-	+0.4	V	VCC = +4.75 V ILOAD = 1.6 µA
ICC	Supply Current	Standby (4)	-	2.0	10	µA	VCC = +5.0 V
		Active (5)	-	2.6	-	mA/MHz	
		Active (6)	-	-	10	mA	
		Low Power	-	1.1	-	mA/MHz	RDY = 0 V
CIN	Input Capacitance	–NMI,–IRQ,–SO, RDY	-	-	7	pF	VCC = +5.0 V, VIN = 0 V, f = 1 MHz, TA = 25°C
		Ø0 (IN)	-	-	30	pF	
CIO	I/O Capacitance - D7-D0, Ø1, Ø2		-	-	10	pF	
COUT	Output Capacitance - A15-A0,R/–W, SYNC		-	-	10	pF	

Notes:

(1) All units are direct current (DC).
(2) A negative sign indicates outward current flow, positive indicates inward flow.
(3) –IRQ and –NMI require an external pull-up resistor.
(4) Typical values are shown for VCC = +5.0 V and TA = +25°C.
(5) Typical value for power estimation only; dependent on frequency of operation.
(6) Maximum value for power consumption; independent of frequency of operation.