

**Philips Components-Signetics**

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ECL Products	

# 100141

## 4-Bit Universal Shift Register

**FEATURES**

- Typical propagation delay: 1.7ns
- Typical supply current ( $-I_{EE}$ ): 175mA

**DESCRIPTION**

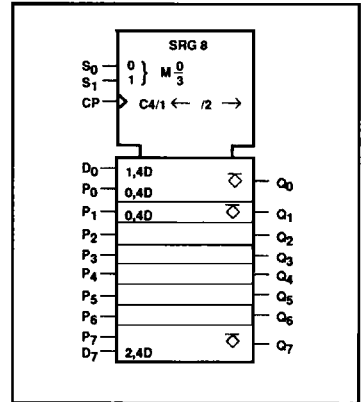
The 100141 is an 8-bit shift register with D-type flip-flops. There are two selection inputs,  $S_0$  and  $S_1$ , allowing Parallel Load, Left Shift, Right Shift, and Hold modes. Unused inputs must be tied Low (to  $V_L$  or  $V_{EE}$ ).

Unused inputs must be tied to a low voltage,  $V_{IL}$  or  $V_{EE}$ .

**PIN DESCRIPTION**

PINS	DESCRIPTION
$D_0 - D_7$	Serial Data Inputs
$P_0 - P_7$	Parallel Data Inputs
CP	Clock Input
$S_0, S_1$	Select Inputs
$Q_0 - Q_7$	Data Outputs

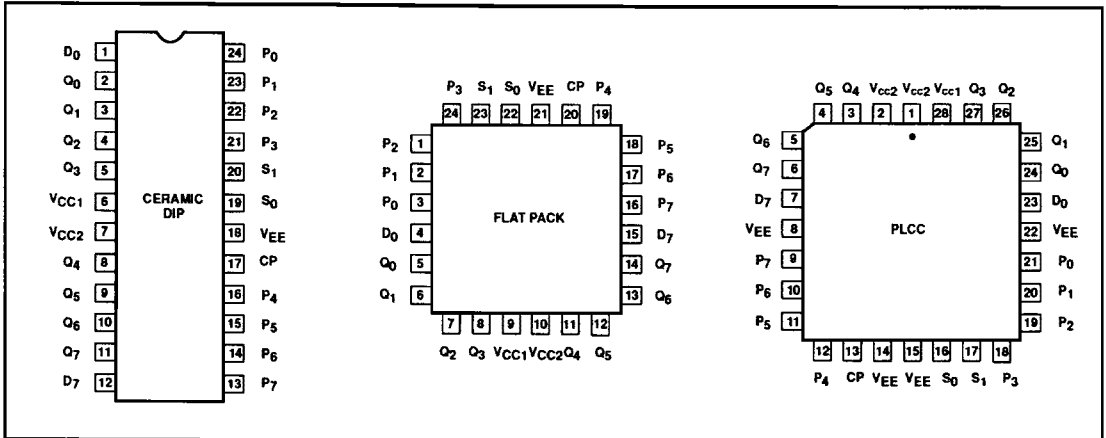
**IEC/IEEE SYMBOL**



**ORDERING INFORMATION**

PACKAGES	ORDER CODE
24-Pin Ceramic DIP (400 mils wide)	100141F
24-Pin Ceramic Flat Pack	100141Y
28-Pin PLCC	100141A

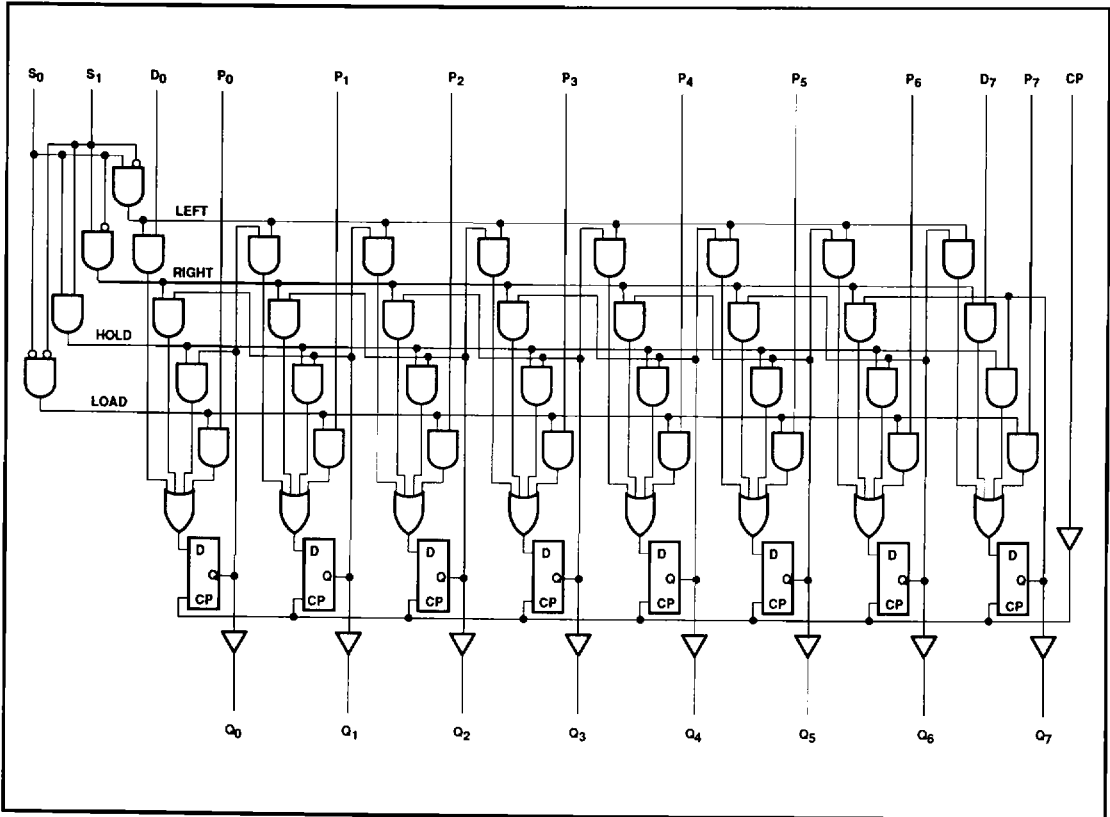
**PIN CONFIGURATIONS**



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## LOGIC DIAGRAM



## FUNCTION TABLE

FUNCTION	INPUTS					OUTPUTS							
	D <sub>7</sub>	D <sub>0</sub>	S <sub>1</sub>	S <sub>0</sub>	CP	Q <sub>7</sub>	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
Parallel Load into Register	X	X	L	L	↑	P <sub>7</sub>	P <sub>6</sub>	P <sub>5</sub>	P <sub>4</sub>	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>
Shift Left	X	L	L	H	↑	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	L
	X	H	L	H	↑	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>	H
Shift Right	L	X	H	L	↑	L	Q <sub>7</sub>	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>
	H	X	H	L	↑	Q <sub>7</sub>	Q <sub>6</sub>	Q <sub>5</sub>	Q <sub>4</sub>	Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
Hold	X	X	H	H	X	← No Change →							
	X	X	X	X	H	← No Change →							
	X	X	X	X	L	← No Change →							

### NOTES:

- H = High voltage level
- L = Low voltage level
- X = Don't care
- ↑ = Low-to-High transition

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**ABSOLUTE MAXIMUM RATINGS**  $V_{CC1} = V_{CC2} = \text{ground}$ ,  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified:

SYMBOL	PARAMETER	LIMITS	UNIT
$V_{EE}$	Supply voltage range	-7.0 to +0.5	V
$V_{IN}$	Input voltage ( $V_{IN}$ should never be more negative than $V_{EE}$ )	$V_{EE}$ to +0.5	V
$I_O$	Output source current (continuous)	-55	mA
$T_S$	Storage temperature range	-65 to +150	$^\circ\text{C}$
$T_J$	Maximum junction temperature	+150	$^\circ\text{C}$

**NOTE:**

Operation beyond the limits set forth in this table may impair the useful life of the device.

**DC OPERATING CONDITIONS**

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX	
$V_{CC1}, V_{CC2}$	Circuit ground		0	0	0	V
$V_{EE}$	Supply voltage		-4.8	-4.5	-4.2	V
$V_{EE}$	Supply voltage when operating with the 10K or the 10KH ECL family		-5.7			V
$V_{IH}$	High level input voltage	$V_{EE} = -4.2\text{V}$	-1150		-880	mV
		$V_{EE} = -4.5\text{V}$	-1165			
		$V_{EE} = -4.8\text{V}$	-1165			
$V_{IL}$	Low level input voltage	$V_{EE} = -4.2\text{V}$	-1810		-1475	mV
		$V_{EE} = -4.5\text{V}$			-1475	mV
		$V_{EE} = -4.8\text{V}$			-1490	mV
$T_A$	Operating ambient temperature range		0	+25	+85	$^\circ\text{C}$

**NOTE:**When operating at other than the specified  $V_{EE}$  voltages (-4.2V, -4.5V, -4.8V), the DC and AC electrical characteristics will vary slightly from their specified values.

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**DC ELECTRICAL CHARACTERISTICS**  $V_{CC1} = V_{CC2} = \text{ground}$ ,  $V_{EE} = -4.8\text{V}$  to  $-4.2\text{V}$ ,  $T_A = 0^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise specified<sup>1,3,4</sup>

SYMBOL	PARAMETER		TEST CONDITIONS <sup>2</sup>		LIMITS			UNIT	
					MIN.	TYP.	MAX.		
$V_{OH}$	High level output voltage		Inputs at $V_{IHMAX}$ or $V_{ILMIN}$	$V_{EE} = -4.2\text{V}$	-1020		-870	mV	
				$V_{EE} = -4.5\text{V}$	-1025	-955	-880	mV	
				$V_{EE} = -4.8\text{V}$	-1035		-880	mV	
$V_{OHT}$	High level output threshold voltage		Outputs loaded with $50\Omega$ to $-2.0\text{V}$ $\pm 0.010\text{V}$	Apply $V_{IHMIN}$ or $V_{ILMAX}$ to one input at a time. Other inputs at $V_{IHMAX}$ or $V_{ILMIN}$ .	$V_{EE} = -4.2\text{V}$	-1030			mV
				$V_{EE} = -4.5\text{V}$	-1035			mV	
				$V_{EE} = -4.8\text{V}$	-1045			mV	
$V_{OLT}$	Low level output threshold voltage		with $50\Omega$ to $-2.0\text{V}$ $\pm 0.010\text{V}$	Apply $V_{IHMIN}$ or $V_{ILMAX}$ to one input at a time. Other inputs at $V_{IHMAX}$ or $V_{ILMIN}$ .	$V_{EE} = -4.2\text{V}$			-1595	mV
				$V_{EE} = -4.5\text{V}$			-1610	mV	
				$V_{EE} = -4.8\text{V}$			-1610	mV	
$V_{OL}$	Low level output voltage		Inputs at $V_{IHMAX}$ or $V_{ILMIN}$ .	$V_{EE} = -4.2\text{V}$	-1810		-1605	mV	
				$V_{EE} = -4.5\text{V}$	-1810	-1705	-1620	mV	
				$V_{EE} = -4.8\text{V}$	-1830		-1620	mV	
$I_{IH}$	High level input current	CP	One input under test at $V_{IHMAX}$ .				550	$\mu\text{A}$	
		$D_n, P_n, S_n$	Other inputs at $V_{ILMIN}$ .				220	$\mu\text{A}$	
$I_{IL}$	Low level input current		One input under test at $V_{ILMIN}$ . Other inputs at $V_{IHMAX}$ .	0.5				$\mu\text{A}$	
$-I_{EE}$	$V_{EE}$ supply current		All inputs at $V_{IHMAX}$ .	119	175	238		mA	

**NOTES:**

- The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
- Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
- The specified limits shown in the DC electrical characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC operating conditions table.
- The device can function down to  $V_{EE} = -5.7\text{V}$ , allowing operation with either the 10K or the 10KH family. Correction factors can be used to calculate new DC limits for the extended  $V_{EE}$  range. For more information, see Chapters 5 and 10, Section 4.

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## AC ELECTRICAL CHARACTERISTICS

Ceramic DIP  $V_{CC1} = V_{CC2} = \text{ground}$ ,  $V_{EE} = -4.8\text{V to } -4.2\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$f_{\text{MAX}}$	Maximum shift frequency CP	Waveform 1	275		275		275		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay CP to $Q_n$	Waveform 1	0.90	2.40	1.10	2.40	1.10	2.55	ns
$t_{\text{TLH}}$ $t_{\text{THL}}$	Transition time		0.90	2.40	1.10	2.40	1.10	2.55	ns
$t_s$	Setup time $D_n$ , $P_n$ to CP	Waveform 2	0.45	1.40	0.45	1.30	0.45	1.40	ns
$t_h$	Hold time CP to $D_n$ , $P_n$		0.45	1.40	0.45	1.30	0.45	1.40	ns
$t_s$	Setup time $S_n$ to CP	Waveform 2	1.40		1.40		1.70		ns
$t_h$	Hold time CP to $D_n$ , $P_n$		0.60		0.60		0.60		ns
$t_s$	Setup time $S_n$ to CP	Waveform 2	3.80		3.80		3.80		ns
$t_h$	Hold time CP to $S_n$		0.10		0.10		0.10		ns
$t_w(\text{H})$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

## NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

## AC ELECTRICAL CHARACTERISTICS

Ceramic DIP  $V_{CC1} = V_{CC2} = \text{ground}$ ,  $V_{EE} = -5.2\text{V} \pm 5\%$ 

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$f_{\text{MAX}}$	Maximum shift frequency CP	Waveform 1	275		275		275		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay CP to $Q_n$	Waveform 1	0.90	2.40	1.10	2.40	1.10	2.55	ns
$t_{\text{TLH}}$ $t_{\text{THL}}$	Transition time		0.90	2.40	1.10	2.40	1.10	2.55	ns
$t_s$	Setup time $D_n$ , $P_n$ to CP	Waveform 2	0.45	1.40	0.45	1.30	0.45	1.40	ns
$t_h$	Hold time CP to $D_n$ , $P_n$		0.45	1.40	0.45	1.30	0.45	1.40	ns
$t_s$	Setup time $S_n$ to CP	Waveform 2	1.40		1.40		1.70		ns
$t_h$	Hold time CP to $S_n$		0.60		0.60		0.60		ns
$t_s$	Setup time $S_n$ to CP	Waveform 2	3.80		3.80		3.80		ns
$t_h$	Hold time CP to $S_n$		0.10		0.10		0.10		ns
$t_w(\text{H})$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

## NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

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## AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC  $V_{CC1} = V_{CC2} = \text{ground}$ ,  $V_{EE} = -4.8\text{V to } -4.2\text{V}$ 

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$f_{\text{MAX}}$	Maximum shift frequency CP	Waveform 1	300		300		300		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay CP to $Q_n$	Waveform 1	0.90 0.90	2.20 2.20	1.10 1.10	2.20 2.20	1.10 1.10	2.35 2.35	ns ns
$t_{\text{TLH}}$ $t_{\text{THL}}$	Transition time		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
$t_s$	Setup time $D_n, P_n$ to CP	Waveform 2	1.20		1.20		1.50		ns
$t_h$	Hold time CP to $D_n, P_n$		0.50		0.50		0.50		ns
$t_s$	Setup time $S_n$ to CP	Waveform 2	2.80		2.80		3.20		ns
$t_h$	Hold time CP to $S_n$		0.00		0.00		0.00		ns
$t_w(\text{H})$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

## NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

## AC ELECTRICAL CHARACTERISTICS

Flat Pack and PLCC  $V_{CC1} = V_{CC2} = \text{ground}$ ,  $V_{EE} = -5.2\text{V} \pm 5\%$ 

SYMBOL	PARAMETER	TEST CONDITION	LIMITS						UNIT
			$T_A = 0^\circ\text{C}$		$T_A = +25^\circ\text{C}$		$T_A = +85^\circ\text{C}$		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
$f_{\text{MAX}}$	Maximum shift frequency CP	Waveform 1	300		300		300		MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay CP to $Q_n$	Waveform 1	0.90 0.90	2.20 2.20	1.10 1.10	2.20 2.20	1.10 1.10	2.35 2.35	ns ns
$t_{\text{TLH}}$ $t_{\text{THL}}$	Transition time		0.45 0.45	1.40 1.40	0.45 0.45	1.30 1.30	0.45 0.45	1.40 1.40	ns ns
$t_s$	Setup time $D_n, P_n$ to CP	Waveform 2	1.20		1.20		1.50		ns
$t_h$	Hold time CP to $D_n, P_n$		0.50		0.50		0.50		ns
$t_s$	Setup time $S_n$ to CP	Waveform 2	2.80		2.80		3.20		ns
$t_h$	Hold time CP to $S_n$		0.00		0.00		0.00		ns
$t_w(\text{H})$	Pulse width High CP	Waveform 1	2.50		2.50		2.50		ns

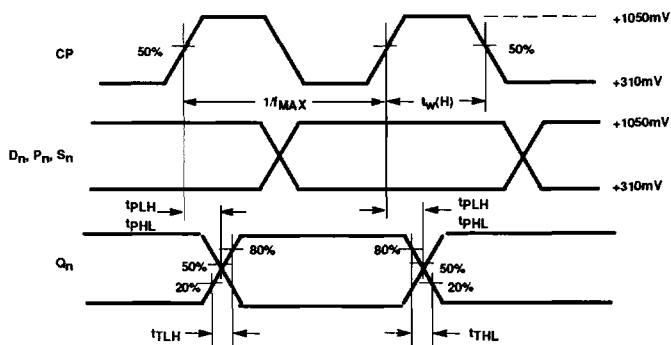
## NOTE:

For AC test setup information, see AC Testing, Chapter 2, Section 3.

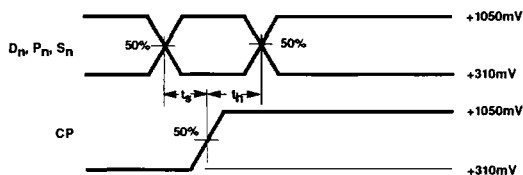
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## AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Data Setup and Hold Times

**NOTE:**

All power and signal voltages shifted up 2.0V for AC bench test purposes.

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## SHIFT FREQUENCY TEST CIRCUIT

