93452 / 93453
ISOPLANAR SCHOTTKY TTL MEMORY
1024×4-BIT PROGRAMMABLE READ ONLY MEMORY

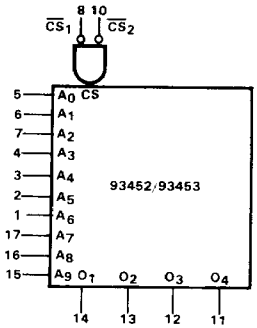
DESCRIPTION – The 93452 and 93453 are fully decoded high-speed 4096-bit field Programmable Read Only Memories organized 1024 words by four bits per word. The devices are identical except for the output stages. The 93452 has uncommitted collector outputs, while the 93453 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW.

- FULL MIL AND COMMERCIAL RANGES
- FAST ADDRESS ACCESS TIME — 35 ns TYP
- ORGANIZATION – 1024 WORDS X 4 BITS
- UNCOMMITTED COLLECTOR OUTPUTS – 93452
- 3-STATE OUTPUTS – 93453
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- 18-PIN DUAL IN-LINE PACKAGE
- REPLACES FOUR 256 X 4 PROMs

PIN NAMES

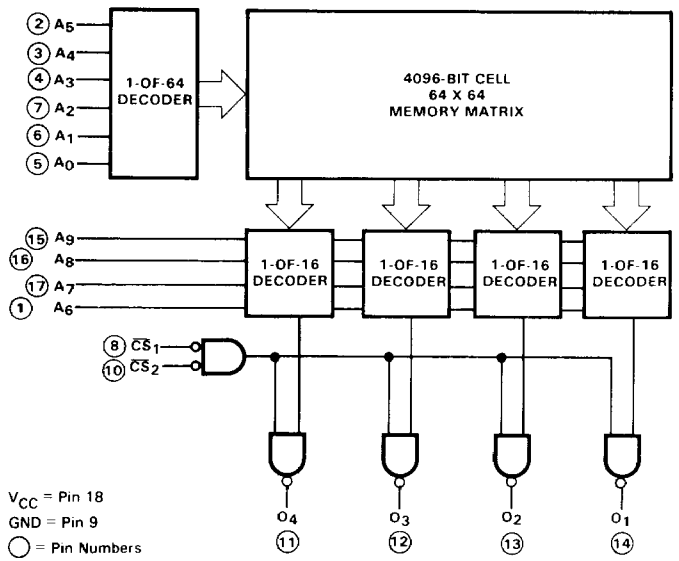
A_0 to A_9	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
O_1 to O_4	Data Outputs

LOGIC SYMBOL



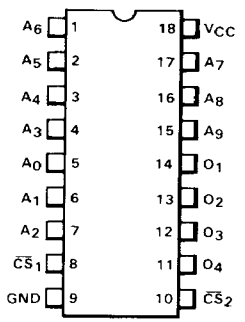
V_{CC} = Pin 18
GND = Pin 9

LOGIC DIAGRAM



V_{CC} = Pin 18
GND = Pin 9
◯ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



FUNCTIONAL DESCRIPTION – The 93452 and 93453 are bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by four bits per word. Open collector outputs are provided on the 93452 for use in wired-OR systems. The 93453 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Selects for both devices are active LOW; conversely, a HIGH (logic "1") on the $\overline{CS}_1$ or $\overline{CS}_2$ will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_9 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined below.

PROGRAMMING – The 93452 and 93453 are manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or buy any of the commercially available programmers which meet these specifications.

PROGRAMMING SPECIFICATIONS

CHARACTERISTIC	SYMBOL	MIN	RECOMMENDED VALUE	MAX	UNITS	COMMENTS
Address Input	V_{IH} V_{IL}	2.4 0	5.0 0	5.0 0.4	V V	Do not leave inputs open
Chip Select	$\overline{CS}_1$,$\overline{CS}_2$	2.4	5.0	5.0	V	Pin 8 or 10 or both
Programming Voltage Pulse	V_{OP}	20	21	21	V	Applied to output to be programmed
Programming Pulse Width	t_{pw}	0.05	0.18	50	ms	All bits can be programmed in $\leq$ 4.1 sec.
Duty Cycle, Programming Pulse			20	*	%	*Maximum duty cycle to maintain $T_C < 85°C$
Programming Pulse Rise Time	t_r	0.5	1.0	3.0	μs	
Number of Pulses Required		1	4	8		
Power Supply Voltage	V_{CC}	4.75	5.0	5.25	V	
Case Temperature	t_c		25	85	°C	
Programming Pulse Current Max.	I_{OP}			100	mA	If pulse generator is used, set current limit to this max value
Low V_{CC} Read	V_{CC}		4.4	5.0	V	Programming Read Verify

PROGRAMMING SEQUENCE – The Fairchild 93452/93453 may be programmed using the following method.

1. Apply the proper power, V_{CC} = 5.0 V, GND = 0 V.
2. Select the word to be programmed by applying the appropriate voltages to the address pins A_0 through A_9.
3. Enable the chip for programming by application of a HIGH (logic "1") to Chip Select ($\overline{CS}_1$), pin 8 or ($\overline{CS}_2$), pin 10 or both.
4. Apply the 21 V programming pulse to the output associated with the bit to be programmed. The other outputs may be left open or tied to any logic "1" (output HIGH), *i.e.*, 2.4 V to V_{CC}. Note that only one output may be programmed at a time.
5. To verify the logic "0" in the bit just programmed, remove the programming pulse from the output and sense it after applying logic "0"s to Chip Select inputs $\overline{CS}_1$ and $\overline{CS}_2$.
6. The above procedure is then repeated to program other bits on the chip.
7. See Chapter 6 for further details.

BOARD PROGRAMMING – To program a single PROM out of a group of "OR" tied memories the following procedure is required. (See Figure 1)

1. Connect all $\overline{CS}_2$ pins to ground.
2. Connect the outputs of a TTL Decoder (supplied by V_{CC} = +12.6 V, V_{EE} = +7.6 V) to the $\overline{CS}_1$ pins of the memories on the board.
3. Address the decoder such that the particular decoder output connected to the $\overline{CS}_1$ pin of the memory to be programmed will be LOW at +7.8 V. All the other decoder outputs will be HIGH at +10.6 V.
4. Apply the 21 V programming pulse to one group of "OR" tied outputs selected for programming; only the addressed bit in the +7.8 V selected memory will program, all other memories remain deselected (those with $\overline{CS}_1$ = +10.6 V).
5. To verify the logic "0" in the bit just programmed remove programming pulse and sense the "OR" tie after lowering the decoder supplies to the conventional V_{CC} = +5.0 V, V_{EE} = 0 V.

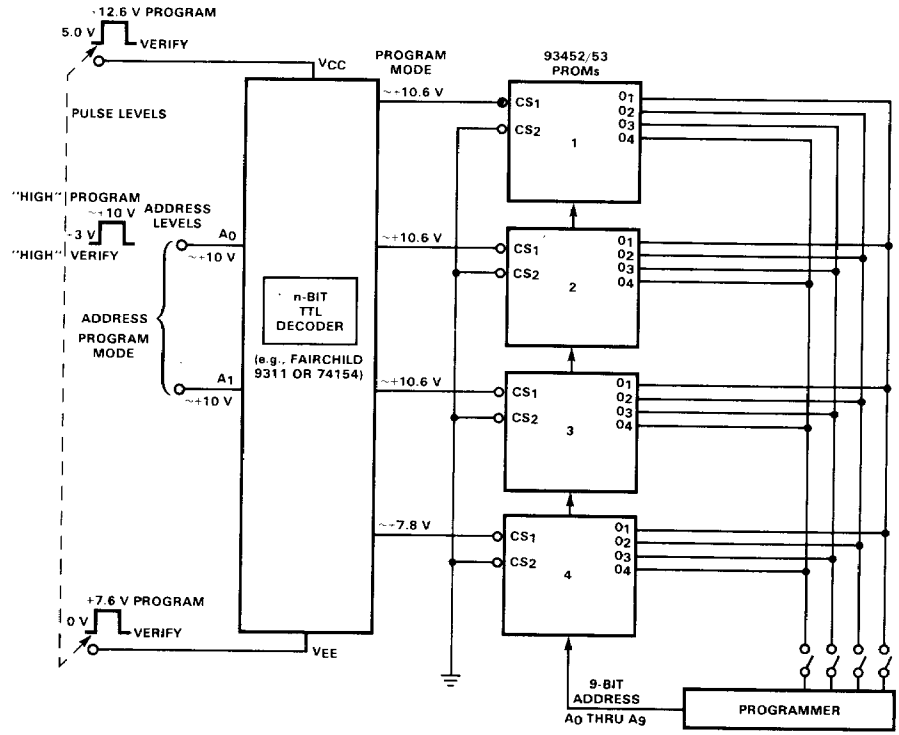


Figure 1

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC}	−0.5 V to +7.0 V
Input Voltages	−0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	−0.5 V to +5.5 V

GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
93452XC, 93453XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93452XM, 93453XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current (93452 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current (93452 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_9 = +10.8 V, A_2 = 10.8 V
V_{OH}	Output HIGH Voltage (93453 only)	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V −55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		120	170	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	55 55	ns ns	See Waveforms and Test Circuits
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

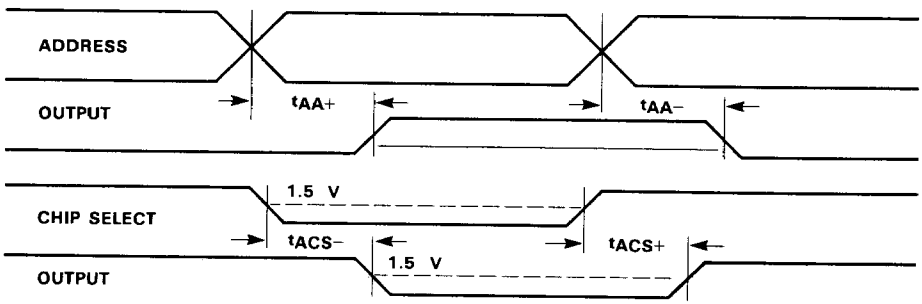
AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	70 70	ns ns	See Waveforms and Test Circuits
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note 1: Typical limits are at V_{CC} = 5.0 V, +25°C and max loading.

7

AC WAVEFORMS



AC TEST OUTPUT LOAD