OKI semiconductor

T-46-23-15

MSM514102

O K I SEMICONDUCTOR GROUP

4,194,304-WORD x 1-BIT DYNAMIC RAM: STATIC COLUMN MODE TYPE

GENERAL DESCRIPTION

The MSM514102 is a new generation dynamic RAM organized as 4,194,304 words by 1 bit. The technology used to fabricate the MSM514102 is OKI's CMOS silicon gate process technology. The device operates at a single + 5 V power supply. Its I/O pins are TTL compatible.

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FEATURES

- Silicon gate, quadruple polysilicon CMOS, 1-transistor memory cell
- 4,194,304 word by 1 bit organization
- 350 mil 26-pin plastic SOJ, 400 mil 20-pin plastic ZIP, 400 mil 18-pin plastic DIP
- Family organization

Family	Access Time (MAX)			Cycle Time (MIN)	Power Dissipation	
					Operating (MAX)	Standby (MAX)
	t_{RAC}	t_{AA}	t_{CAC}			
MSM514102-8	80 ns	40 ns	20 ns	160 ns	495 mW	5.5 mW (MOS level)
MSM514102-8A	80 ns	40 ns	25 ns	160 ns	495 mW	
MSM514102-10	100 ns	50 ns	25 ns	190 ns	440 mW	

- Single + 5 V supply, ± 10% tolerance
- Input: TTL compatible
- Output: TTL compatible, tristate, nonlatch
- Refresh: 1024 cycles/16 ms
- Common I/O capability using "Early Write" operation
- $\overline{CS}$ before $\overline{RAS}$ refresh, $\overline{CS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability
- Multi bit test mode capability
- Built-in V_{BB} generator circuit

PIN CONFIGURATION (TOP VIEW)

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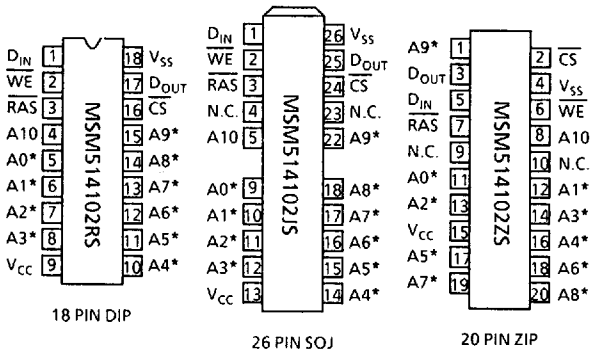

* Refresh Address

Pin Names	Function
A0 to A10	Address Input
$\overline{RAS}$	Row Address Strobe
$\overline{CS}$	Chip Select Input
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable
V_{CC}	Power Supply < +5V>
V_{SS}	Ground <0V>
N.C.	No Connection

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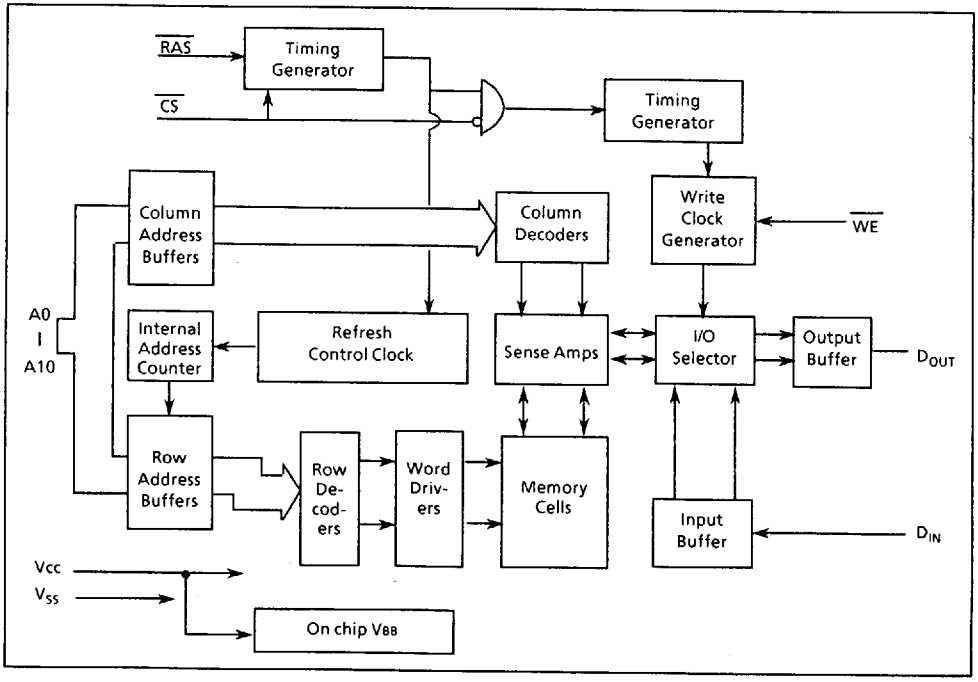
FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Conditions	Value	Unit	Note
Voltage on any pin relative to V_{SS}	VT	Ta = 25 °C	− 1.0 to + 7.0	V	1
Short circuit output current	Ios	Ta = 25 °C	50	mA	1
Power dissipation	P_D	Ta = 25 °C	1	W	1
Operating temperature	Topr	−	0 to + 70	°C	1
Storage temperature	Tstg	−	− 55 to + 150	°C	1

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RECOMMENDED OPERATING CONDITIONS

(Ta = 0 to + 70°C)

Parameter	Symbol	MIN	TYP	MAX	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	2
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	−	6.5	V	2
Input low voltage	V_{IL}	− 1.0	−	0.8	V	2

Notes: 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2. All voltages are referenced to V_{SS}.

DC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C)

Parameter	Symbol	Conditions		MSM 514102-8		MSM 514102-8A		MSM 514102-10		Unit	Note
				MIN	MAX	MIN	MAX	MIN	MAX		
Output high voltage	V_{OH}	I_{OH} = −5.0 mA		2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	I_{OL} = 4.2 mA		0	0.4	0	0.4	0	0.4	V	
Input leakage current	I_{LI}	0 V ≤ VI ≤ 6.5V; all other pins not under test = 0 V		−10	10	−10	10	−10	10	μA	
Output leakage current	I_{LO}	D_{OUT} = disable 0 V ≤ VO ≤ 5.5 V		−10	10	−10	10	−10	10	μA	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$, $\overline{CS}$ cycling, t_{RC} = min		−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IH} D_{OUT} = Hz	TTL	−	2	−	2	−	2	mA	
			MOS	−	1	−	1	−	1	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CS}$ = V_{IH} t_{RC} = min		−	90	−	90	−	80	mA	1, 2
Power supply current (Standby)	I_{CC5}	$\overline{RAS}$ = V_{IH} $\overline{CS}$ = V_{IL} D_{OUT} = enable		−	5	−	5	−	5	mA	1
Average power supply current ($\overline{CS}$ before $\overline{RAS}$ refresh)	I_{CC6}	$\overline{RAS}$ cycling, $\overline{CS}$ before $\overline{RAS}$		−	90	−	90	−	80	mA	1
Average power supply current (Static column mode)	I_{CC9}	$\overline{RAS}$ = V_{IL} $\overline{CS}$ = V_{IL} t_{SC} = min		−	80	−	80	−	70	mA	1

Notes: 1. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with the output open.

2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}.

CAPACITANCE

(Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Conditions	TYP	MAX	Unit
Input capacitance (A0 to A10, D_{IN})	C_{IN1}	−	−	6	pF
Input capacitance ($\overline{RAS}$, $\overline{CS}$, $\overline{WE}$)	C_{IN2}	−	−	7	pF
Output capacitance (D_{OUT})	C_{OUT}	−	−	7	pF

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AC CHARACTERISTICS

(V_{CC} = 5 V ± 10%, Ta = 0 to +70°C) Note 1, 2, 3, 11, 12

Parameter	Symbol	MSM 514102-8		MSM 514102-8A		MSM 514102-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	160	–	160	–	190	–	ns	
Read/write cycle time	t_{RWC}	185	–	190	–	220	–	ns	
Static column mode cycle time	t_{SC}	45	–	45	–	55	–	ns	
Static column mode read/write cycle time	t_{SRWC}	70	–	70	–	80	–	ns	
Access time from $\overline{RAS}$	t_{RAC}	–	80	–	80	–	100	ns	4, 5, 6
Access time from $\overline{CS}$	t_{CAC}	–	20	–	25	–	25	ns	4. 5
Access time from column address	t_{AA}	–	40	–	40	–	50	ns	4. 6, 7
Access time from last write	t_{ALW}	–	75	–	75	–	95	ns	4, 7
Data output enable time reference to $\overline{WE}$	t_{OW}	–	20	–	25	–	25	ns	
Output low impedance time from $\overline{CS}$	t_{CLZ}	0	–	0	–	0	–	ns	4
Data output hold time reference to column address	t_{AOH}	5	–	5	–	5	–	ns	
Data output hold time reference to $\overline{WE}$	t_{WOH}	0	–	0	–	0	–	ns	
Output buffer turn-off delay time	t_{OFF}	0	20	0	20	0	25	ns	8
Transition time	t_T	3	50	3	50	3	50	ns	3
Refresh period	t_{REF}	–	16	–	16	–	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	70	–	70	–	80	–	ns	
$\overline{RAS}$ pulse width	t_{RAS}	80	10,000	80	10,000	100	10,000	ns	
$\overline{RAS}$ pulse width (Static column mode)	t_{RASC}	80	100,000	80	100,000	100	100,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	20	–	25	–	25	–	ns	
$\overline{CS}$ precharge time	t_{CP}	10	–	10	–	10	–	ns	
$\overline{CS}$ pulse width	t_{CS}	20	100,000	25	100,000	25	100,000	ns	
$\overline{CS}$ hold time	t_{CSH}	80	–	80	–	100	–	ns	
$\overline{CS}$ to $\overline{RAS}$ precharge time	t_{CRP}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ delay time	t_{RCD}	22	60	25	55	25	75	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	17	40	20	40	20	50	ns	6
Row address set-up time	t_{ASR}	0	–	0	–	0	–	ns	
Row address hold time	t_{RAH}	12	–	15	–	15	–	ns	
Column address set-up time	t_{ASC}	0	–	0	–	0	–	ns	
Column address hold time	t_{CAH}	15	–	15	–	20	–	ns	

AC CHARACTERISTICS (Continued)

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Parameter	Symbol	MSM 514102-8		MSM 514102-8A		MSM 514102-10		Unit	Note
		MIN	MAX	MIN	MAX	MIN	MAX		
Column address hold time reference to $\overline{RAS}$ (WRITE CYCLE)	t_{AWR}	60	–	60	–	75	–	ns	
Column address hold time reference to $\overline{RAS}$	t_{AR}	95	–	95	–	115	–	ns	
Column address to $\overline{RAS}$ lead time	t_{RAL}	40	–	40	–	50	–	ns	
Column address hold time reference to $\overline{RAS}$ precharge	t_{AH}	10	–	10	–	10	–	ns	
Column address hold time reference to $\overline{WE}$	t_{AHLW}	75	–	75	–	95	–	ns	
Last write to column address delay time	t_{LWAD}	20	35	20	35	25	45	ns	7
Read command set-up time	t_{RCS}	0	–	0	–	0	–	ns	
Read command hold time reference to $\overline{CS}$	t_{RCH}	0	–	0	–	0	–	ns	9
Read command hold time reference to $\overline{RAS}$	t_{RRH}	10	–	10	–	10	–	ns	9
Write command set-up time	t_{WCS}	0	–	0	–	0	–	ns	10
Write command pulse width	t_{WP}	15	–	15	–	20	–	ns	
Write command hold time from $\overline{RAS}$	t_{WCR}	60	–	60	–	75	–	ns	
Write invalid time	t_{WI}	10	–	10	–	10	–	ns	
Write command hold time (Dout disable)	t_{WH}	0	–	0	–	0	–	ns	10
Write command to $\overline{CS}$ lead time	t_{CWL}	20	–	25	–	25	–	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	20	–	25	–	25	–	ns	
$\overline{CS}$ to $\overline{WE}$ delay time	t_{CWD}	20	–	25	–	25	–	ns	10
Column address to $\overline{WE}$ delay time	t_{AWD}	40	–	40	–	50	–	ns	10
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	80	–	80	–	100	–	ns	10
Data-in set-up time	t_{DS}	0	–	0	–	0	–	ns	
Data-in hold time	t_{DH}	15	–	15	–	20	–	ns	
Data-in hold time from $\overline{RAS}$	t_{DHR}	60	–	60	–	75	–	ns	
$\overline{CS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ set-up time ($\overline{CS}$ before $\overline{RAS}$)	t_{CSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{CS}$ hold time ($\overline{CS}$ before $\overline{RAS}$)	t_{CHR}	20	–	20	–	20	–	ns	
$\overline{CS}$ precharge time (Refresh counter test)	t_{CPT}	40	–	40	–	50	–	ns	
$\overline{WE}$ to $\overline{RAS}$ precharge time ($\overline{CS}$ before $\overline{RAS}$)	t_{WRP}	10	–	10	–	10	–	ns	
$\overline{WE}$ hold time from $\overline{RAS}$ ($\overline{CS}$ before $\overline{RAS}$)	t_{WRH}	20	–	20	–	20	–	ns	
$\overline{RAS}$ to $\overline{WE}$ set-up time (Test mode)	t_{WSR}	10	–	10	–	10	–	ns	
$\overline{RAS}$ to $\overline{WE}$ hold time (Test mode)	t_{WHR}	20	–	20	–	20	–	ns	

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Notes: 1. An initial pause of 200 μs is required after power-up followed by a minimum of eight initialization cycles ($\overline{RAS}$ only refresh cycle or $\overline{CS}$ before $\overline{RAS}$ refresh cycle) before proper device operation is achieved.
In case of using internal refresh counter, a minimum of eight $\overline{CS}$ before $\overline{RAS}$ initialization cycles is required.

2. The AC characteristics assume $t_T = 5$ ns.

3. V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring of input signals. Also, transition times are measured between V_{IH} and V_{IL}.

4. Measured with a load circuit equivalent to 2TTL loads and 100pF.

5. Operation within the t_{RCD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RCD} (max.) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max.) limit, then access time is controlled exclusively by t_{CAC}.

6. Operation within the t_{RAD} (max.) limit insures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

7. Operation within the t_{LWAD} (max.) limit insures that t_{ALW} (max.) can be met. t_{LWAD} (max.) is specified as a reference point only; if t_{LWAD} is greater than the specified t_{LWAD} (max.) limit, then access time is controlled exclusively by t_{AA}.

8. t_{OFF} (max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

9. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

10. t_{WCS}, t_{WH}, t_{CWD}, t_{RWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geqq t_{WCS}$ (min.) and $t_{WH} \geqq t_{WH}$ (min.), the cycle is an early write cycle and the data out will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geqq t_{CWD}$ (min.), $t_{RWD} \geqq t_{RWD}$ (min.) and $t_{AWD} \geqq t_{AWD}$ (min.), the cycle is read/write cycle and data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

11. The test mode is initiated by performing a $\overline{WE}$ and $\overline{CS}$ before $\overline{RAS}$ refresh cycle. This mode is latched and remain in effect until the exit cycle is generated.
The test mode specified in this data sheet is 8-bit parallel test function.
RA10, CA10 and CA0 are not used. In a read cycle, if all internal bits are equal, the data output pin will indicate a high level. If any internal bits are not equal, then data output pin will indicate a low level.
The test mode is cleared and the memory device returned to its normal operational state by performing a $\overline{RAS}$ only refresh cycle or a $\overline{CS}$ before $\overline{RAS}$ refresh cycle.

12. In a test mode read cycle, the value of access time parameters is delayed for 5 ns for the specified value. These parameters should be specified in test mode cycles by adding the above value to the specified value in this data sheet.

READ CYCLE

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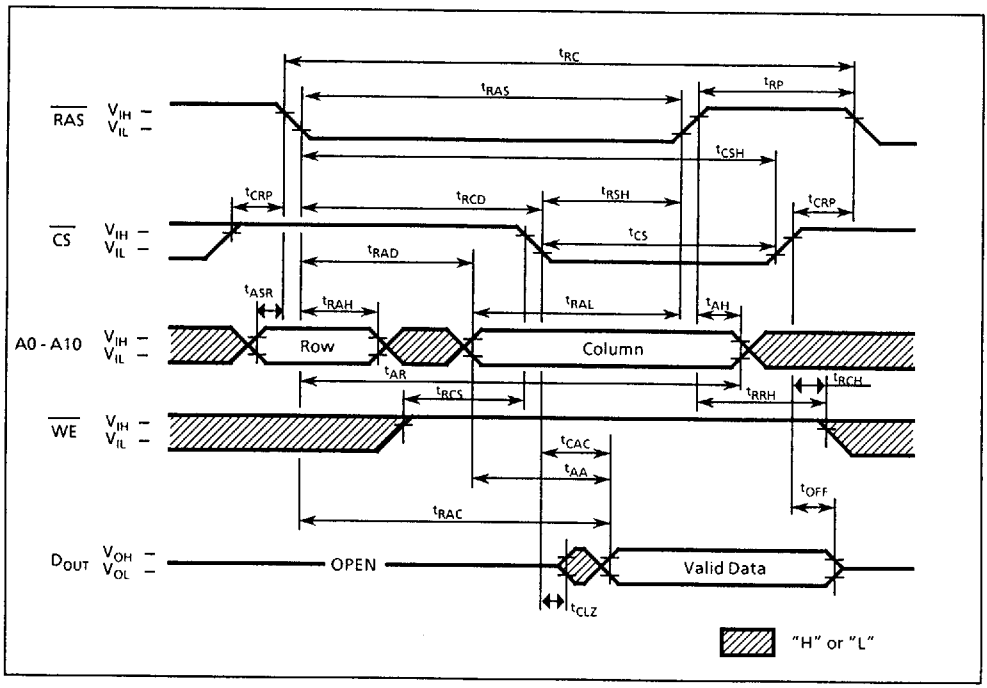
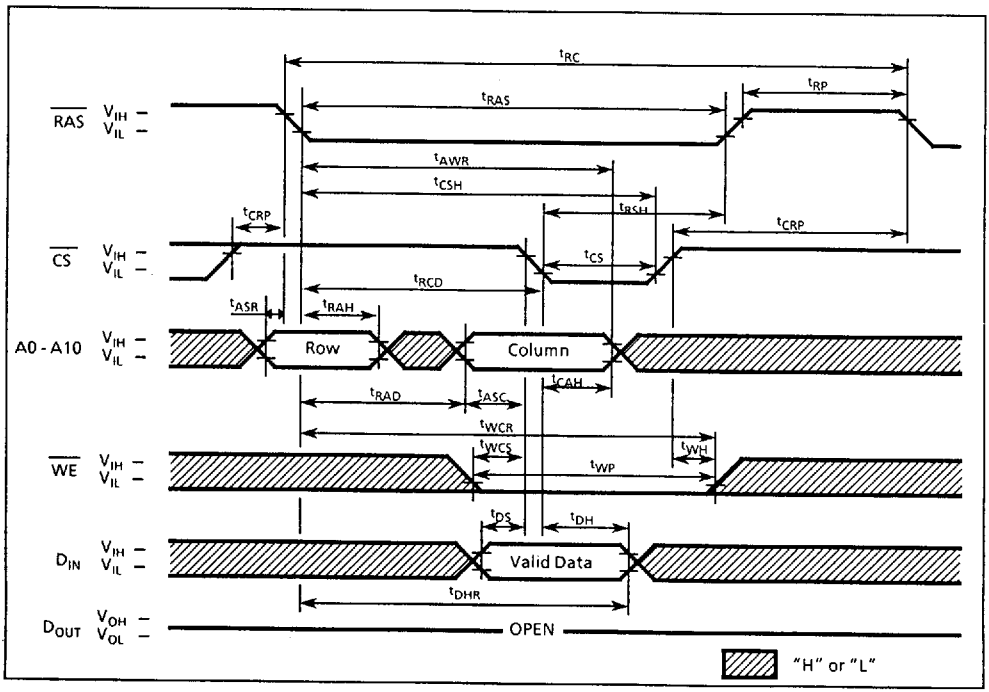


WRITE CYCLE (EARLY WRITE)



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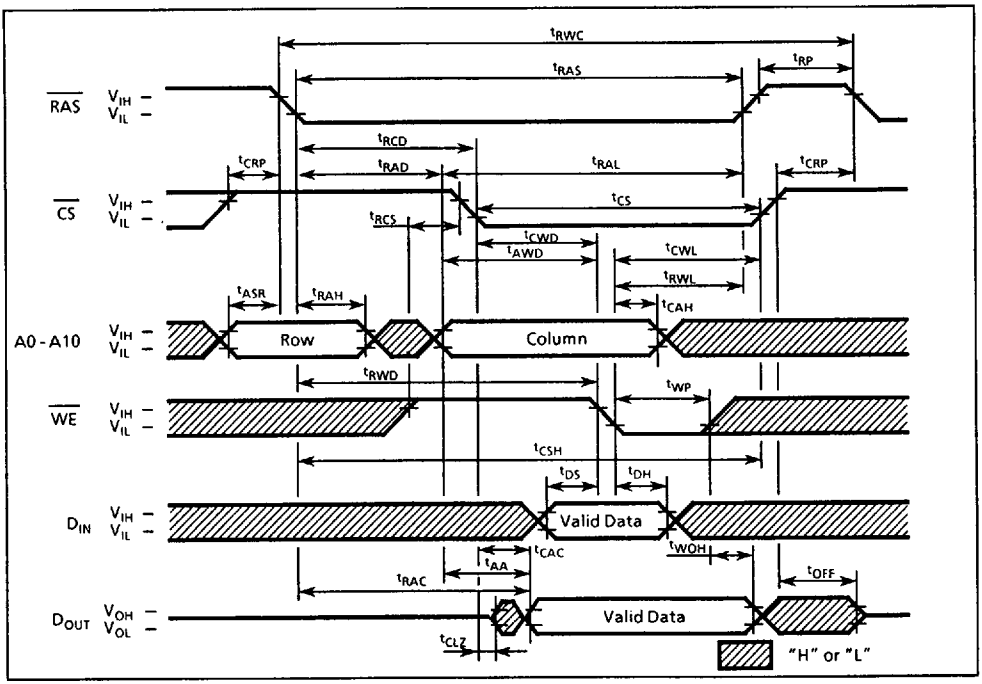
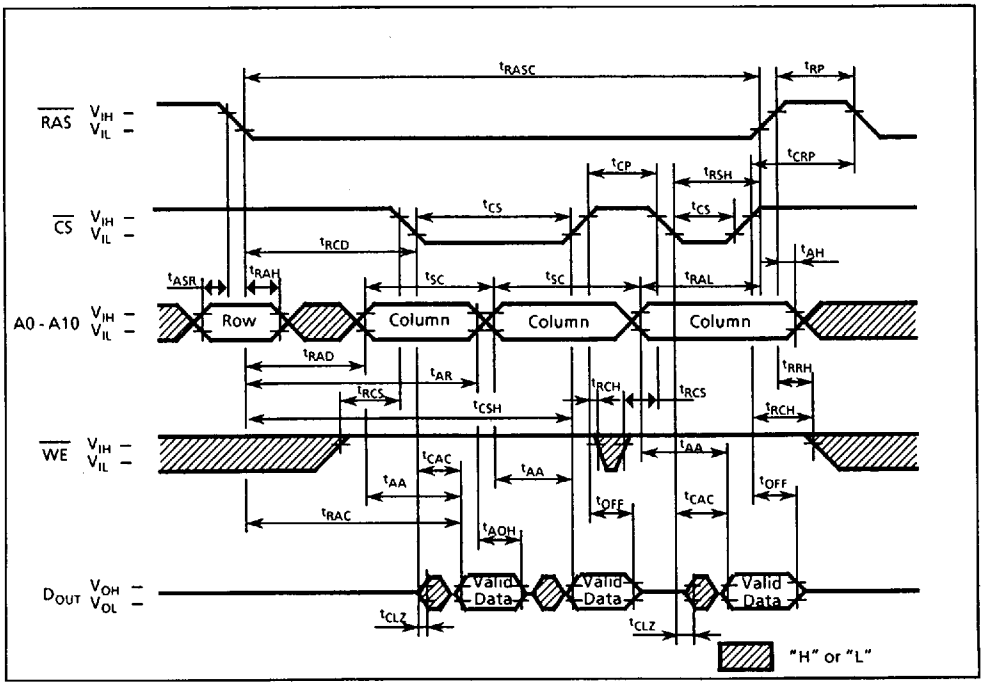
READ/WRITE CYCLE



STATIC COLUMN MODE READ CYCLE



STATIC COLUMN MODE WRITE CYCLE (EARLY WRITE)

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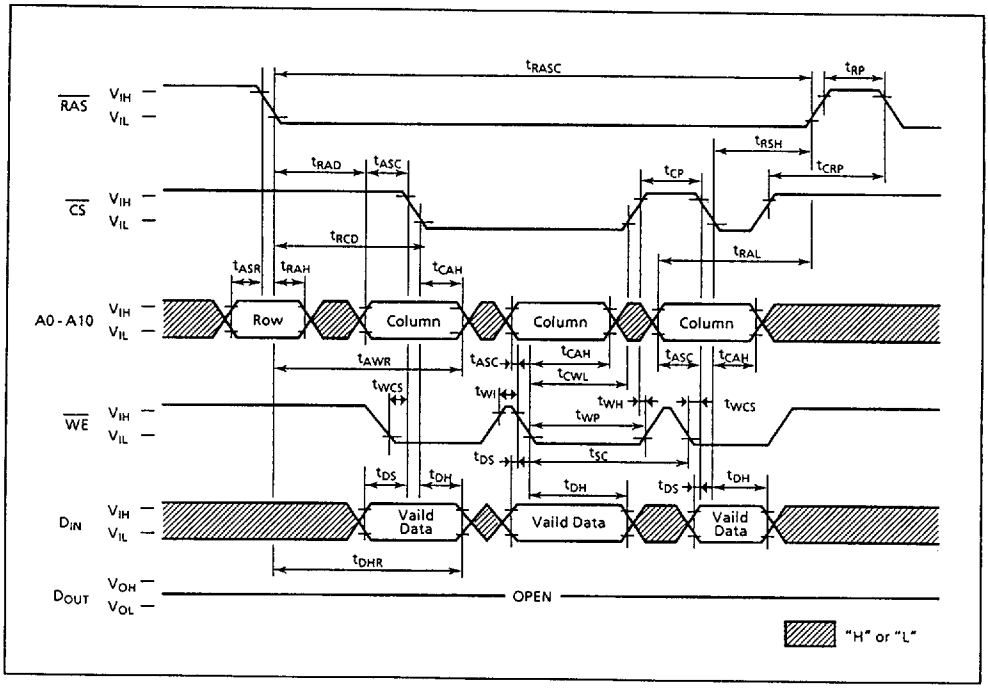
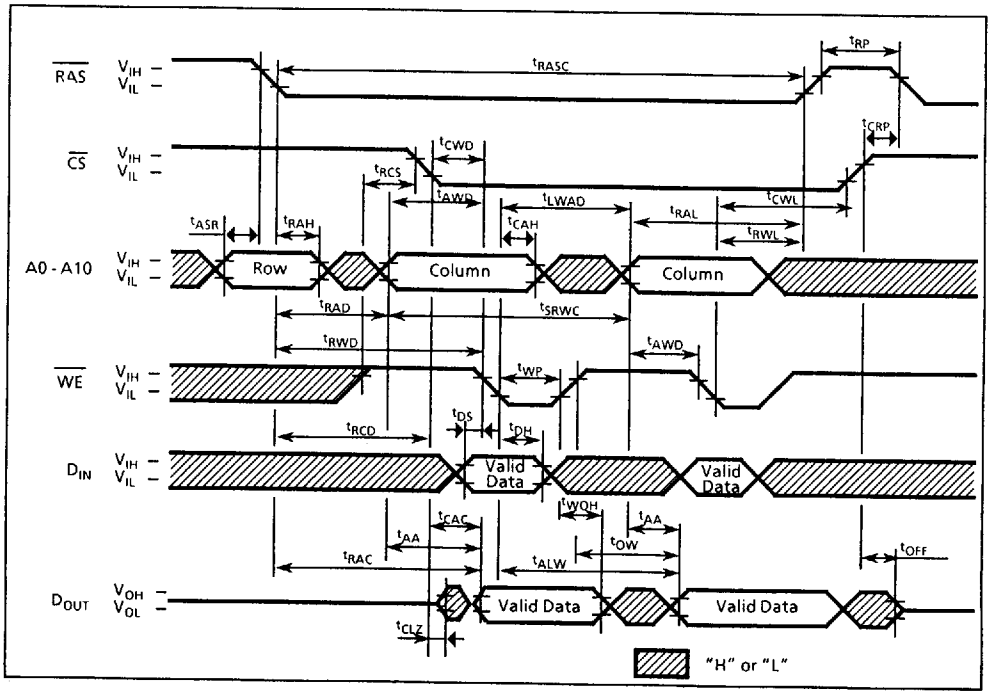


STATIC COLUMN MODE READ/WRITE CYCLE



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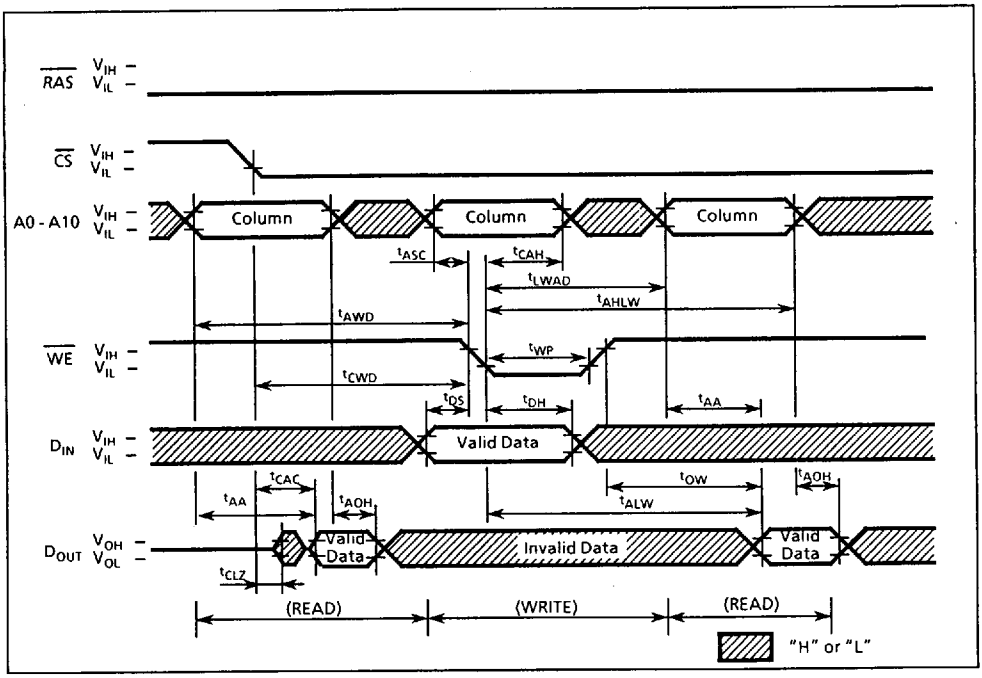
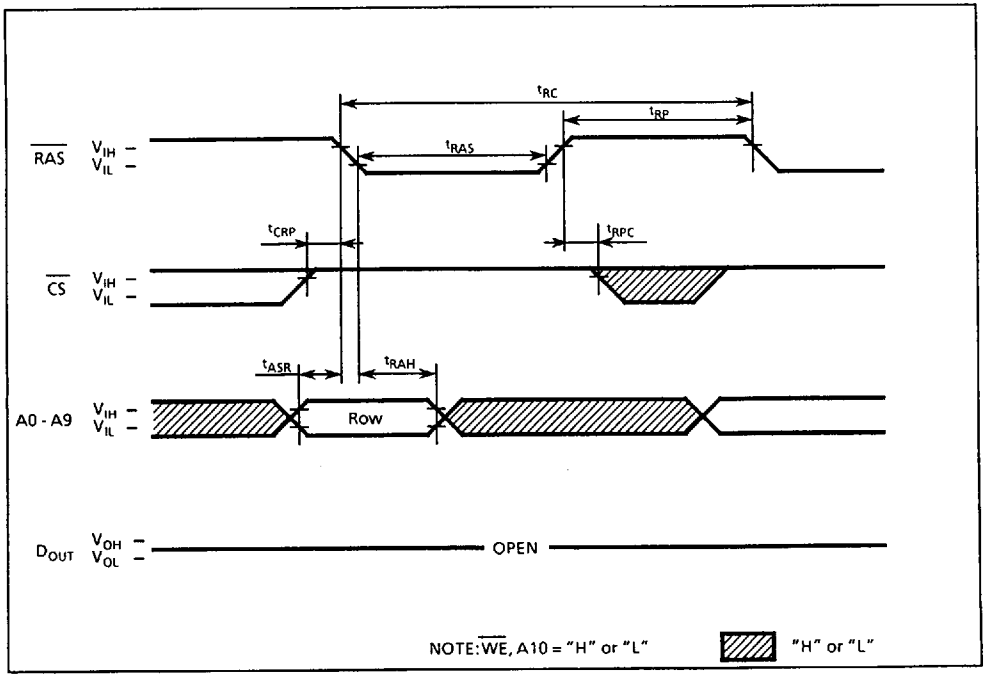
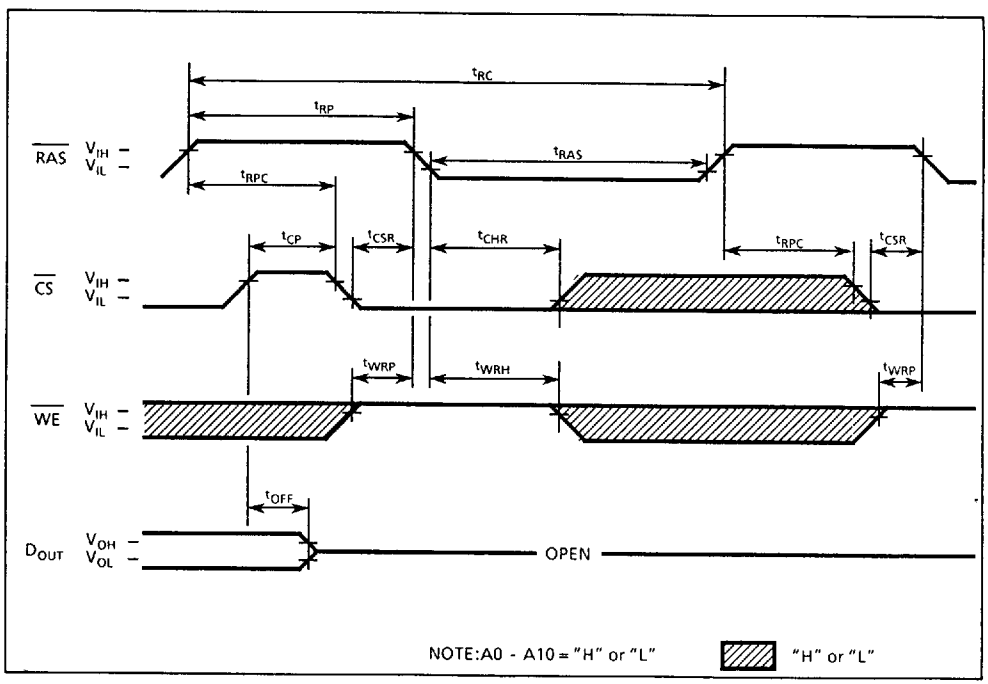
STATIC COLUMN MODE READ/WRITE MIXED CYCLE



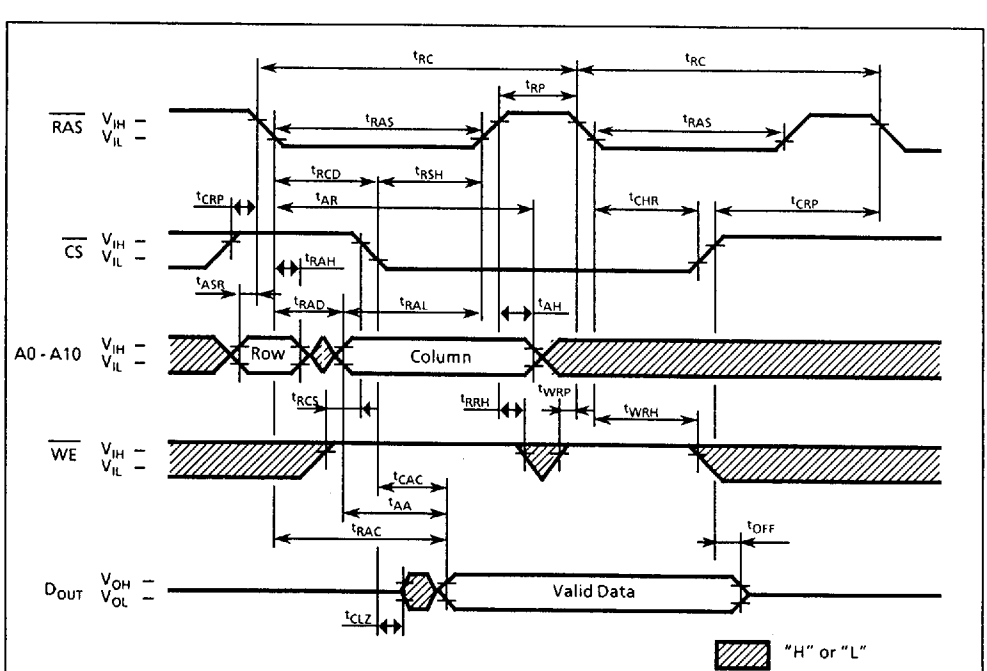
RAS ONLY REFRESH CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ AUTO REFRESH CYCLE



HIDDEN REFRESH READ CYCLE



HIDDEN REFRESH WRITE CYCLE

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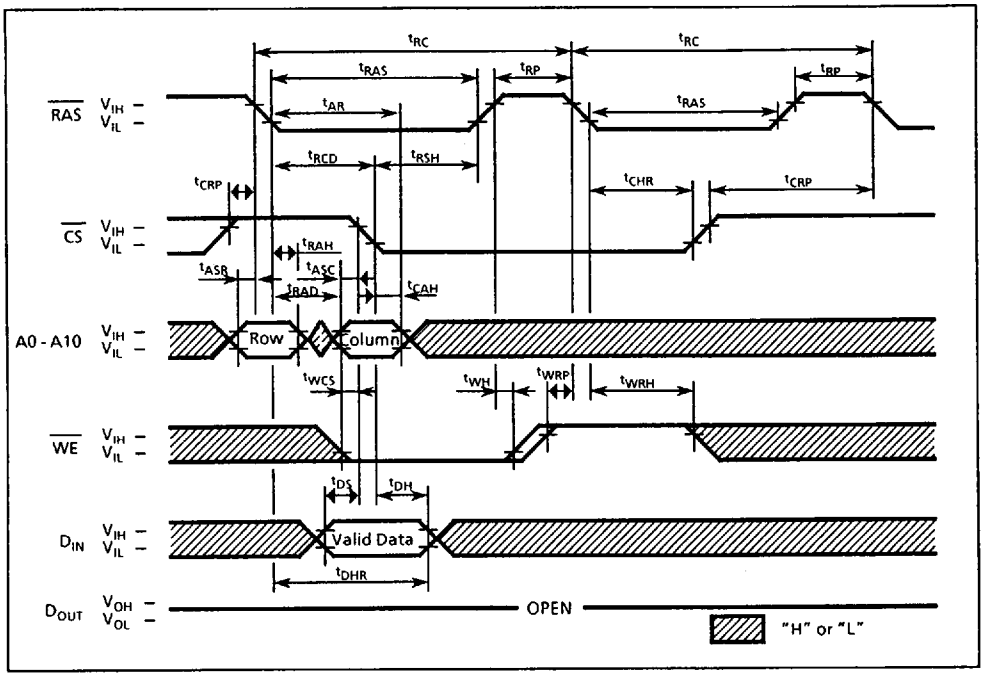
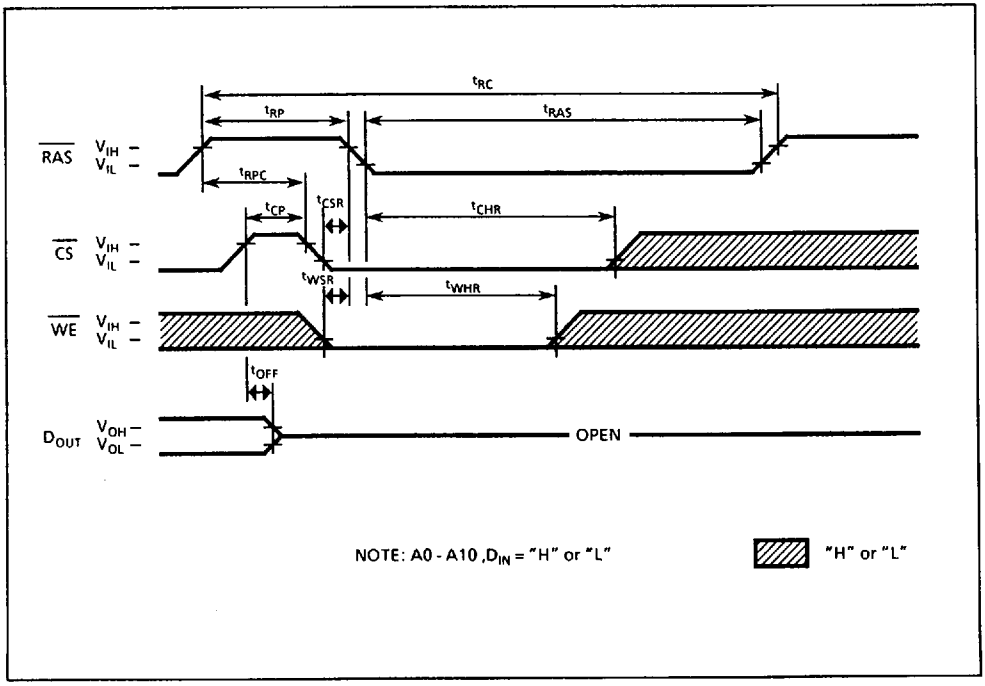


TEST MODE INITIATE CYCLE



$\overline{CS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE