

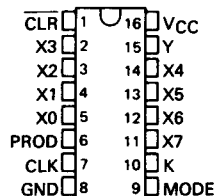
# SN54LS384, SN74LS384

## 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

D2419, JANUARY 1981 — REVISED MARCH 1988

- Two's-Complement Multiplication
- Magnitude Only Multiplication
- Cascadable for Any Number of Bits
- 8-Bit Parallel Multiplicand Data Input
- Serial Multiplier Data Input
- Serial Data Output for Multiplication Product
- 40 MHz Typical Maximum Clock Frequency

SN54LS384 . . . J PACKAGE  
SN74LS384 . . . N PACKAGE  
(TOP VIEW)



### description

The 'LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's-complement form to produce a two's-complement product without external correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. These X latches are controlled via the clear input. When the clear input is low, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is high, the latches are closed and are insensitive to X input changes.

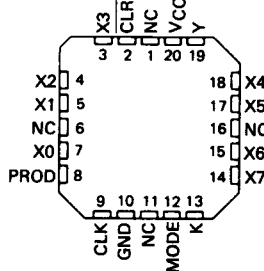
The multiplier word data is passed by the Y input in a serial bit stream, least significant bit first. The product is clocked out the PROD output, least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an (m + n)-bit product. The 'LS384 must be clocked for m + n clock cycles to produce this two's complement product. The n-bit multiplier (Y-input) sign bit data must be extended for the remaining m bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The PROD output of one device is connected to the K input of the succeeding device when cascading. The mode input is used to indicate which device contains the most significant bit. The mode input is wired high or low depending on the position of the 8-bit slice in the total X word length. The device with the most significant bit is wired low and all lower order bit packages are wired high.

The SN54LS384 will be characterized for operation over the full military temperature range from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74LS384 will be characterized for operation from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

SN54LS384 . . . FK PACKAGE  
(TOP VIEW)



NC - No internal connection

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PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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# SN54LS384, SN74LS384

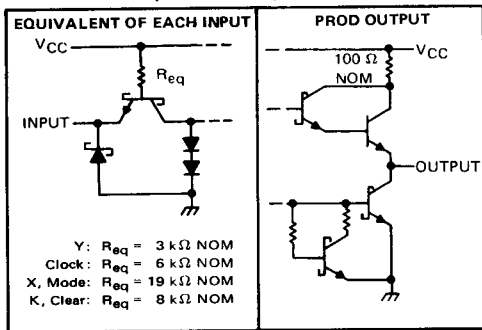
## 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

FUNCTION TABLE

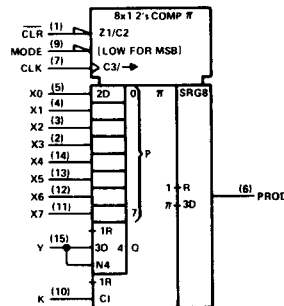
| INPUTS |     |       |   | INTERNAL<br>$Y_{-1}$ | OUTPUT<br>PROD | FUNCTION   |
|--------|-----|-------|---|----------------------|----------------|--|
| CLR    | CLK | $X_i$ | Y |                      |                |  |
| L      | X   | Data  | X | L                    | L              | Load new multiplicand and clear internal sum and carry registers |
| H      | ↑   | X     | L | L                    | Output         | Shift sum register   |
| H      | ↑   | X     | L | H                    | per            | Add multiplicand to sum register and shift                       |
| H      | ↑   | X     | H | L                    | Booth's        | Subtract multiplicand from sum register and shift                |
| H      | ↑   | X     | H | H                    | algorithm      | Shift sum register   |

H = high-level, L = low-level, X = irrelevant, ↑ = low-to-high-level transition

### schematics of inputs and outputs



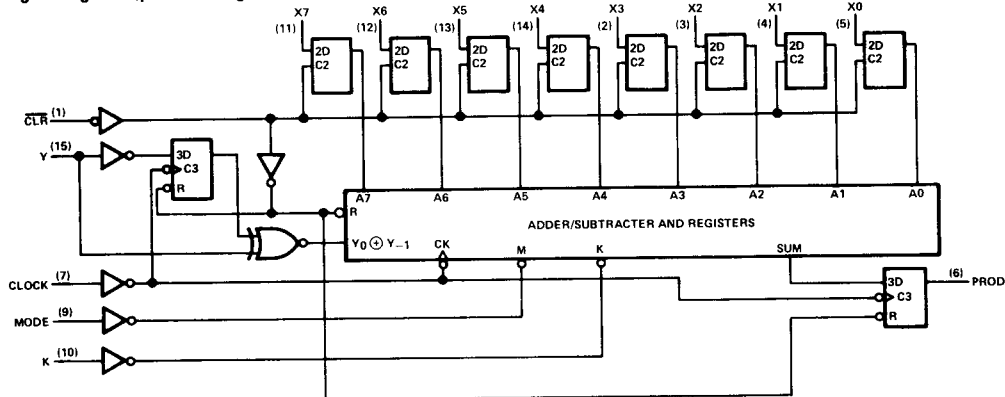
### logic symbol†



†This symbol is in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

### logic diagram (positive logic)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

|   |                |
|---|----------------|
| Supply voltage, $V_{CC}$ (see Note 1)           | 7 V            |
| Input voltage (see Note 2)                      | 5.5 V          |
| Operating free-air temperature range: SN54LS384 | -55°C to 125°C |
| SN74LS384                                       | 0°C to 70°C    |
| Storage temperature range                       | -65°C to 150°C |

NOTES: 1. Voltage values are with respect to network ground terminal.  
 2. Input voltages must be zero or positive with respect to network ground terminal.

# SN54LS384, SN74LS384

## 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

### recommended operating conditions

|   |                  | SN54LS384 |     |     | SN74LS384 |     |      | UNIT    |       |
|---|------------------|-----------|-----|-----|-----------|-----|------|---------|-------|
|   |                  | MIN       | NOM | MAX | MIN       | NOM | MAX  |         |       |
| Supply voltage, $V_{CC}$                        |                  | 4.5       | 5   | 5.5 | 4.75      | 5   | 5.25 | V       |       |
| High-level output current, $I_{OH}$             |                  |           |     |     | -400      |     |      | $\mu$ A |       |
| Low-level output current, $I_{OL}$              |                  |           |     |     | 4         |     |      | 8 mA    |       |
| Clock frequency, $f_{clock}$                    |                  |           |     |     | 0         |     |      | 25 MHz  |       |
| Setup time, $t_{SU}$                            | Y before Clock † | 45        |     |     | 38        |     |      | ns      |       |
|   | K before Clock † | 30        |     |     | 24        |     |      |         |       |
|   | X before Clear † | 23        |     |     | 19        |     |      |         |       |
| Clear inactive-state set up time before Clock † |                  | 30        |     |     | 20        |     |      | ns      |       |
| Hold time, $t_H$                                | Y after Clock †  | 0         |     |     | 0         |     |      |         |       |
|   | K after Clock †  | 0         |     |     | 0         |     |      |         |       |
|   | X after Clear †  | 2         |     |     | 2         |     |      |         |       |
| Pulse width, $t_W$                              | Clock high       | 20        |     |     | 20        |     |      | ns      |       |
|   | Clock low        | 20        |     |     | 20        |     |      |         |       |
|   | Clear low        | 38        |     |     | 33        |     |      |         |       |
| Operating free-air temperature, $T_A$           |                  | -55       |     |     | 125       |     |      | 0       | 70 °C |

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER |  | TEST CONDITIONS†   | SN54LS384 |      |     | SN74LS384 |      |     | UNIT    |
|-----------|--|--|-----------|------|-----|-----------|------|-----|---------|
|           |  |  | MIN       | TYP‡ | MAX | MIN       | TYP‡ | MAX |         |
| $V_{IH}$  | High-level input voltage               |  | 2         |      |     | 2         |      |     | V       |
| $V_{IL}$  | Low-level input voltage                |  |           |      |     | 0.7       |      |     | 0.8 V   |
| $V_{IK}$  | Input clamp voltage                    | $V_{CC} = \text{MIN}, I_I = -18 \text{ mA}$  |           |      |     | -1.5      |      |     | -1.5 V  |
| $V_{OH}$  | High-level output voltage              | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, V_{OH} = -400 \mu\text{A}$                        | 2.5       | 3.4  |     | 2.7       | 3.4  |     | V       |
| $V_{OL}$  | Low-level output voltage               | $V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OL} = 4 \text{ mA}$<br>$I_{OL} = 8 \text{ mA}$ | 0.25      | 0.4  |     | 0.25      | 0.4  |     | 0.5 V   |
| $I_I$     | Input current at maximum input voltage | $V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$   |           |      |     | 1         |      |     | 1 mA    |
| $I_{IH}$  | High-level input current               | X, Mode  |           |      |     | 20        |      |     | $\mu$ A |
|           |  | K, Clear   |           |      |     | 30        |      |     |         |
|           |  | Clock  |           |      |     | 40        |      |     |         |
|           |  | Y  |           |      |     | 80        |      |     |         |
| $I_{IL}$  | Low-level input current                | X, Mode  |           |      |     | -0.48     |      |     | mA      |
|           |  | K, Clear   |           |      |     | -1.2      |      |     |         |
|           |  | Clock  |           |      |     | -1.6      |      |     |         |
|           |  | Y  |           |      |     | -3.2      |      |     |         |
| $I_{OS}$  | Short-circuit output current§          | $V_{CC} = \text{MAX}$  | -20       | -100 |     | -20       | -100 |     | 91 mA   |
| $I_{CC}$  | Supply current                         | $V_{CC} = \text{MAX},$ See Note 3  | 91        | 132  |     | 91        | 132  |     | mA      |

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at  $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$ .

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3:  $I_{CC}$  is measured with the clear input grounded and all other inputs and outputs open.

### switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ \text{C}$

| PARAMETER |   | TEST CONDITIONS            | MIN | TYP | MAX | UNIT |
|-----------|---|----------------------------|-----|-----|-----|------|
| $f_{max}$ | Maximum clock frequency                                     |                            |     | 25  | 40  |      |
| $t_{PLH}$ | Propagation delay time, low-to-high-level output from clock | $C_L = 15 \text{ pF},$     |     | 15  | 23  | ns   |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from clock | $R_L = 2 \text{ k}\Omega,$ |     | 15  | 23  | ns   |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output from clear | See Note 4                 |     | 17  | 25  | ns   |

NOTE 4: Load circuits and voltage waveforms are shown in Section 1.

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70-100 Source (continued)

# SN54LS384, SN74LS384 8-BIT BY 1-BIT TWO'S-COMPLEMENT MULTIPLIERS

## TYPICAL APPLICATION DATA

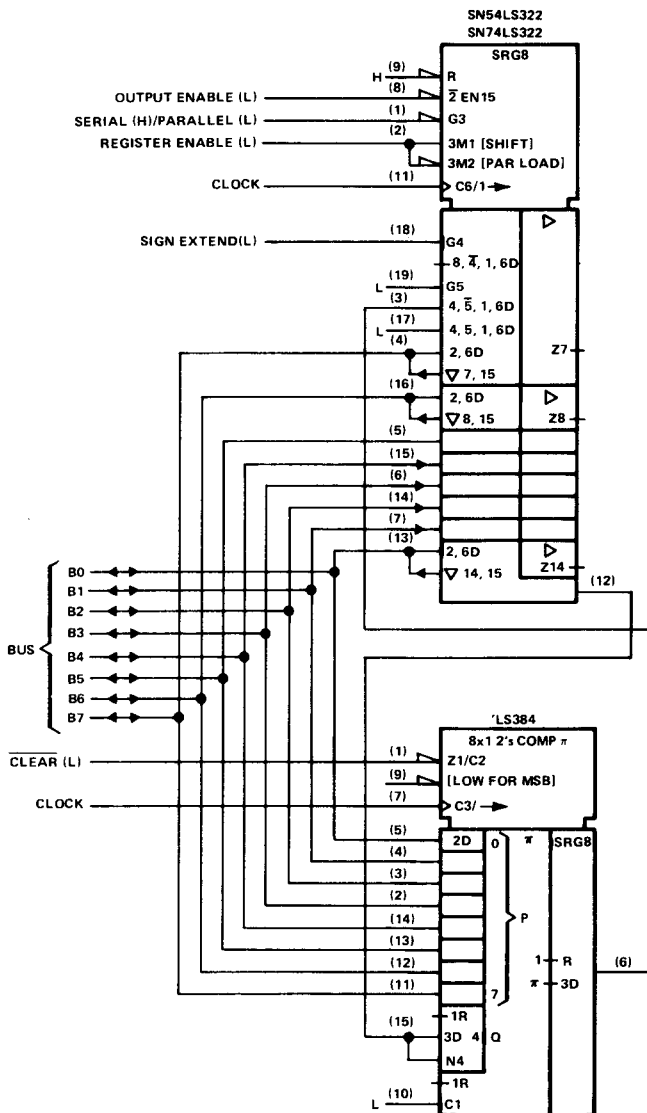


FIGURE 2—8-BIT BY 8-BIT MULTIPLIER, BUS ORGANIZED,  
WITH 8-BIT TRUNCATED PRODUCT

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