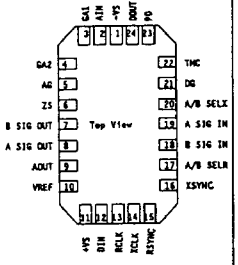
μ-LAW SINGLE CHIP CODEC WITH FILTERS

The Fujitsu MB6024 is a single chip Codec with Filters Fabricated with a silicon gate CMOS process. It has been designed to meet the needs for per channel voice frequency Codecs used in PCM systems. Both the transmit and receive sections are incorporated into a single chip.

CERAMIC PACKAGE
LCC-24C-F03

- Transmit High-pass and Low-pass Filters
- Receive Low-pass Filter with SinX/X Correction
- Anti-aliasing Filter
- Conformance to the CCITT and AT&T Specification
- Synchronous and Asynchronous Operation
- Serial Data Rates of 64 kHz to 3.152 MHz
- PLL Circuit as Internal Clock Generator
- Internal Voltage Reference
- Internal Auto-zero Circuit
- TTL Compatible Digital Interface
- Zero Code Suppression is Pin-selectable
- μ-Law with signaling
- Package
  24-pad Ceramic LCC package

PIN ASSIGNMENT



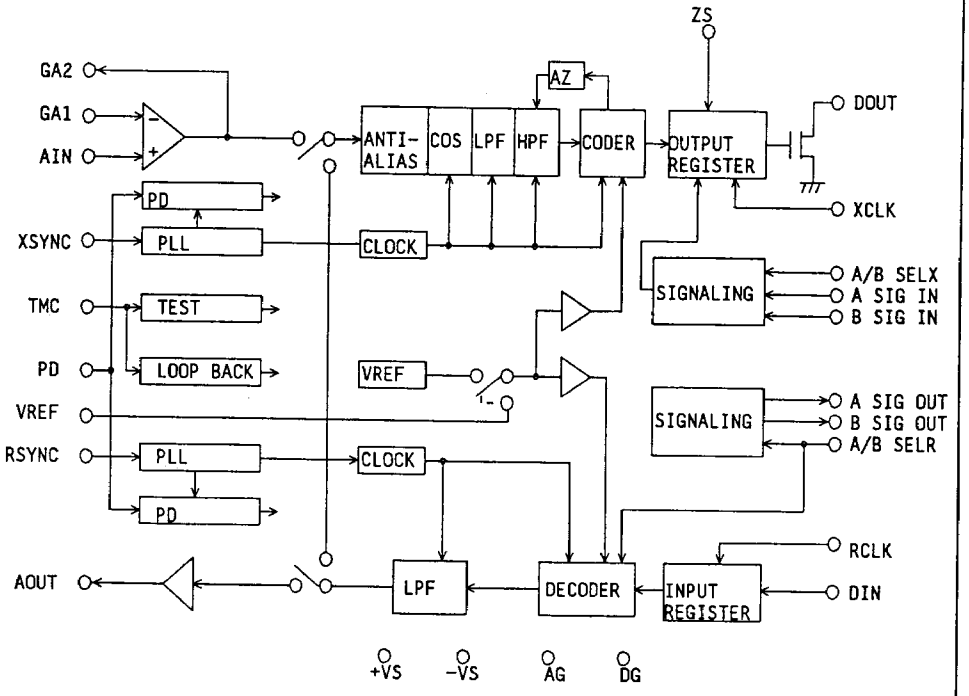
ABSOLUTE MAXIMUM RATINGS (See NOTE)

Rating	Symbol	Pin	Min	Max	Unit
Positive Supply Voltage	+VS	11	-0.3	7	V
Negative Supply Voltage	-VS	1	-7	0.3	V
Reference Supply Voltage	V_{REF}	10	-VS	+VS	V
Analogue Input Voltage	V_{AIN}	2	-VS-0.3	+VS+0.3	V
Digital Input Voltage	V_{DIN1}	6,12,13,14, 15,16,17, 18,19,20	-0.3	+VS+0.3	V
Digital Input Voltage	V_{DIN2}	22,23	-VS-0.3	+VS+0.3	V
Storage Temperature	T_{STG}		-55	150	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig.1 – MB6024 BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The simplified block diagram of the MB6024 is shown in Figure 1. The transmit section is composed of an input gain amplifier, an anti-aliasing filter, a band-pass filter and a cpmpressing coder. An auto-zero circuit is also included. The receive section is composed of an expanding decoder and a low-pass filter.

TRANSMIT SECTION

Input analog signals first enter an operational amplifier provided for gain adjustment. This amplifier is followed by a 2nd order analog anti-aliasing filter. This filter provides attenuation of 40 dB (typical) at the 256 kHz, the effective clock frequency of the following switched capacitor Cosine Filter. From the Cosine Filter, the signals enter a 5th order low-pass filter clocked at 128 kHz, followed by a 3rd order high-pass filter clocked at 8 kHz. The resulting band-pass characteristics meet both the D3/D4 specification and the CCITT G.712 recommendation. The output of the high-pass filter is then sampled by the coder at 8 kHz. This coder transforms the analog signals into 8-bit words using compressing law. The encoded PCM data is shifted out serially by the transmit clock, which can vary from 64 kHz to 3.152 MHz. An auto-zero circuit is provided for the DC offset correction.

RECEIVE SECTION

The PCM data is shifted in by the receive clock which vary from 64 kHZ to 3.152 MHz. The decoder reconstructs the analog signals from the PCM data using expanding law. The decoder is followed by a 5th order low pass filter. This filter smooths the sampled and held signals and corrects for the SinX/X attenuation due to the 8 kHz sampling and holding operation.

INTERNAL CLOCK

Two independent Phase Locked Loops generate internal clocks for the transmit and receive sections from the respective synchronization clocks.

TEST MODE

Test modes allow analog loop back operation and independent avaluation of the coder, decoder and receive filter.

SIGNALING

The A/B signaling function is provided. The A/B signaling Pins are transition sensitive.

ZERO CODE SUPPRESSION

Zero code suppression is pin-selectable. If zero code suppression is selected negative input signal values between the decision value numbers 127 and 128 are encoded as 00000010.

POWER DOWN MODE

Two power down modes are provided. The transmit and receive sections independently go into power down operation in the absense of the respective synchronization clocks. If the external power down input is connected to a TTL low level, both the transmit and receive sections are powerd down regardless of the synchronization clocks.

PIN DESCRIPTION

Pin Name	Pin No.	Description
+VS	11	Positive Voltage Supply, +5V ± 5%
-VS	1	Negative Voltage Supply, -5V ± 5%
DG	21	Digital Ground All digital signals should be referenced to this pin.
AG	5	Analog Ground All analog signals should be referenced to this pin.
XCLK	14	Transmit clock This TTL compatible input defines the bit rate on the transmit PCM highway. The device can operate with bit rates of 64 kHz to 3.152 MHz. The digital PCM codes are shifted out of the device on the rising edges of the clock.
XSYNC	16	Transmit Synchronization Clock This TTL compatible inut defines the beginning of the transmit timeslot on the transmit PCM highway. It must be synchronized with XCLK. The clock rate is typically 8 kHz and its duration can be equal or more than one XCLK cycle.
RCLK	13	Receive Clock This TTL compatible input defines the bit rate on the receive PCM highway. The device can operate with clock rate of 64 kHz to 3.152 MHz. The digital PCM codes are accepted on the trailing edges of the clock.
RSYNC	15	Receive Synchronization Clock This TTL compatible input defines the beginning of the receive timeslot in the receive PCM highway. It must be synchronized with RCLK. The clock rate is typically 8 kHz and its duration can be equal to or more than one RCLK cycle.
DOUT	24	Digital Output This is a LS-TTL compatible open-drain output. A pull-up resistor greater than 0.5 kΩ must be connected to +VS. PCM digital codes are shifted out of the device on the rising edge of XCLK in a serial format. This input goes into high-impedance state when 8-bit are shifted out of the output of shift register.
DIN	12	Digital Input This TTL compatible input to the decoder accepts an 8-bit data word into the shift register on the trailing edges of RCLK.
AIN	2	Analog Input Analog signals to be filetred and coded are supplied from this pin.
AOUT	9	Analog Output Decoded and filtered analog signals are outut from this pin. The load impedance connected to this output should be greater than 3 kΩ in parallel with less than 100 pF.

PIN DESCRIPTION (Continued)

Pin Name	Pin No.	Description
PD	23	Power Down If this TTL compatible input is at a TTL low level both the transmit and receive sections are powered down regardless of the synchronization clocks.
ZS	6	Zero Code Suppression If this TTL compatible input is at a TTL high zero code suppression is selected. In this mode negative input singal values between the decision value numbers 127 and 128 are encoded as 00000010.
A/B SELX	20	Transmit A/B Signaling Selection This TTL compatible input is provided to select A or B paths for the signaling information. It is transition sensitive.
A SIG IN	19	A Signaling Input This TTL compatible input is selected on a positive transition of A/B SELX. This input is sent in the 8-bit of the transmit word of the next timeslot.
B SIG IN	18	B Signaling Input This TTL compatible input is selected on a negative transition of A/B SELX. This input is sent in the 8-bit of the transmit word of the next timeslot.
A/B SELR	17	Receive A/B Signaling Selection This TTL compatible input is provided to select A or B paths for the signaling information. On a transition of this input the 7 most significant bits decoding is selected.
A SIG OUT	8	A Signaling Output This is a LS-TTL compatible open-drain output. The signaling bit is latched to this output on a positive transition of A/B SELR.
B SIG OUT	7	B Signaling Output This is a LS-TTL compatible open-drain output. The signaling bit is latched to this output on a positive transition of A/B SELR.
VREF	10	Reference Voltage Supply This pin is provided for the supply of an external voltage reference or for the selection of an internal reference. If VREF is greater than 2 volts the external voltage reference is selected. In this mode a 2.5 volt reference is recommended. If this pin is at a TTL low level or left open the internal reference (2.5 volts) is selected.

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PIN DESCRIPTION

Pin Name	Pin No.	Description
TMC	22	Test Mode Control This three level input is provided for the selection of analog loop back mode or test modes. If this pin is at a TTL high level the normal operation is selected. If this pin is at a TTL low level the analog loop back mode is selected. In this mode the output of the receive filter is internally connected to the input of the transmit filter and AOUT is forced to AG level. If this pin is connected to -VS then the test modes depend on A/B SELR is selected. These test modes allow independent evaluation of the coder, decoder and receive filter. When A/B SELR is TTL high AIN is internally connected to the inputs of the coder and receive filter and their outputs are available on the DOUT pin and the AOUT pin, respectively. When A/B SELR is TTL low level, AIN is internally connected to the input of the coder and its output is available on the DOUT pin. And also the output of the decoder is available on the AOUT pin.
GA1 GA2	3 4	Gain Adjust 1 Gain Adjust 2 These pins are provided for adjusting the gain of transmit section. GA1 and GA2 are the inverting-input and output of the amplifier, respectively. The load impedance connected to GA2 should be from 10 to 20 kΩ in parallel with less than 50 pF.

RECOMMENDED OPERATING CONDITIONS

Rating	Symbol	Pin	Value			Unit
			MIn	Typ	Max	
Positive Supply Voltage	+VS	11	+4.75	+5.0	+5.25	V
Negative Supply Voltage	-VS	1	-5.25	-5.0	-4.75	V
External Reference Voltage	V_{REF}	10		2.5		V
Internal Reference Voltage*	V_{IREF}	10	-0.8	0	+0.8	V
Digital Output Load Resistance	R_{DL}	24	0.5			kΩ
Digital Output Load Capacitance	C_{DL}	24			144	pF
A(B) SIGOUT Load Resistance	R_{DLSI}	7,8	5			kΩ
A(B) SIGOUT Load Capacitance	C_{DLSI}	7,8			100	pF
Analog Output Load Resistance	R_L	9	3			kΩ
Analog Output Load Capacitance	C_L	9			100	pF
Operating Temperature	T_{OP}		0	25	70	°C

* VREF pin (Pin No. 10) may be left open to select Internal Reference Voltage.

DC CHARACTERISTICS

(±VS= ±5V ± 5%, T_A = 0 - 70 °C, unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Positive Supply Current	$+I_{VS}$	11	Operating		7.0	10.0	mA
Negative Supply Current	$-I_{VS}$	1	Operating	-10.0	-5.0		mA
Positive Supply Current Power Down Mode	$+I_{VSST}$	11	XSYNC=RSYNC=VIL		1.0	2.0	mA
			PD=VIL		0.3	1.0	mA
Negative Supply Current Power Down Mode	$-I_{VSST}$	1	XSYNC=RSYNC=VIL	-0.5	-0.1		mA
			PD=VIL	-0.5	-0.1		mA
Reference Supply Current	I_{VREF}	10	VREF=2.5V	10	40	100	µA

DC CHARACTERISTICS (Continued)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Digital Input High Voltage	V_{IH}	6,12,13,14, 15,16,17,18, 19,20,22,23		2.0		+VS	V
Digital Input Low Voltage	V_{IL}	6,12,13,14, 15,16,17,18, 19,20,22,23		0		0.8	V
Digital Input High Current	I_{IH}	12,13,14,15, 16,23				10	μA
Digital Input Low Current	I_{IL}	12,13,14,15, 16,23				10	μA
Pull Down Current	I_{PLD}	6,17,18,19, 20	V_{IH} = +VS	0		150	μA
Pull up Current	I_{PLU}	22	V_{IL} = 0V	-150		0	μA
Digital Input Capacitance	C_{DIN}	6,12,13,14, 15,16,17,18, 19,20,22,23				10	pF
Digital Output Low Voltage	V_{OL1}	24	RDL=0.5kΩ +IOL=0.4mA			0.4	V
Digital Output Low Voltage	V_{OL2}	7,8	RDLSI=5kΩ +IOL=0.4mA			0.4	V
Digital Output Leakage Current	I_{OL}	7,8,24				10	μA
Digital Output Capacitance	C_{DOUT}	7,8,24				12	pF
Analog Input Offset Voltage	A_{INOFF}	2		-200	0	200	mV
Analog Input Resistance	R_{AIN}	2		300			kΩ
Analog Input Capacitance	C_{AIN}	2				10	pF
Analog Output Offset Voltage	A_{OUTOFF}	9		-150		150	mV
Analog Output Resistance	R_{AOUT}	9			10	30	Ω

AC CHARACTERISTICS

(±VS = ±5V ±5%, T_A= 0 - 70 °C, unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
Digital Input Rise Time	t_r	12,13,14,15, 16,17,18,19, 20,22	0.8V → 2.0V			50	ns
Digital Input Fall Time	t_f	12,13,14,15, 16,17,18,19, 20,22	2.0V → 0.8V			50	ns
Shift Clock Frequency	F_c	13, 14		64		3152	kHz
Shift Clock High Width	t_{WCH}	13, 14	V_{IH}=2.0V	140			ns
Shift Clock Low Width	t_{WCL}	13, 14	V_{IL}=0.8V	140			ns
Synchronization Frequency	F_s	15, 16			8		kHz
Synchronization High Width	t_{WSH}	15, 16	V_{IH}=2.0V	1/Fc (Fc: MHz)		117	µs
XSYNC to XCLK Delay	t_{SX}	14, 16		100			ns
XCLK to XSYNC Delay	t_{XS}	14, 16		50			ns
RSYNC to RCLK Delay	t_{SR}	13, 15		100			ns
RCLK to RSYNC Delay	t_{RS}	13, 15		50			ns
RCLK to DIN Delay	t_{RD}	12, 13		50			ns
DIN to RCLK Delay	t_{DR}	12, 13		50			ns
XCLK or XSYNC to DOUT Delay	t_{ZD}	14, 16, 24	NOTE 1 BIT 1	30		200	ns
XCLK to DOUT Delay	t_{XD}	14, 24	NOTE 1 BIT 2 to 8	30		200	ns
XCLK to DOUT Delay	t_{DZ}	14, 24	HZ	30		200	ns

Note 1: DOUT Load Conditions : R_{DL} = 0.5 kΩ, C_{DL} = 144 pF, $+I_{OL}$ = 0.4 mA

AC CHARACTERISTICS

(±VS = ±5V ±5%, T_A= 0 - 70 °C, unless otherwise noted.)

Parameter	Symbol	Pin	Conditions	Value			Unit
				Min	Typ	Max	
DOUT Fall Time	t_{Df}	24		10		100	ns
XCLK to TMC Delay	t_{XTM}	14, 22		200			ns
TMC to XCLK Delay	t_{TMX}	14, 22		200			ns
A/B SELX to XCLK Delay	t_{ABSX}	14, 20		1			µs
XCLK to A/B SELX Delay	t_{XABS}	14, 20		1			µs
A(B)SIGIN to XCLK Delay	t_{SIX}	14,18,19		1			µs
XCLK to A(B)SIGIN Delay	t_{XSI}	14,18, 19		1			µs
A/B SELR to RCLK Delay	t_{ABSR}	13, 17		1			µs
RCLK to A/B SELR Delay	t_{RABS}	13, 17		1			µs
RCLK to A(B)SIGOUT Delay	t_{RSI}	7,8,13	NOTE 2	0		20	µs
A(B) SIGOUT Fall Time	t_{SIf}	7, 8		10		300	ns

Note 2: A(B) SIGOUT Load Conditions : R_{DLSI} = 5.0 kΩ, C_{DLSI} = 100 pF, I_{OL} = 0.4 mA

Fig.2 - TIMING DIAGRAM

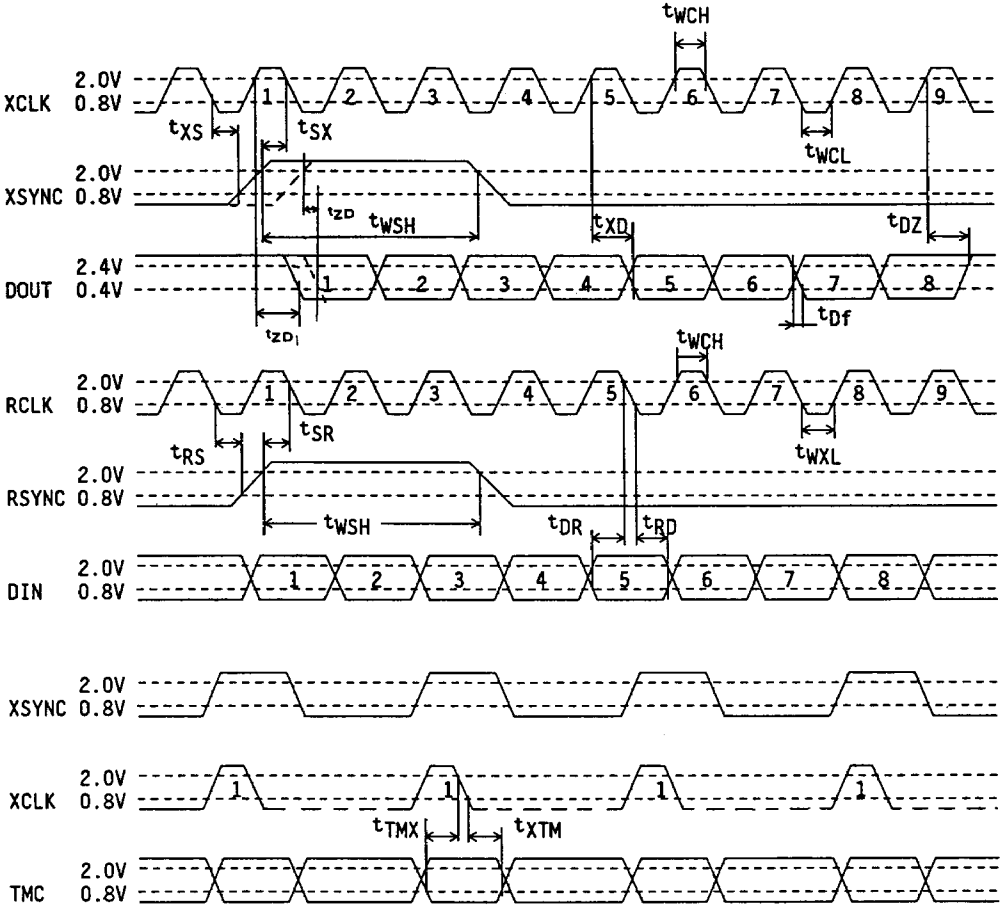

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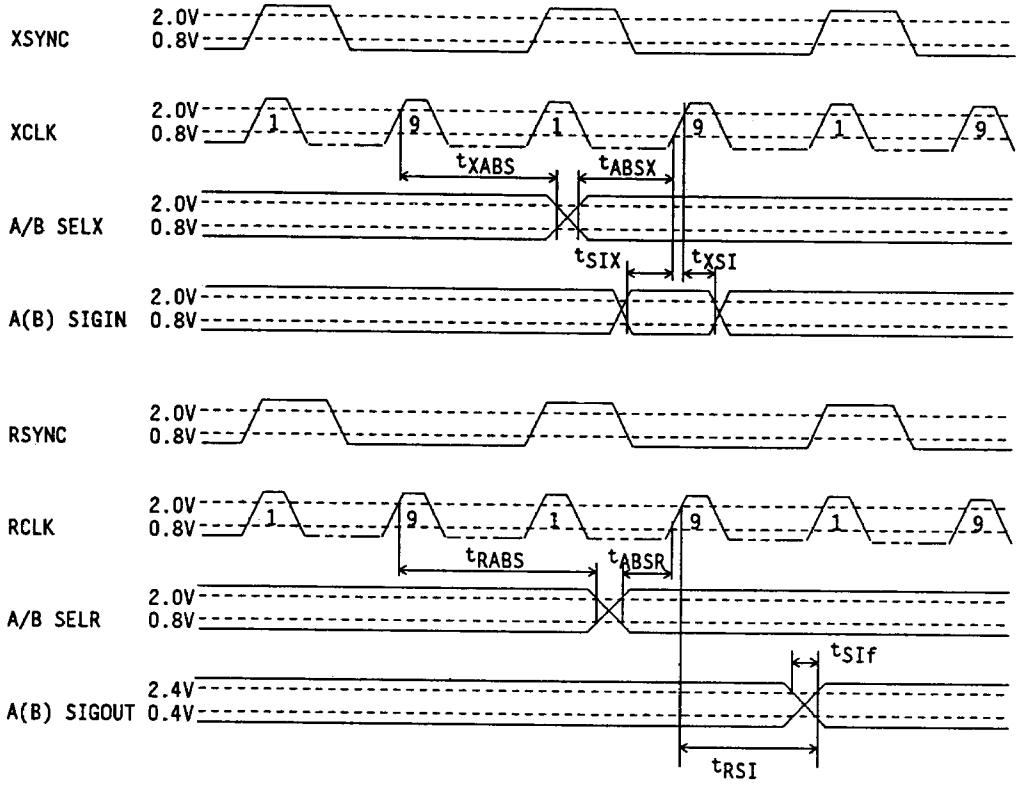
Fig.3 -TIMING DIAGRAM



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TRANSMISSION CHARACTERISTICS

(±VS =±5.0 V ± 5%, T_A = 0 - 70 °C, unless otherwise noted.)

Parameter	Symbol	Conditions		Value Min	Value Typ	Value Max	Unit
Signal to Distortion (A to A)	SDA	1020Hz tone (C Message)	+3 to -30dBm0	35.0			dB
			-40dBm0	30.0			dB
			-45dBm0	25.0			dB
Signal to Distortion (A to D)	SDX	1020Hz tone (C Message)	+3 to -30dBm0	36.0			dB
			-40dBm0	31.0			dB
			-45dBm0	26.0			dB
Signal to Distortion (D to A)	SDR	1020Hz tone (C Message)	+3 to -30dBm0	36.0			dB
			-40dBm0	31.0			dB
			-45dBm0	26.0			dB
Gain Tracking (A to A)	GTA	1020Hz tone	+3 to -40dBm0	-0.4		0.4	dB
			-40 to -50dBm0	-0.8		0.8	dB
			-50 to -55dBm0	-2.0		2.0	dB
Gain Tracking (A to D)	GTX	1020Hz tone	+3 to -40dBm0	-0.2		0.2	dB
			-40 to -50dBm0	-0.4		0.4	dB
			-50 to -55dBm0	-0.8		0.8	dB
Gain Tracking (D to A)	GTR	1020Hz tone	+3 to -40dBm0	-0.2		0.2	dB
			-40 to -50dBm0	-0.4		0.4	dB
			-50 to -55dBm0	-0.8		0.8	dB
Frequency Response (A to A)	FRA	0 - 60Hz		24.0			dB
		60 - 300Hz		-0.2			dB
		300 - 3000Hz		-0.2		0.3	dB
		3000 - 3400Hz		-0.2		1.6	dB
		3400 - 4600Hz		Note 1			dB
		4.6 - 12KHz		64.0			dB
		Relative to 0dBm0, 820Hz					
Frequency Response (A to D)	FRX	0 - 60Hz		24.0			dB
		60 - 300Hz		-0.1			dB
		300 - 3000Hz		-0.1		0.15	dB
		3000 - 3400Hz		-0.1		0.8	dB
		3400 - 4600Hz		Note 2			dB
		4.6 - 12KHz		32.0			dB
		Relative to 0dBm0, 820Hz					
Frequency Response (D to A)	FRR	0 - 300Hz		-0.1			dB
		300 - 3000Hz		-0.1		0.15	dB
		3000 - 3400Hz		-0.1		0.8	dB
		3400 - 4600Hz		Note 2			dB
		4.6 - 12KHz		32.0			dB
		Relative to 0dBm0, 820Hz					

Note 1 : $29(1-\mathrm{Sin}\frac{\pi(4000-f)}{1200})$ Note 2 : $14.5(1-\mathrm{Sin}\frac{\pi(4000-f)}{1200})$

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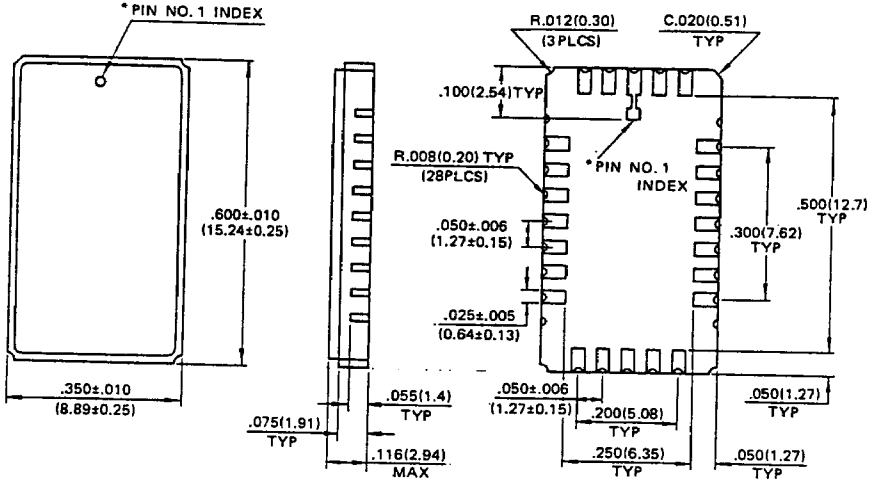
TRANSMISSION CHARACTERISTICS (Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Idle Channel Noise (A to A)	ICNA	C Message		-80	-72.0	dBm0c
Idle Channel Noise (A to D)	ICNX	C Message		-83	-74.0	dBm0c
Idle Channel Noise (D to A)	ICNR	C Message		-83	-78.0	dBm0c
Crosstalk (A to A)	CTA	1020Hz, 0dBm0			-66	dB
Crosstalk (D to D)	CTD	1020Hz, 0dBm0			-66	dB
Analog Input Level	AIL	1020Hz, 0dBm0, Internal VREF ±VS=±5.0V, TA=25°C	1.213	1.227	1.241	Vrms
Analog Output Level	AOL	1020Hz, 0dBm0 ±VS=±5.0V, TA=25°C	1.213	1.227	1.241	Vrms
Gain Accuracy (A to A)	GAA	1020Hz, 0dBm0 Internal VREF	-0.5	0	+0.5	dB
		±VS=±5.0V, T_A=25°C	-0.3	0	+0.3	dB
Gain Accuracy (A to D)	GAX	1020Hz, 0dBm0 Internal VREF	-0.25	0	+0.25	dB
		±VS=±5.0V, TA=25°C	-0.15	0	+0.15	dB
		Variation with power Supply		±0.02		dB
		Variation with Temperature		±0.001		dB/°C
Gain Accuracy (D to A)	GAR	1020Hz, 0dBm0 Internal VREF	-0.25	0	+0.25	dB
		±VS=±5.0V, TA=25°C	-0.15	0	+0.15	dB
		Variation with power Supply		±0.02		dB
		Variation with Temperature		±0.001		dB/°C
Propagation Delay (A to A)	PDA	FC ≥ 1544kHz			540	µs

TRANSMISSION CHARACTERISTICS (Continued)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Delay to Distortion (A to A)	DDA	500 - 600Hz 600 - 1000Hz 1000 - 2600Hz 2600 - 2800Hz 1020Hz, 0dBm0 Relative to Minimun Dealy			1.5 0.75 0.25 1.5	ms ms ms ms
PSRR (+VS) (A to A)	PSRRA+	0<f≤50kHz Idle Channel Noise (C Message) +VS+50mVop AIN=AGND	25	30		dB
PSRR (-VS) (A to A)	PSRRA-	0<f≤50kHz Idle Channel Noise (C Message) -VS+50mVop AIN=AGND	35	40		dB
Intermoduration (A to A)	IMA1	AIN a. 0.47kHz, -10dBm0 b. 0.32kHz, -10dBm0 AOUT(2a-b)			-38	dB
Intermoduration (A to A)	IMA2	AIN a. 1.02kHz, -9dBm0 b, 0.05kHz, -23dBm0 AOUT(a-b)			-52	dBm0
Signal Frequency Noise (A to A)	SFNA	0 - 4kHz 4 - 200kHz AIN=AGND			-70 -50	dBm0 dBm0
Discrimination (A to A)	DISA	AIN=0dBm0 4.6 - 200kHz	30			dB
In Band Spurious (A to A)	IBSA	2nd, 3rd, Harmonic AIN=0dBm0, 1020 Hz	43			dB

24-PAD CERAMIC (FRIT SEAL) LEADLESS CHIP CARRIER
(CASE No.: LCC-24C-F03)



* Shape of PIN NO. 1 INDEX: Subject to change without notice.

Dimensions in
inches (millimeters)