FEATURES

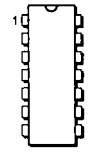
- ☐ Built-in dial tone rejection
- ☐ Single 5 Volt supply
- ☐ Three-state outputs
- ☐ Narrow 14 or 18 pin package

GENERAL DESCRIPTION

The SC11202, SC11203 and SC11204 are central office quality dual-tone, multi-frequency (DTMF)—touch tone—receivers built with Sierra's proprietary 3 micron CMOS process. They receive analog DTMF signals and decode them into the 16 standard digits. The SC11202 and SC11203 provide either a 4-bit hexadecimal code or binary coded 2 of 8, while the SC11204 provides 4-bit hex code only. The outputs are three state, CMOS logic compatible, facilitating bus interfaces. A built-in dial tone rejection circuit eliminates the need for any front-end or prefiltering. The only external components required are an inexpensive 3.58 MHz crystal and a bias resistor for the time base. Up to ten DTMF receivers may be operated from a single crystal through the Alternate Time Base (ATB) pin. The SC11202 is pin and function compatible to Silicon Systems' 202 (18 pin), the SC11203 is pin and function compatible with Silicon Systems' 203 (18 pin with an Early Detect output) and the SC11204 is a 14-pin device compatible with SSI's 204. Unlike the SSI parts, all Sierra DTMF Receivers include an integral dial tone rejection filter.

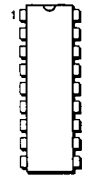
Applications include central office switches, PBXs, auto dialers for redialing a number over an alternate carrier, subscriber equipment such as telephone answering machines, remote banking or other transaction systems that employ DTMF signals for remote operation and voice/DTMF response systems.

14-PIN DIP PACKAGE



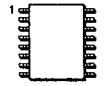
SC11204CN

18-PIN DIP PACKAGE



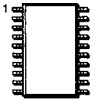
SC11202CN
SC11203CN

16-PIN SOIC PACKAGE



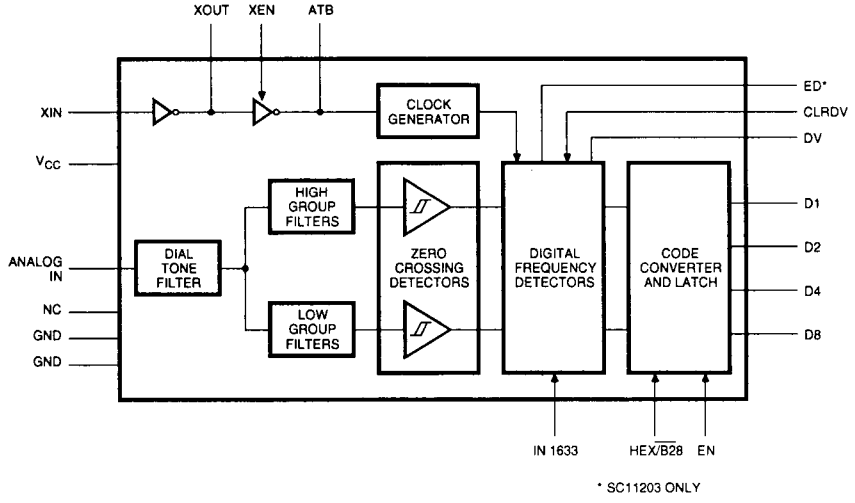
SC11204CM

20-PIN SOIC PACKAGE



SC11202CM
SC11203CM

BLOCK DIAGRAM



* SC11203 ONLY

PIN DESCRIPTION

PIN NAME	PIN NO.				FUNCTION
	SC11202 SC11203		SC11204		
	P1	P2	P3	P4	
D1 D2 D4 D8	1 18 17 16	1 20 19 18	2 1 14 13	2 1 16 15	Digital outputs that provide the code corresponding to the detected digit. These outputs are push-pull CMOS when EN (pin 3) is high and are a high impedance, open circuit, when EN is low. In the SC11202 and SC11203, the digital output format is programmed by the HEX/$\overline{B28}$ pin (2) to be either hexadecimal or binary coded 2 of 8 (see Table 3). In the SC11204 the output is hexadecimal and is on pins 2, 1, 14 and 13. These outputs become valid after a tone pair has been detected and they are cleared when a valid pause is timed.
HEX/$\overline{B28}$	2	2			Selects the digital output format on the SC11202 and SC11203. When HEX/$\overline{B28}$ is high, the outputs on D1, D2, D4 and D8 are hexadecimal; when it is low, the outputs are binary coded 2 of 8. See Table 3 for the hexadecimal and binary 2 of 8 codes.
EN	3	3	3	3	Enables the digital outputs D1, D2, D4 and D8.
IN1633	4	5			When tied high, this pin inhibits the detection of tone pairs containing the 1633 Hz component. To detect all 16 standard digits, IN1633 must be tied low. It has an internal pull-down to ground.
V_{CC}	5	6	4	4	Positive supply: 5 Volts.
ED	6*	8*			Provided only on the SC11203, the ED output goes high as soon as a DTMF tone pair begins to be detected, and goes low when a pause begins to be detected. D1, D2, D4 and D8 outputs are guaranteed to be valid when DV is high, but are not necessarily valid when ED is high.
GND	7, 10	9, 12	8	9	Ground; 0 Volts. Pin 10 must be tied to ground; pin 7 is optional.
XEN	8	10	6	7	Enables the crystal oscillator. When high, the crystal oscillator is enabled. This pin should be tied low if the device is driven by an external oscillator through the ATB input.
Analog IN	9	11	7	8	Accepts the analog input. This pin is internally biased so that the input signal may be AC coupled through a 0.01 µF capacitor. The input may be DC coupled as long as it does not exceed the positive supply.
XOUT XIN	11 12	13 14	9 10	10 11	Crystal oscillator output and input. A 3.58 MHz crystal in parallel with a 1 MΩ, 10% resistor is connected between these pins. The oscillator is enabled by tying XEN (pin 8) high. In this mode, the clock frequency is also provided at the ATB output (pin 13).
ATB	13	15	11	12	Alternate time-base. For a device with a crystal and a resistor connected between pins 11 and 12, and XEN tied high. ATB is a 447.5 KHz clock output that can be used to drive up to ten other DTMF receivers. For these devices, XEN must be tied low and ATB is an input.
DV CLRDV	14 15	16 17	12	14	Data valid and clear data valid. DV goes high after a valid tone pair is sensed and decoded at the output of pins D1, D2, D4 and D8. DV remains high until a valid pause occurs or until the CLRDV input is taken high, whichever occurs first.
NC			5		NC indicated that no internal connection is made to the pin and it may be left floating.

NOTES: P1 is the 18-pin DIP; P2 is the 20-pin SOIC; P3 is the 14-pin DIP; P4 is the 16-pin SOIC
* ED pin not connected on SC11202

PIN DESCRIPTIONS (Cont.)

Table 1. DTMF Dialing Matrix

	COL 0	COL 1	COL 2	COL 3
Row 0	1	2	3	A
Row 1	4	5	6	B
Row 2	7	8	9	C
Row 3	*	0	#	D

Table 2. Detection Frequency

LOW GROUP f_o	HIGH GROUP f_o
Row 0 = 697 Hz	Col. 0 = 1209 Hz
Row 1 = 770 Hz	Col. 1 = 1336 Hz
Row 2 = 852 Hz	Col. 2 = 1477 Hz
Row 3 = 941 Hz	Col. 3 = 1633 Hz

Table 3. HEX/$\overline{B28}$ Output Codes

	HEXADECIMAL				BINARY CODED 2 OF 8			
DIGIT	D8	D4	D2	D1	D8	D4	D2	D1
1	0	0	0	1	0	0	0	0
2	0	0	1	0	0	0	0	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	0	0
5	0	1	0	1	0	1	0	1
6	0	1	1	0	0	1	1	0
7	0	1	1	1	1	0	0	0
8	1	0	0	0	1	0	0	1
9	1	0	0	1	1	0	1	0
0	1	0	1	0	1	1	0	1
*	1	0	1	1	1	1	0	0
#	1	1	0	0	1	1	1	0
A	1	1	0	1	0	0	1	1
B	1	1	1	0	0	1	1	1
C	1	1	1	1	1	0	1	1
D	0	0	0	0	1	1	1	1

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2 and 3)

Supply Voltage, V_{CC}	7 V
DC Input Voltage	–0.5 to V_{CC} + 0.5 V
Analog Input Voltage	V_{CC} – 10 V to V_{CC} + 0.5 V
Storage Temperature Range	–65°C to 150°C
Power Dissipation (Note 3)	500 mW
Lead Temperature (soldering 10 sec)	300°C

OPERATING CONDITIONS (Note 4)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_A	Ambient Temperature		0		70	°C
V_{CC}	Positive Supply Voltage		4.5		5.5	V
GND	Ground			0		V
F_C	Crystal Frequency		3.576	3.579545	3.583	MHz

Notes: 1. Absolute maximum ratings are those values beyond which damage to the device may occur.
2. Unless otherwise specified all voltages are referenced to ground.
3. Power dissipation temperature derating:
Plastic package: –12mW/C from 65°C to 85°C
Ceramic package: –12mW/C from 100°C to 125°C.

ELECTRICAL CHARACTERISTICS (Note 4)

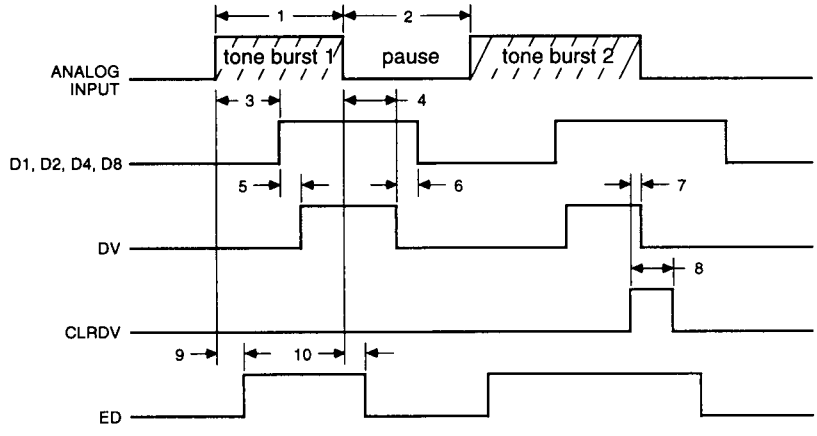
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Frequency Detect Bandwidth		±(1.5+2 Hz)	±2.3	±3.5	% of f_o
Amplitude for Detection	Each Tone	–32		–2	dBM Referenced to 600Ω
Minimum Acceptable Twist	Twist = $\frac{\text{High Tone}}{\text{Low Tone}}$	–10		+10	dB
60 Hz Tolerance				0.8	Vrms
Dial Tone Tolerance	'Precise' Dial Tone			18.0	dB Referenced to Lower Amplitude Tone
Talk Off	MITEL Tape #CM 7291		2		Hits
Digital Ouputs (except XOUT)	'0' Level 400 µA Load	0		0.5	Volts
	'1' Level 200 µA Load	V_{CC}–0.5		V_{CC}	Volts
Digital Inputs	'0' Level	0		0.3 V_{CC}	Volts
	'1' Level	0.7 V_{CC}		V_{CC}	Volts
Power Supply Noise	Wide Band			10	mVp–p
Supply Current	T_A = 25°C		10	16	mA
Noise Tolerance	MITEL Tape #CM 7291			–12	dB Referenced to Lowest Amplitude Tone
Input Impedance	$V_{CC} \geq V_{IN}$ V_{CC}–10	100 kΩ//15 pFk			

Notes: 4. Min and max values are valid over the full temperature and operating voltage range. Typical values are for 25°C and 5 V operation.

TIMING CHARACTERISTICS (at 25°C and 5 V supply)

NO	SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNITS
1	TON	Tone Time for Detection		40			ms
1	TON	Tone Time for Rejection				20	ms
2	TOFF	Pause Time for Detection		40			ms
2	TOFF	Pause Time for Rejection				20	ms
3	TD	Detect Time		25		46	ms
4	TR	Release Time		35		50	ms
5	TSU	Data Setup Time		7			µs
6	TH	Data Hold Time		4.2		5.0	ms
7	TCL	DV Clear Time			160	250	ns
8	TPW	CLRDV Pulse Width		200			ns
9	TED	ED Detect Time		7		22	ms
10	TER	ED Release Time		2		18	ms
	TOE	Output Enable Time	C_L = 50 pF, R_L = 1 kΩ		200	300	ns
	TOD	Output Disable Time	C_L = 35 pF, R_L = 500 Ω		150	200	ns
	TOR	Output Rise Time	C_L = 50 pF		200	300	ns
	TOF	Output Fall Time	C_L = 50 pF		160	250	ns

TIMING CHARACTERISTICS (Cont.)

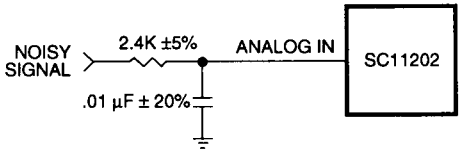


APPLICATION NOTES

The DTMF receiver will tolerate total input rms noise up to 12 dB below the lowest amplitude tone. For most telephone applications, the combination of the high frequency attenuation of the telephone line and internal band-limiting make special circuitry at the input to the DTMF receiver unnecessary. However, noise near the 74.6 kHz internal sampling frequency will be aliased (folded back) into the audio spectrum; if excessive noise is present above 37.3 kHz, the simple RC filter shown below can be employed to band limit the incoming signal. Noise will also be reduced by placing a ground trace around the XIN and XOUT pins on the circuit board layout when using a crystal. XOUT is not intended to drive an additional device. XIN may be driven externally in which case XOUT must be left floating.

Crystal Oscillator

The DTMF receivers contain an onboard inverter with sufficient gain to provide oscillation when connected to a low-cost television color-burst crystal. The crystal oscillator is enabled by tying XEN high. The crystal is connected between XIN and XOUT. A 1 MΩ, 10% resistor is also connected between these pins. In this mode, ATB is a clock frequency output. Other DTMF receivers may use the same frequency reference by tying their ATB pins to the ATB of a crystal connected device. XIN and XEN of the auxiliary devices must then be tied high and low respectively. Ten devices may run off a single DTMF receiver with a crystal as shown below.



For use in extreme high frequency input noise environment.