OKI semiconductor

MSC2323258D-xxBS4/DS4

2,097,152 Word By 32 Bit DYNAMIC RAM MODULE : FAST PAGE MODE WITH EDO

GENERAL DESCRIPTION

The Oki MSC2323258D-xxBS4/DS4 is a fully decoded, 2,097,152 word X 32 bit CMOS dynamic random access memory composed of four 16Mb(1Mx16) DRAMs in SOJ. The mounting of four DRAMs together with decoupling capacitors on a 72-pin glass epoxy Single-in-Line Package supports any application where high density and large capacity of storage memory are required.

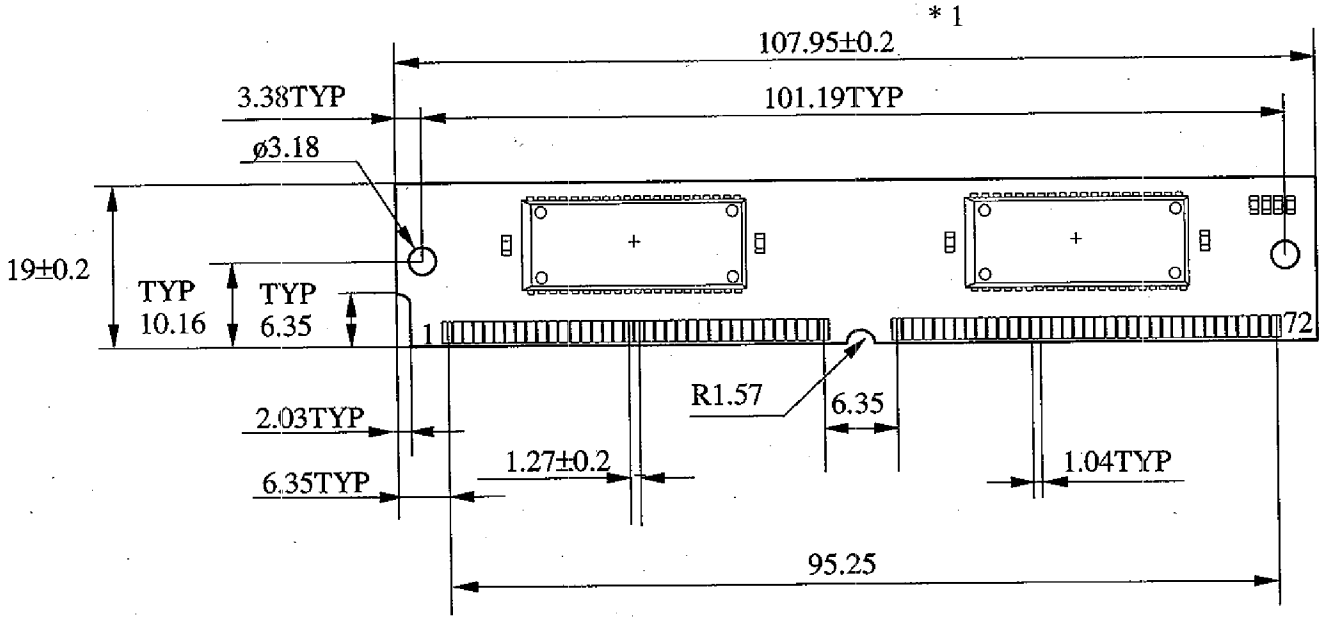
FEATURES

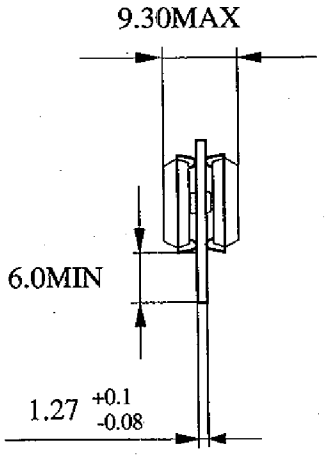
- 2,097,152 word X 32 bit organization
- 72-pin SIMM
  MSC2323258D-xxBS4 : Gold tab
  MSC2323258D-xxDS4 : Solder tab
- Single +5 V supply ±10 % tolerance
- Input : TTL compatible
- Output : TTL compatible, tristate, nonlatch
- Refresh : 1024 cycles/16 ms
- $\overline{CAS}$ before $\overline{RAS}$ refresh, $\overline{CAS}$ before $\overline{RAS}$ hidden refresh, $\overline{RAS}$ only refresh capability

FAMILY ORGANIZATION

FAMILY	ACCESS TIME (MAX)			Cycle Time	Power Dissipation	
	t_{RAC}	t_{AA}	t_{CAC}	(MAX)	Operating (MAX)	Standby (Max)
MSC2323258D-60BS4/DS4	60ns	30ns	15ns	104ns	1486mW	22mW
MSC2323258D-70BS4/DS4	70ns	35ns	20ns	124ns	1376mW	

MSC2323258D-xxBS4/DS4

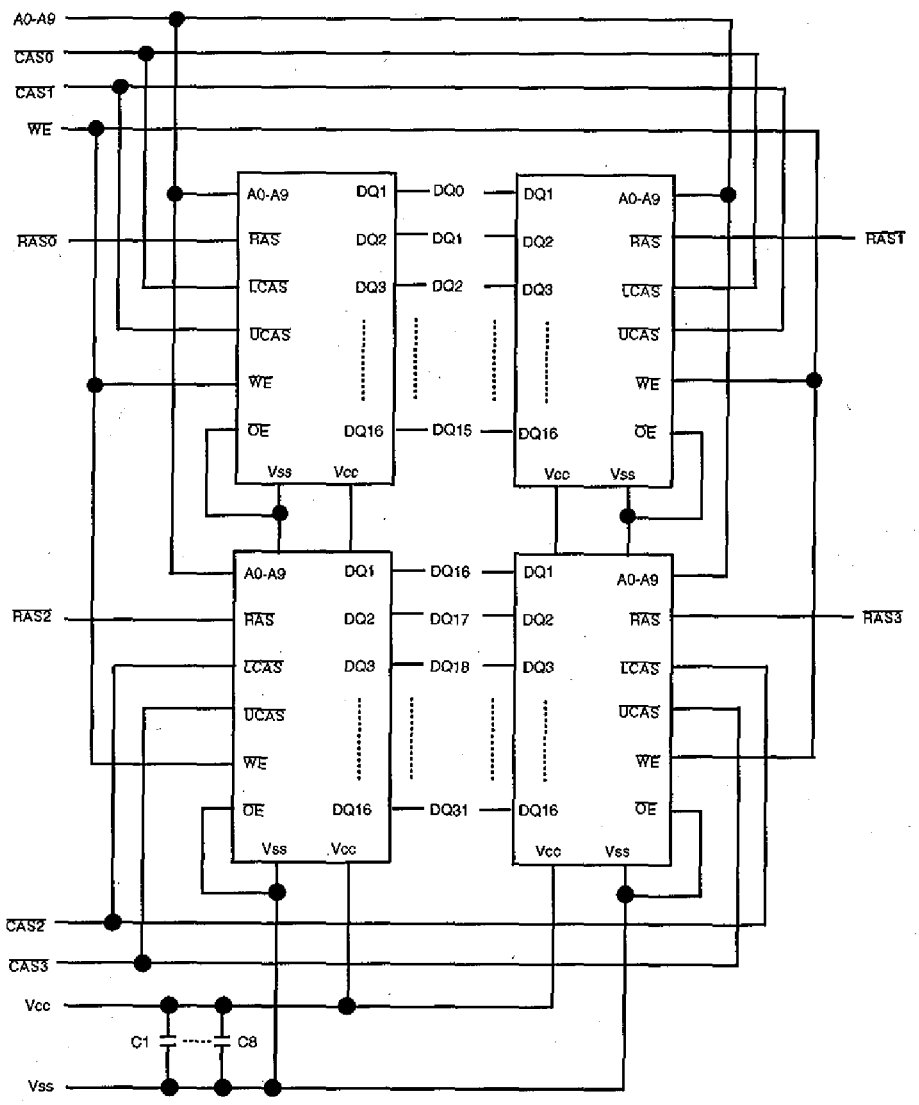




* 1 The common size defference of the board width 12.5mm of its height is specified as ±0.2. The value above 12.5mm is specified as ±0.5.

FUNCTIONAL BLOCK DIAGRAM

MSC2323258D-xxBS4/DS4



PIN CONFIGURATION

MSC2323258D-xxBS4/DS4

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	Vss	19	NC	37	NC	55	DQ11
2	DQ0	20	DQ4	38	NC	56	DQ27
3	DQ16	21	DQ20	39	Vss	57	DQ12
4	DQ1	22	DQ5	40	$\overline{CAS0}$	58	DQ28
5	DQ17	23	DQ21	41	$\overline{CAS2}$	59	Vcc
6	DQ2	24	DQ6	42	$\overline{CAS3}$	60	DQ29
7	DQ18	25	DQ22	43	$\overline{CAS1}$	61	DQ13
8	DQ3	26	DQ7	44	$\overline{RAS0}$	62	DQ30
9	DQ19	27	DQ23	45	$\overline{RAS1}$	63	DQ14
10	Vcc	28	A7	46	NC	64	DQ31
11	NC	29	NC	47	WE	65	DQ15
12	A0	30	Vcc	48	NC	66	NC
13	A1	31	A8	49	DQ8	67	PD1
14	A2	32	A9	50	DQ23	68	PD2
15	A3	33	$\overline{RAS3}$	51	DQ9	69	PD3
16	A4	34	$\overline{RAS2}$	52	DQ25	70	PD4
17	A5	35	NC	53	DQ10	71	NC
18	A6	36	NC	54	DQ26	72	Vss

PRESENCE DETECT PINS

Pin No.	Pin name	-60	-70
67	PD1	NC	NC
68	PD2	NC	NC
69	PD3	NC	Vss
70	PD4	NC	NC

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	- 1.0 ~ + 7.0	V
Voltage Vcc supply relative to Vss	V_{CC}	- 1.0 ~ + 7.0	V
Short circuit output current	I_{OS}	50	mA
Power dissipation	P_D	4	W
Operating temperature	T_{OPR}	- 0 ~ + 70	°C
Storage temperature	T_{STG}	- 40 ~ + 125	°C

NOTE:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted within the limits as specified in this data sheet. Exposure to absolute maximum rating conditions for extended period may affect device reliabity.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN	TYPE	MAX	UNIT	Operating temperature
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	0 °C ~ + 70 °C
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.4	-	6.5	V	
Input low voltage	V_{IL}	-1.0	-	0.8	V	

CAPACITANCE

Parameter	Symbol	Typ.	MAX	Unit
Input Capacitance(A0-A9)	C_{IN1}	-	32	pF
Input Capacitance($\overline{WE}$)	C_{IN2}	-	35	pF
Input Capacitance($\overline{RAS0}$-$\overline{RAS3}$)	C_{IN3}	-	13	pF
Input Capacitance($\overline{CAS0}$-$\overline{CAS3}$)	C_{IN4}	-	20	pF
I/O Capacitance(DQ0-DQ31)	C_{DQ}	-	25	pF

Capacitance measured with Boonton Meter.

DC CHARACTERISTICS

(Vcc = 5V± 10%, Ta = 0 ~ +70 °C)

Parameter	Symbol	Condition		MSC2323258D-60BS4/DS4		MSC2323258D-70BS4/DS4		Unit	Note
				Min	Max	Min	Max		
Input Leakage Current	I_{LI}	0V≤V_{in}≤6.5V; All other pins not under test = 0V		-40	40	-40	40	µA	
Output Leakage Current	I_{LO}	Data out is disable 0V≤V_{out}≤5.5V		-20	20	-20	20	µA	
Output High Voltage	V_{OH}	I_{OH} = -5.0mA		2.4	Vcc	2.4	Vcc	V	
Output Low Voltage	V_{OL}	I_{OL} = 4.2mA		0	0.4	0	0.4	V	
Average power supply current (Operating)	I_{CC1}	$\overline{RAS}$ cycling, $\overline{CAS}$ cycling t_{RC}=min		-	270	-	250	mA	1,2
Power supply current (Standby)	I_{CC2}	$\overline{RAS}$=V_{IH} $\overline{CAS}$ =V_{IH}	TTL	-	8	-	8	mA	
			MOS	-	4	-	4	mA	
Average power supply current ($\overline{RAS}$ only refresh)	I_{CC3}	$\overline{RAS}$ cycling, $\overline{CAS}$ =V_{IL} t_{RC}=min		-	270	-	250	mA	1
Average power supply current ($\overline{CAS}$ before $\overline{RAS}$ refresh)	I_{CC6}	t_{RC} = min.		-	270	-	250	mA	1
Average power supply current (Fast page)	I_{CC7}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling t_{PC} = min.		-	270	-	250	mA	1,3

NOTE:
1. Icc is dependent on output loading and cycles rates. Specified values are obtained with the output open.
2. Address can be changed once or less while $\overline{RAS}$ = V_{IL}
3. Address can be changed once or less while $\overline{CAS}$ = V_{IH}

AC CHARACTERISTIC

(Vcc = 5V±10%, Ta = 0 ~70 °C)

NOTE 1,2,3

Parameter	Symbol	MSC2323258D-60BS4/DS4		MSC2323258D-70BS4/DS4		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Random read or write cycle time	t_{RC}	104	-	124	-	ns	
Fast page mode cycle time	t_{HPC}	25	-	30	-	ns	
Fast page mode read modify write cycle time	t_{HPRWC}	68	-	78	-	ns	
Access time from $\overline{RAS}$	t_{RAC}	-	60	-	70	ns	4,5,6
Access time from $\overline{CAS}$	t_{CAC}	-	15	-	20	ns	4,5
Access time from column address	t_{AA}	-	30	-	35	ns	4,6
Access time from $\overline{CAS}$ precharge	t_{CPA}	-	35	-	40	ns	4,12
Output low impedance time from $\overline{CAS}$	t_{CLZ}	0	-	0	-	ns	4
Output hold time from $\overline{CAS}$ low	t_{DOH}	5	-	5	-	ns	
$\overline{CAS}$ to dataoutput buffer turn-off delay time	t_{CEZ}	0	15	0	20	ns	7,8
$\overline{RAS}$ to dataoutput buffer turn-off delay time	t_{REZ}	0	15	0	20	ns	7,8
$\overline{WE}$ to dataoutput buffer turn-off delay time	t_{WEZ}	0	15	0	20	ns	7
Transition time	t_T	1	50	1	50	ns	3
Refresh period	t_{REF}	-	16	-	16	ms	
$\overline{RAS}$ precharge time	t_{RP}	40	-	50	-	ns	
$\overline{RAS}$ pulse width	t_{RAS}	60	10K	70	10K	ns	
$\overline{RAS}$ pulse width (Fast page mode)	t_{RASP}	60	100K	70	100K	ns	
$\overline{RAS}$ hold time	t_{RSH}	10	-	13	-	ns	
$\overline{CAS}$ precharge time	t_{CP}	10	-	10	-	ns	14
$\overline{CAS}$ pulse width	t_{CAS}	10	10K	13	10K	ns	
$\overline{RAS}$ low to $\overline{CAS}$ high delay time	t_{CSH}	40	-	45	-	ns	
$\overline{CAS}$ high to $\overline{RAS}$ low delay time	t_{CRP}	5	-	5	-	ns	12
$\overline{CAS}$ high to $\overline{RAS}$ high delay time	t_{RHCP}	35	-	40	-	ns	12
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	14	45	14	50	ns	5
$\overline{RAS}$ to column address delay time	t_{RAD}	12	30	12	35	ns	6
Row address set-up time	t_{ASR}	0	-	0	-	ns	
Row address hold time	t_{RAH}	10	-	10	-	ns	

AC CHARACTERISTICS (Continued)
(Vcc = 5V±10%, Ta = 0 ~70 °C)

Parameter	Symbol	MSC2323258D-60BS4/DS4		MSC2323258D-70BS4/DS4		UNIT	NOTE
		MIN	MAX	MIN	MAX		
Column address set-up time	t_{ASC}	0	-	0	-	ns	11
Column address hold time	t_{CAH}	10	-	13	-	ns	11
Column address to $\overline{RAS}$ lead time	t_{RAL}	30	-	35	-	ns	
Read command set-up time	t_{RCS}	0	-	0	-	ns	11
Read command hold time	t_{RCH}	0	-	0	-	ns	9,11
Read command hold time reference to $\overline{RAS}$	t_{RRH}	0	-	0	-	ns	9
Write command set-up time	t_{WCS}	0	-	0	-	ns	11
Write command hold time	t_{WCH}	10	-	13	-	ns	11
Write command pulse width	t_{WP}	10	-	10	-	ns	
Write command pulse width(output disable)	t_{WPE}	10	-	10	-	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	10	-	13	-	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	10	-	13	-	ns	13
Data-in set-up time	t_{DS}	0	-	0	-	ns	10,11
Data-in hold time	t_{DH}	15	-	20	-	ns	10,11
$\overline{CAS}$ precharge $\overline{WE}$ delay time	t_{CPWD}	54	-	64	-	ns	
$\overline{CAS}$ active delay time from $\overline{RAS}$ precharge	t_{RPC}	5	-	5	-	ns	11
$\overline{RAS}$ to $\overline{CAS}$ set-up time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CSR}	5	-	5	-	ns	11
$\overline{CAS}$ hold time ($\overline{CAS}$ before $\overline{RAS}$)	t_{CHR}	10	-	10	-	ns	12

NOTES: 1) An initial pause of 200 μs is required after power-up followed by aminimum of 8 initializatin cycles (examples: $\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) before proper device operation is achieved.
2) The AC measurements assume the transition time (t_T) = 5 ns.
3) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring the timing of the input signals. Transition times are measured between V_{IH} and V_{IL}.
4) Measured by using an eqivalent load circuit of 2 TTL loads and 100 pF.
5) Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD}(max) is specified as a reference point only: if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
6) Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD}(max) is specified as a reference point only: if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled by t_{AA}.
7) t_{CEZ} (max.), t_{REZ} (max.) and t_{WEZ} (max.) spec. define at which time the output data achieves a high impedance state and is not referenced to output voltage levels.
8) When both t_{CEZ} and t_{REZ} were satisfied, output data achieves a high impedance state.
9) Either the t_{RRH} or the t_{RCH} spec. must be satisfied for proper read cycle.
10) These parameters are referenced to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in an early write cycle.
11) These parameters are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
12) These parameters are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
13) t_{CWL} should be satisfied by both $\overline{UCAS}$ or $\overline{LCAS}$.
14) t_{CP} is determined by the time of both $\overline{UCAS}$ or $\overline{LCAS}$ are high.