LOW SKEW, 1-TO-4 LVCMOS/LVTTL-TO-LVDS FANOUT BUFFER

ICS8545-01

General Description

ICS HiPerClockS™

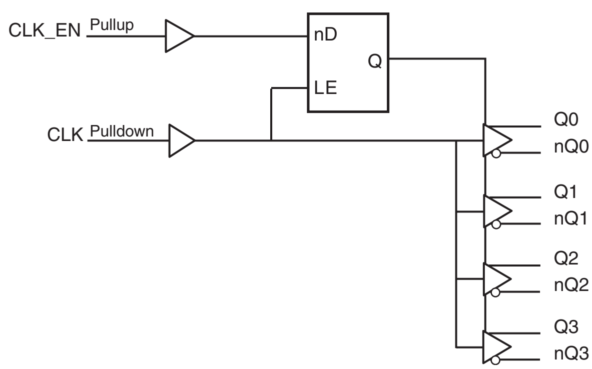
The ICS8545-01 is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-LVDS Clock Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. Utilizing Low Voltage Differential Signaling (LVDS) the ICS8545-01 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS8545-01 accepts a LVCMOS/LVTTL input level and translates it to 3.3V LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS8545-01 ideal for those applications demanding well defined performance and repeatability.

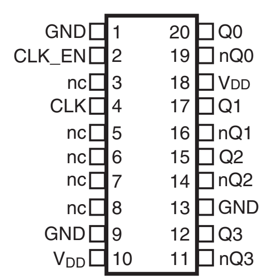
Features

- Four differential LVDS output pairs
- Two LVCMOS/LVTTL clock inputs to support redundant or selectable frequency fanout applications
- Maximum output frequency: 650MHz
- Translates LVCMOS/LVTTL input signals to LVDS levels
- Output skew: 40ps (maximum)
- Part-to-part skew: 500ps (maximum)
- Propagation delay: 3.6ns (maximum)
- Full 3.3Vsupply mode
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS8545-01

20-Lead TSSOP
6.5mm x 4.4mm x 0.925mm package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 9, 13	GND	Power		Power supply ground.
2	CLK_EN	Input	Pullup	Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, $\overline{Q}$ outputs are forced high. LVCMOS / LVTTL interface levels.
3, 5, 6, 7, 8	nc	Unused		No connect.
4	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
10, 18	V_{DD}	Power		Positive supply pins.
11, 12	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
14, 15	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
16, 17	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
19, 20	nQ0, Q0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Function Tables

Table 3. Clock Input Function Table

Input	Outputs	
CLK	**Q0:Q3**	**nQ0:nQ3**
0	LOW	HIGH
1	HIGH	LOW

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O Continuos Current Surge Current	 10mA 15mA
Package Thermal Impedance, θ_{JA}	91.1°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 4A. Power Supply DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current				50	mA

Table 4B. LVCMOS/LVTTL DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN}$ = 3.465V			150	µA
		CLK_EN	$V_{DD} = V_{IN}$ = 3.465V			5	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		CLK_EN	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA

Table 4C. LVDS DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage		200	280	360	mV
ΔV_{OD}	V_{OD} Magnitude Change				40	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	V_{OS} Magnitude Change			5	25	mV
I_{Oz}	High Impedance Leakage		-10	±1	+10	µA
I_{OFF}	Power Off Leakage		-20	±1	+20	µA
I_{OSD}	Differential Output Short Circuit Current			-3.5	-5	mA
I_{OS}	Output Short Circuit Current			-3.5	-5	mA
V_{OH}	Output Voltage High			1.34	1.6	V
V_{OL}	Output Voltage Low		0.9	1.06		V

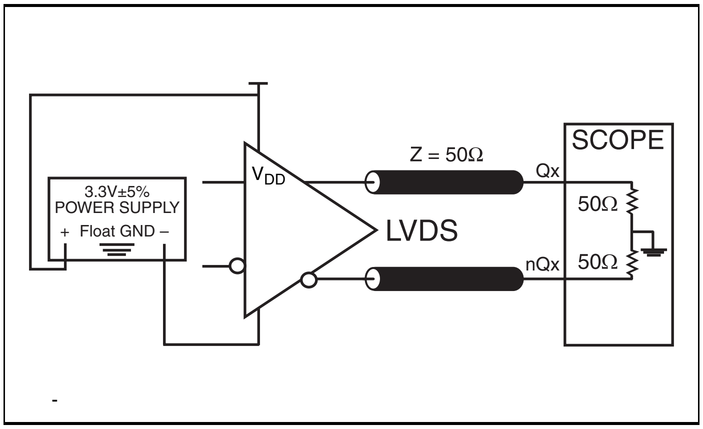
AC Electrical Characteristics

Table 5. AC Characteristics, V_{DD} = 3.3V ± 5%, T_A = 0°C to 70°C

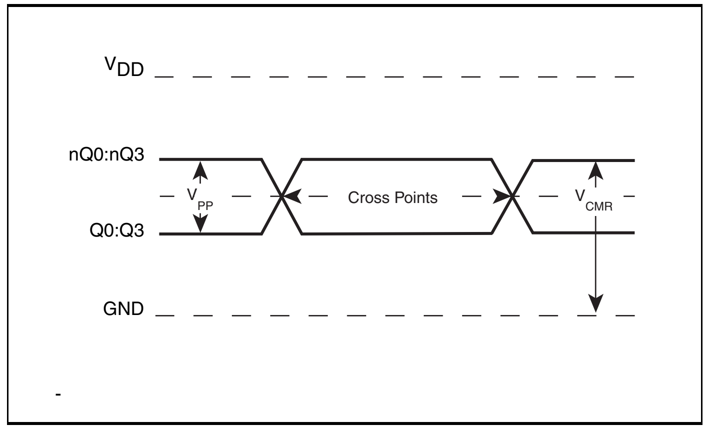
Parameter	Symbol	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				650	MHz
t_{PD}	Propagation Delay; NOTE 1		1.4		3.6	ns
*t*sk(o)	Output Skew; NOTE 2, 4				40	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				500	ps
t_R / t_F	Output Rise/Fall Time	20% to 80% @ 50MHz	150		500	ps
odc	Output Duty Cycle	$f \leq$ 266MHz	45		55	%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from V_{DD}/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at V_{DD}/2 of the input to the differential output crossing point.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions.
Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

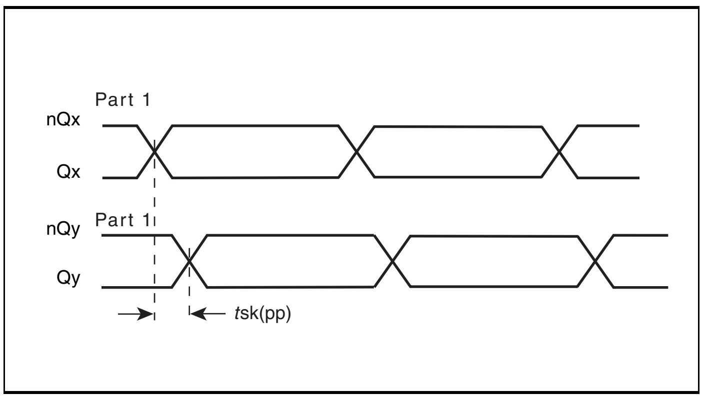
Parameter Measurement Information



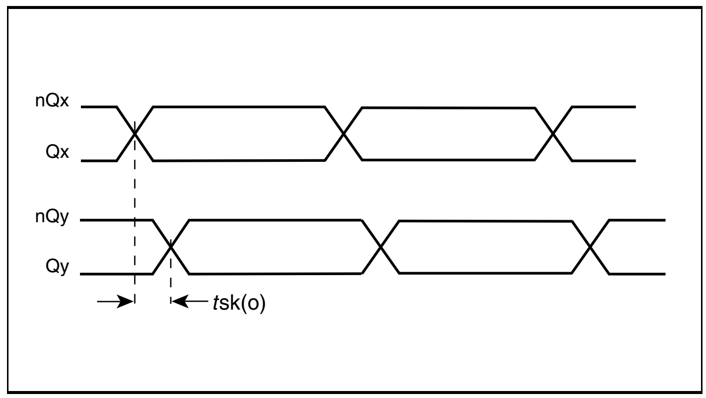
3.3V LVDS Output Load AC Test Circuit



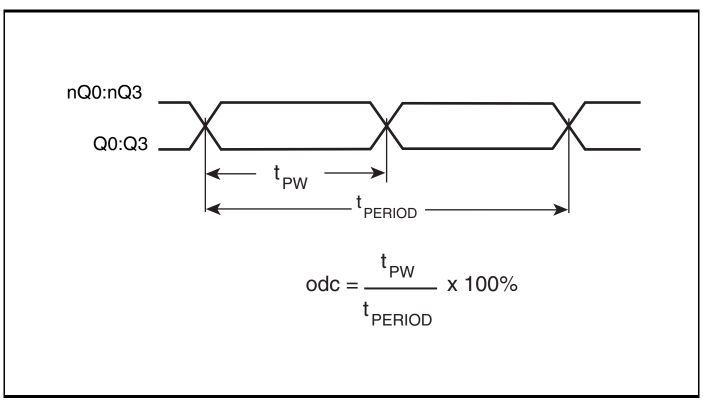
Differential Output Level



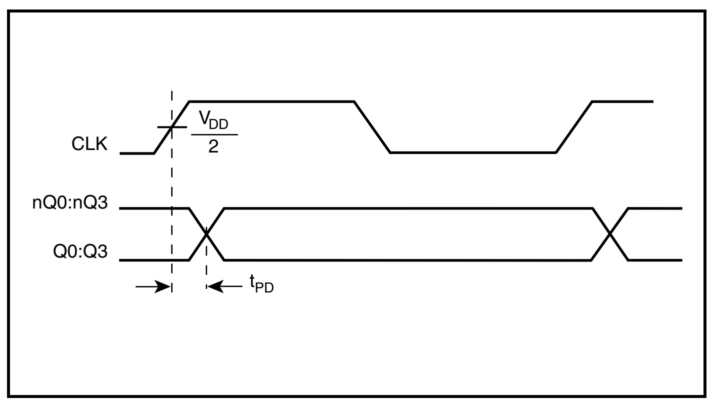
Part-to-Part Skew



Output Skew

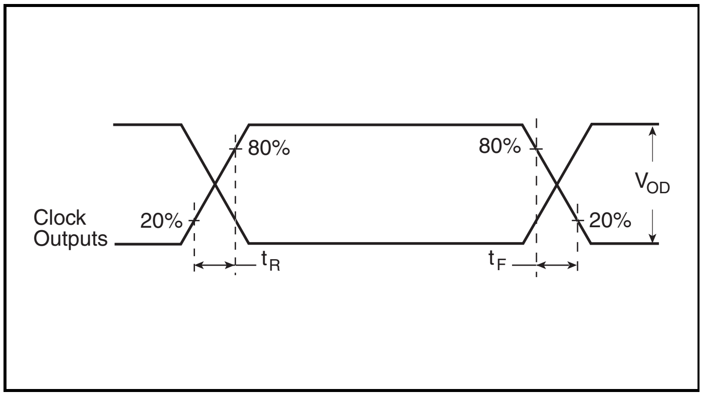


Output Duty Cycle/Pulse Width/Period

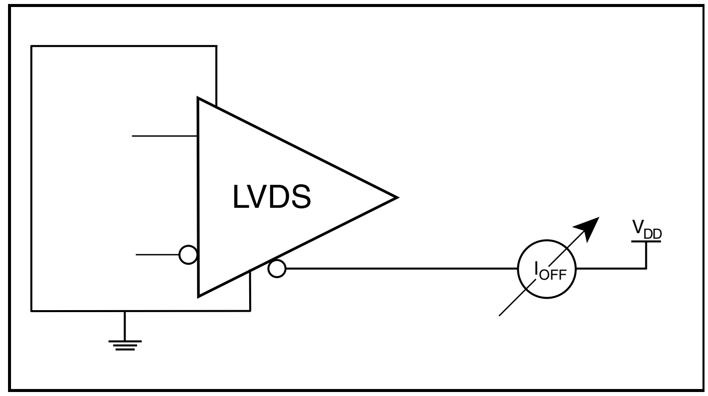


Propagation Delay

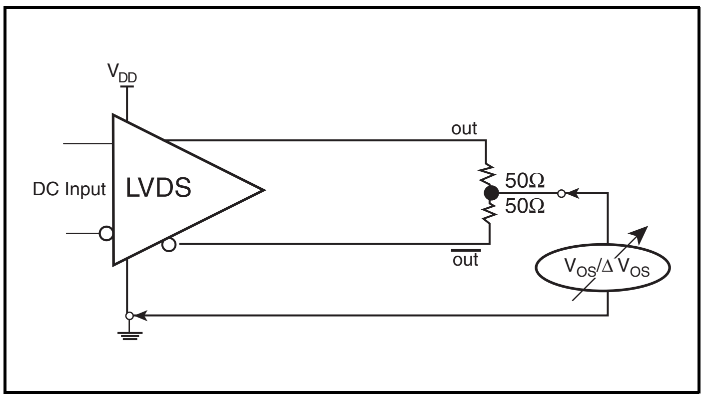
Parameter Measurement Information, continued



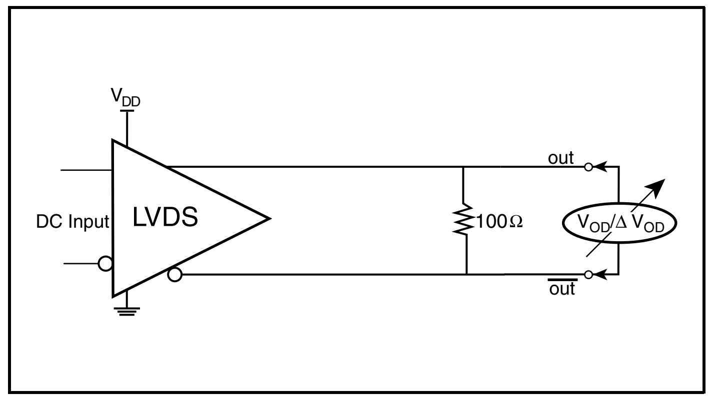
Output Rise/Fall Time



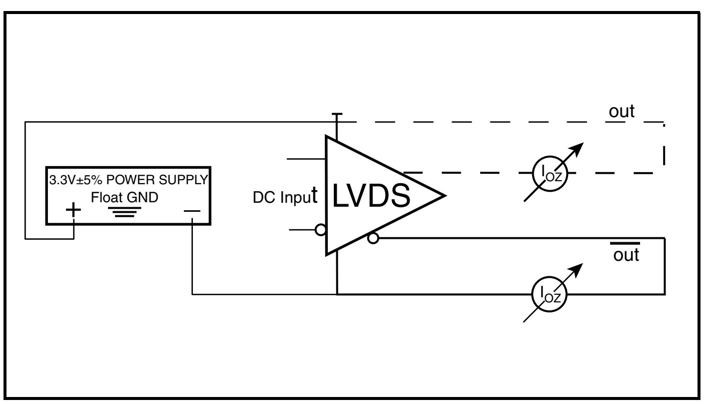
Power Off Leakage Setup



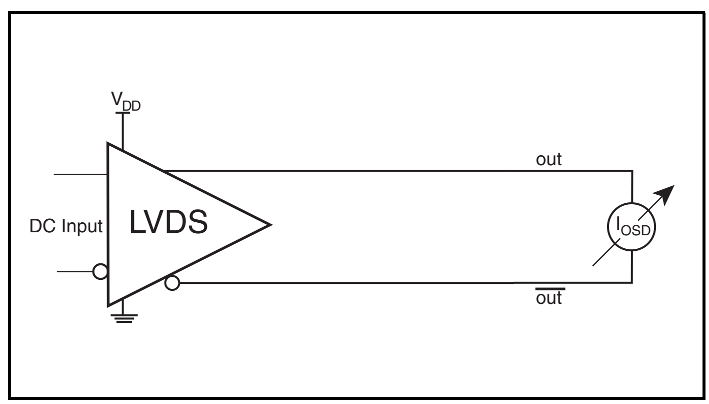
Offset Voltage Setup



Differential Output Voltage Setup

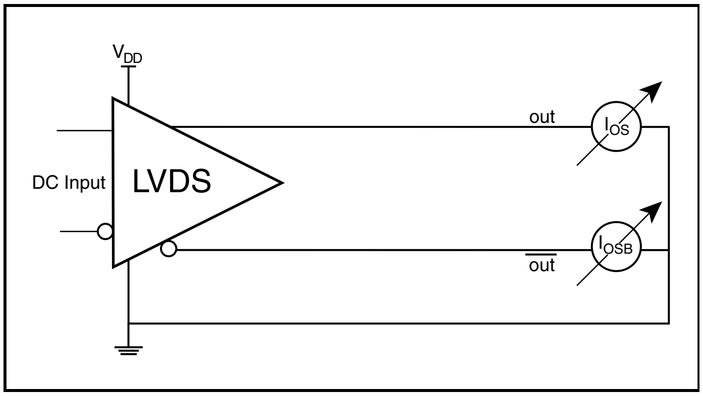


High Impedance Leakage Current Setup



Differential Output Short Circuit Setup

Parameter Measurement Information, continued



Output Short Circuit Current Setup

Application Information

Recommendations for Unused Output Pins

Outputs:

LVDS Outputs

All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS Driver Termination

A general LVDS interface is shown in Figure 1. In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input.

For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.

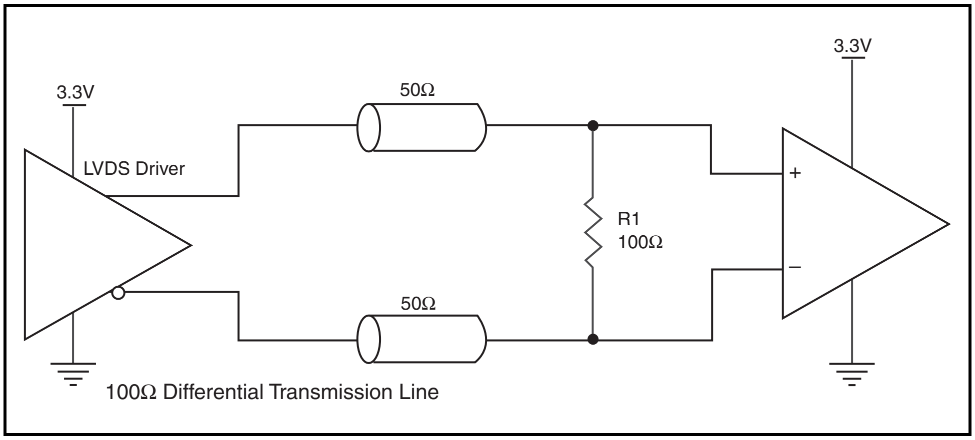


Figure 1. Typical LVDS Driver Termination

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8545-01.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS8545-01 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{DD\_MAX} * I_{DD\_MAX}$ = 3.465V * 50mA = **173.25mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 91.1°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.173W * 91.1°C/W = 85.7°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 6. Thermal Resistance θ_{JA} for 20 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters Per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

Reliability Information

Table 7. θ_{JA} vs. Air Flow Table for a 20 Lead TSSOP

θ_{JA} by Velocity			
Meters Per Second	**0**	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	91.1°C/W	86.7°C/W	84.6°C/W

Transistor Count

The transistor count for ICS8545-01 is: 644

Package Outline and Package Dimension

Package Outline - G Suffix for 20 Lead TSSOP

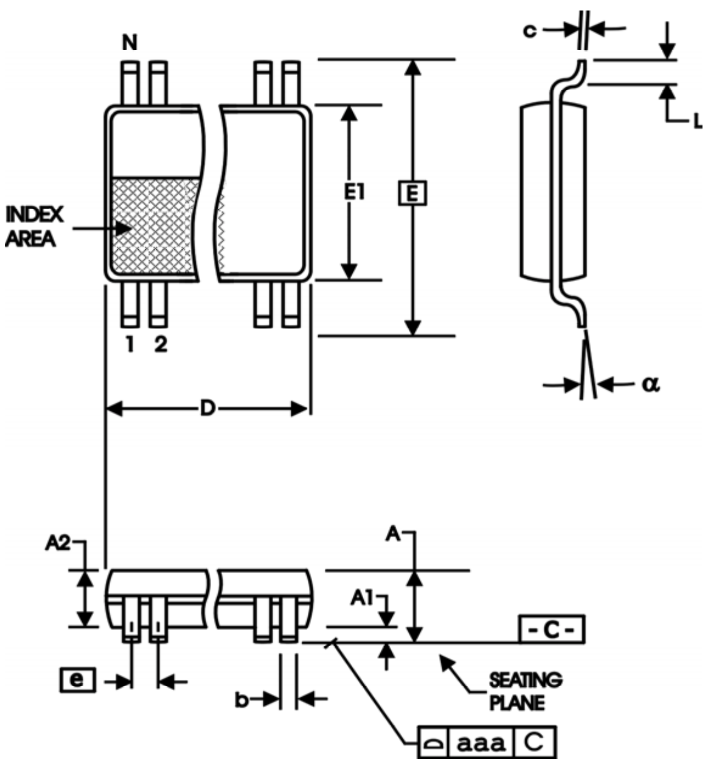


Table 8. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	20	
A		1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	6.40	6.60
E	6.40 Basic	
E1	4.30	4.50
e	0.65 Basic	
L	0.45	0.75
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-153

Ordering Information

Table 9. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8545AG-01	ICS8545AG-01	20 Lead TSSOP	Tube	0°C to 70°C
8545AG-01T	ICS8545AG-01	20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C
8545AG-01LF	ICS8545AG01L	"Lead-Free" 20 Lead TSSOP	Tube	0°C to 70°C
8545AG-01LFT	ICS8545AG01L	"Lead-Free" 20 Lead TSSOP	2500 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Innovate with IDT and accelerate your future networks. Contact:

www.IDT.com

For Sales
800-345-7015
408-284-8200
Fax: 408-284-2775

For Tech Support
netcom@idt.com
480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800 345 7015
+408 284 8200 (outside U.S.)

Asia Pacific and Japan
Integrated Device Technology
Singapore (1997) Pte. Ltd.
Reg. No. 199707558G
435 Orchard Road
#20-03 Wisma Atria
Singapore 238877
+65 6 887 5505

Europe
IDT Europe, Limited
321 Kingston Road
Leatherhead, Surrey
KT22 7TU
England
+44 (0) 1372 363 339
Fax: +44 (0) 1372 378851

www.IDT.com