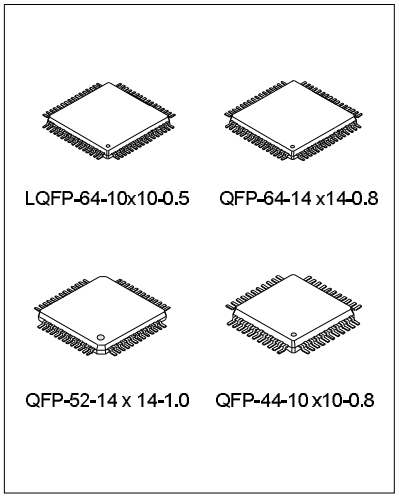
8-BIT MCU FOR REMOTE CONTROLLER WITH LCD DRIVER(OTP)

DESCRIPTION

SC65C03P08 is a single-chip CMOS microcontroller (OTP) with LCD display. It adopts 8-bit MCU core, and can be used in the field of remote controller with LCD display.



FEATURES

* OTP 8192*8 BITS
* RAM 128 * 8 BITS
* LCD 32SEGMENTS, 4 COMMONS
* Built-in booster pump
* Crystal oscillator frequency is 32.768KHz, and built-in RC OSC.
* Built-in low voltage detection and power on reset circuit.

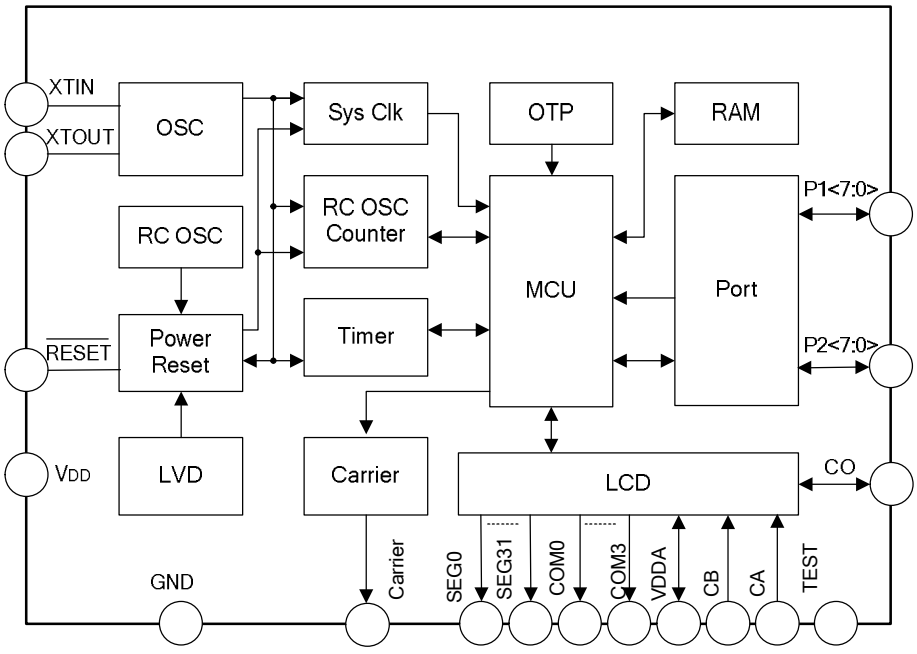
APPLICATIONS

* TV remote controller
* DVD remote controller
* Air-condition remote controller

ORDERING INFORMATION

Device	Package
SC65C03P08	LQFP-64-10x10-0.5
SC65C03P08A	QFP-64-14x14-0.8
SC65C03P08B	QFP-52-14×14-1.0
SC65C03P08C	QFP-44-10x10-0.8

BLOCK DIAGRAM



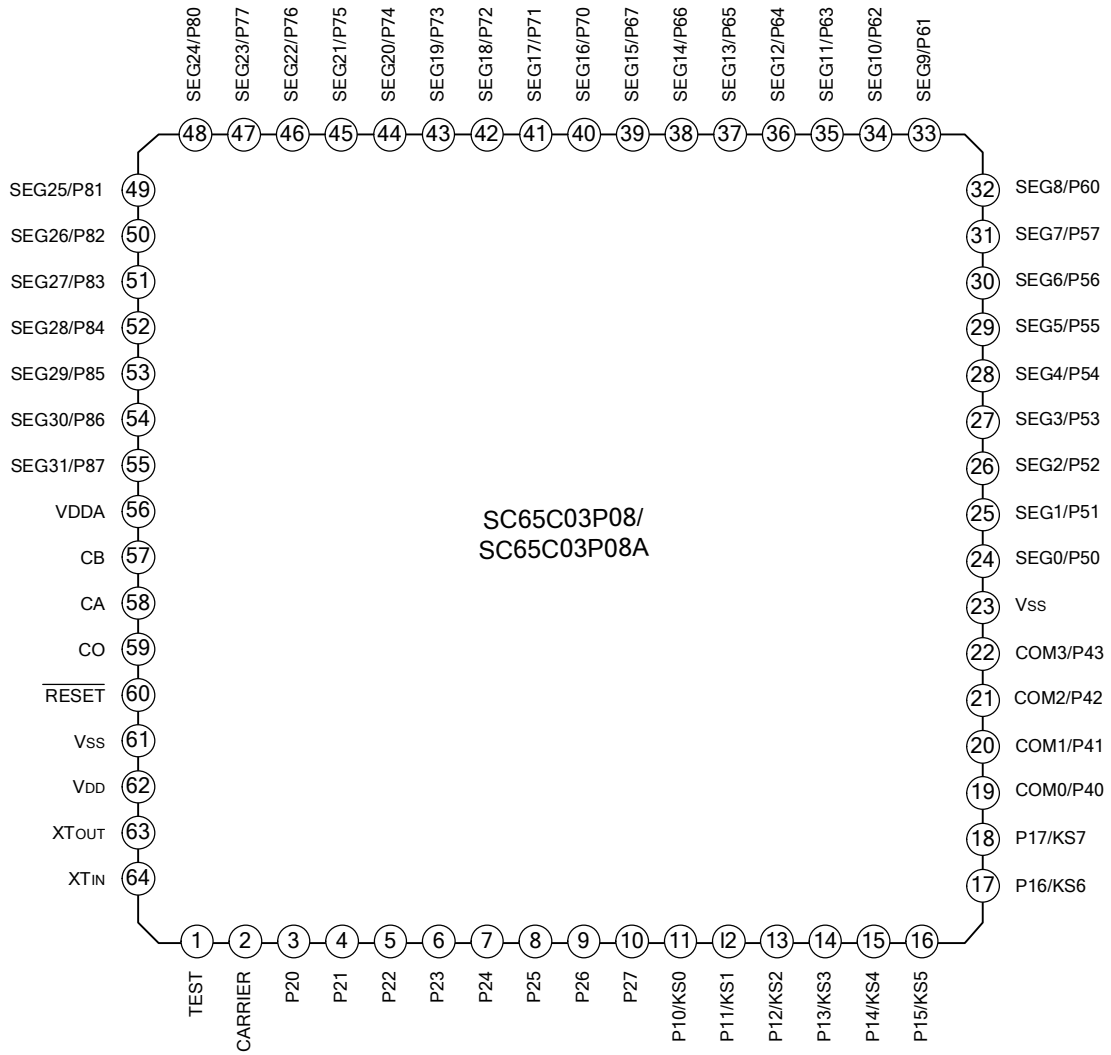
ABSOLUTE MAXIMUM RATING (T_{amb}=25°C)

Characteristics	Symbol	Rating	Unit
Operating Voltage	V_{DD}	-0.3 ~ +5.0	V
Input Voltage	V_{IN}	-0.3 ~ V_{DD} + 0.3	V
Output Current of Code Sending(VOH=2.7V)	P30	8	mA
Storage Temperature	T_{stg}	-65 ~ +150	°C
Operating Temperature	T_{opr}	-40 ~ + 80	°C

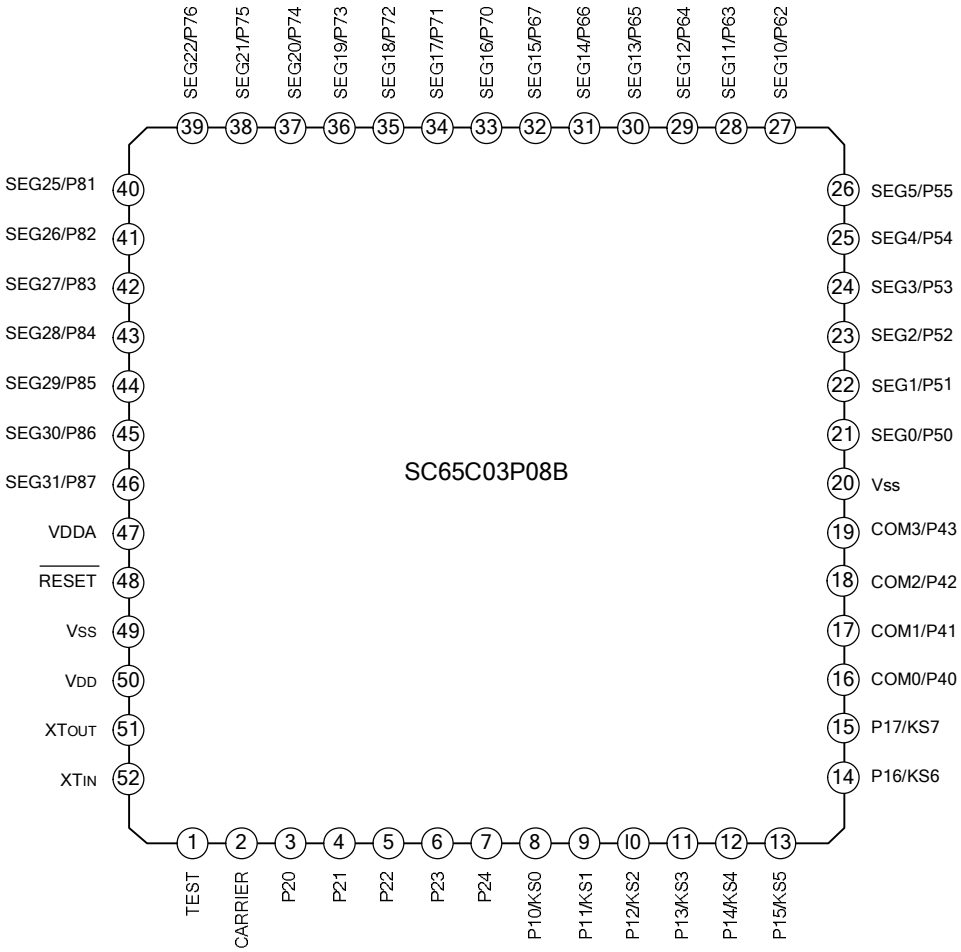
ELECTRICAL CHARACTERISTICS (unless otherwise specified, T_{amb}= -40~85°C, V_{DD}=2.0~3V)

Characteristics	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Operating Voltage	V_{DD}		2.2	--	4.0	V
Operating Current 1	$I_{DD}1$	V_{DD}=3V; T_{amb}=25°C RC OSC operating	--	1.2	2	mA
Operating Current 2	$I_{DD}2$	V_{DD}=3V; T_{amb}=25°C 32.768k OSC operating, CPU sleep	--	8	15	μA
Oscillate Frequency	F_{OSC}		--	--	4M	MHz
Input Pull-up Resistor	R		50	100	150	K
High Level Input Voltage	V_{IH}	V_{DD} = 3V	0.7V_{DD}	--	V_{DD}	V
Low Level Input Voltage	V_{IL}	V_{DD} = 3V	--	--	0.3V_{DD}	V
High Level Output Voltage	V_{OH}	V_{DD} = 3V	2.7	--	--	V
High Level Output Voltage	V_{OL}	V_{DD} = 3V		--	0.3	V
High Level Drive Current	I_{OH}	V_{DD} = 3V V_{OH} = 2.7V	--	--	-1	mA
Low Level Drive Current	I_{OL}	V_{DD} = 3V V_{OL}= 0.3V	--	--	1	mA

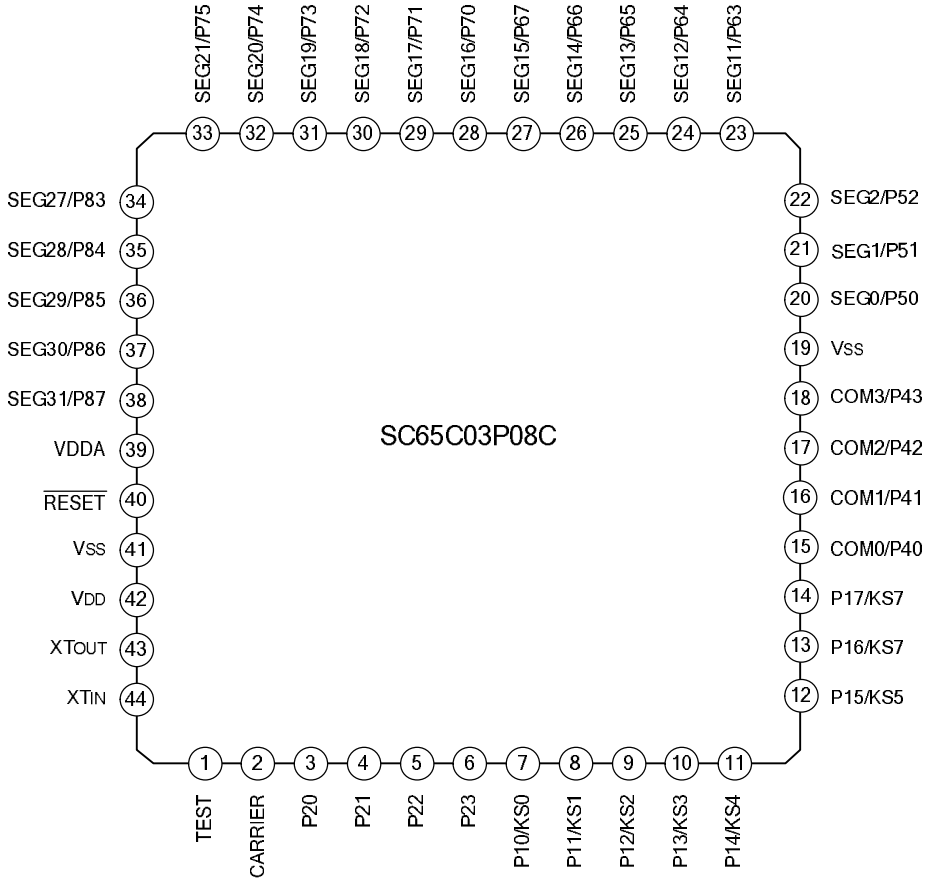
PIN CONFIGURATION



PIN CONFIGURATION (Continued)



PIN CONFIGURATION (Continued)



PIN DESCRIPTION

Pin no.			Pin Name	PIN DESCRIPTION
64 pins	52 pins	44 pins		
1	1	1	TEST	Low level enter test mode
2	2	2	CARRIER	Carrier output pin
3~6	3~6	3~6	P20 ~P23	I/O
7	7	--	P24	I/O
8	--	--	P25	I/O, also as buzzer output
9	--	--	P26	I/O, also as high level interrupt input
10	--	--	P27	I/O, also as low level interrupt input
11~18	8~15	7~14	P10/KS0~ P17/KS7	Keyboard input pin, with pull-up resistor. It also can be I/O ports.
19~22	16~19	15~18	COM0/P40~ COM3/P43	LCD COM segment, it also can be I/O ports.
23	20	19	VSS	Ground.
24~26	21~23	20~22	SEG0/P50~ SEG2/P52	I/O ports
27~29	24~26	--	SEG3/P53~ SEG5/P55	I/O ports
30~33	--	--	SEG6/P56~ SEG9/P61	I/O ports
34	27	--	SEG10/P62	I/O ports
35~45	28~38	23~33	SEG11/P63~ SEG21/P75	I/O ports
46	39	--	SEG22/P76	I/O ports
47	--	--	SEG23/P77	I/O ports
48	--	--	SEG24/P80	I/O ports
49~50	40~41	--	SEG25/P81~ SEG26/P82	I/O ports
51~55	42~46	34~38	SEG27/P83~ SEG31/P87	I/O ports
56	47	39	VDDA	Analog power supply.
57	--	--	CB	Charge pump capacitor B.
58	--	--	CA	Charge pump capacitor A.
59	--	--	CO	Charge pump output.
60	48	40	$\overline{\text{RESET}}$	Low level reset pin
61	49	41	VSS	Digit ground.
62	50	42	VDD	Digit power supply.
63	51	43	XTOUT	32KHz crystal oscillator output pin.
64	52	44	XTIN	32KHz crystal oscillator input pin.

OTP PIN DESCRIPTION

Pin name	OTP pin name	OTP pin descriptions
P22	OE_IN	OTP output enable pin , high level active.
P20	PROGB	OTP program enable pin, high level active.
P21	PcCtrl	The address of MCU add 1, high pulse active.
TEST	VPP	The input voltage of download is 12.5V.
VDD	VCC	The operating voltage of download is 6.5V.
VSS	VSS	GND
$\overline{\text{RESET}}$	PcRST	The address of MCU reset.
P10/KS0	D0	OTP data 0 I/O pin.
P11/KS1	D1	OTP data 1 I/O pin.
P12/KS2	D2	OTP data 2 I/O pin.
P13/KS3	D3	OTP data 3 I/O pin.
P14/KS4	D4	OTP data 4 I/O pin.
P15/KS5	D5	OTP data 5 I/O pin.
P16/KS6	D6	OTP data 6 I/O pin.
P17/KS7	D7	OTP data 7 I/O pin.

FUNCTION DESCRIPTION

CPU core illustration:

1. **Address:**

   The address of special function register is 0X00~0X7F;

   RAM 128 BYTES, and the address is 0X80~0X17F;

   OTP 8K BYTES, and the address is E000H-FFFFH.

2. **Interrupts:**

   All the interrupts there have no priority level; there are 6 interrupts:

   Interrupt 2: 16 bits timer interrupt;

   Interrupt 3: key interrupt;

   Interrupt 4: frequency counter timer interrupt;

   Interrupt 5: real time clock interrupt;

   Interrupt 6: external rising edge interrupt;

   Interrutp7: external falling edge interrupt;

Register descriptions:

IRQ interrupt mask register (16'h0000):

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Mask7	Mask6	Mask5	Mask4	Mask3	Mask2	Mask1	Mask0

Bit7~0: IRQ interrupt mask bit

0: Enable

1: Disable (Default)

IRQ interrupt source register (16'h0001):

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
$\overline{\text{EXTINT1}}$	EXTINT0	RTCINT	FCTINT	KEYINT	TimerINT	---	---

BIT7-BIT2: when the interrupt generates, the corresponding bit is set to 1, if writing data to this bit, the interrupt source is cleared. In addition, bit2 of PSW is the Irq enable bit, when this bit is 0, the interrupt stored in the interrupt source register is active. Irq is rising edge active.

Interrupt enter address: FFF8H, FFF9H

RESET enter address: FFFAH, FFFBH

3. WDT descriptions

The WDT is always work and can not be shut off, all the operations to WDT are focus on three registers:

WDT clear register

09H	WDT_CLR0	W
0AH	WDT_CLR1	W

WDT set up register (16'h0004):

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
---	---	---	---	---	---	Ctrl1	Ctrl0

bit1~0: it is used to set the overflow time of WDT, the default mode is 10

00: MCLK/2^{14}

01: MCLK/2^{15}

10: MCLK/2^{16}

11: MCLK/2^{17}

bit7~2: unused

Example : clear WDT

WDT_CLR0 write in 00H

WDT_CLR1 write in 00H

WDT_CLR0 write in 53H

WDT_CLR1 write in ACH

Finish

4. system control register

Sleep control register（16'h0010）:

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
---	---	---	---	---	32KEN	lowdtEn	Sleep

Bit0: system sleep control bit

0: the system is in the normal mode (default)

1: control system enter sleep mode

Bit1: low power detect control bit

0: low power detect not work

1: enable low power detect

Bit2: 32.768k oscillator control

0: shut off 32.768k oscillator

1: enable 32.768k oscillator

Bit7~3: unused;

Periphery resource illustration

1. BUZZ output

P16 pin can output 2KHz, 4KHz, 8KHz, 16KHz BUZZ signal, and the control registers are as following:

Buzz control register (3FH)

BIT7: "0": inhibit BUZZ output signal

"1": enable BUZZ output signal

BIT6, 5: "00": 2KHz BUZZ signal output

"01": 4KHz BUZZ signal output

"10": 8KHz BUZZ signal output

"11": 16KHzBUZZ signal output

BIT4.3: unused

Bit2: Double voltage circuit bias enable signal and high active.

Bit1: LCD clock enable signal and high active.

Bit0: Double voltage circuit clock enable signal and high active.

2. LCD controller/driver

LCD includes 32 segments and 4 common outputs, all segments and commons share with GPIO.

LCD RAM (40H-4FH)

The following 16 registers store 32 SEGs, and corresponding 4 COM segments, 32*4 segments totally.

BIT / REG, OUTPUT			COM3 7	COM2 6	COM1 5	COM0 4	COM3 3	COM2 2	COM1 1	COM0 0
SEG01_00	SEG1	SEG0	1/0				1/0			
SEG03_02	SEG3	SEG2	1/0				1/0			
SEG05_04	SEG5	SEG4	1/0				1/0			
SEG07_06	SEG7	SEG6	1/0				1/0			
SEG09_08	SEG9	SEG8	1/0				1/0			
SEG11_10	SEG11	SEG10	1/0				1/0			
SEG13_12	SEG13	SEG12	1/0				1/0			
SEG15_14	SEG15	SEG14	1/0				1/0			
SEG17_16	SEG17	SEG16	1/0				1/0			
SEG19_18	SEG19	SEG18	1/0				1/0			
SEG21_20	SEG2	SEG20	1/0				1/0			
SEG23_22	SEG22	SEG21	1/0				1/0			
SEG25_24	SEG24	SEG23	1/0				1/0			
SEG27_26	SEG26	SEG25	1/0				1/0			
SEG29_28	SEG28	SEG27	1/0				1/0			
SEG31_30	SEG31	SEG30	1/0				1/0			
INITIAL VALUE			--				--			

LCD control register (3AH)

The control register is used to control LCD driver operating mode.

REG	B7	B6	B5	B4	B3	B2	B1	B0
LCD_CTRL	Not used		LCD_FREQ[1:0]		LCD_EN	--	DUTY[1：0]	
INITIAL VALUE	--		00		0	--	11	

- **LCD_FREQ [1:0] (B[5:4])**

  This two bits are used to control LCD driver internal clock; LCD drive output frame frequency:

  Frame_FREQ = LCD_FREQ * Duty Ratio.

  When LCD_FREQ [1:0] = (0, 0):1K Hz

  = (0, 1): 512 Hz

  = (1, 0): 256 Hz

  = (1, 1): 128 Hz

- **LCD_EN (B3)**

  This bit is the enable bit of LCD driver, 0: inactive; 1: enable.

- **DUTY [1:0] (B[1:0]):**

  These two bits control DUTY mode of LCD driver:

  When DUTY = (0, 0): static (COM0)

  = (0, 1): 1/2 (COM0 - COM1)

  = (1, 0): 1/3 (COM0 - COM2)

  = (1, 1): 1/4 (COM0 - COM3)

LCD segment control register (3BH,30H-37H)

The following 9 registers determined the PAD is LCD drive port or GPIO port, and it is also used to control GPIO input or output.

REG	B7	B6	B5	B4	B3	B2	B1	B0
COM_CTRL (3BH)	P4_IEN[3]	P4_IEN[2]	P4_IEN[1]	P4_IEN[0]	COM_EN[3]	COM_EN[2]	COM_EN[1]	COM_EN[0]
SEG_CTRL0 (30H)	P5_IEN[3]	P5_IEN[2]	P5_IEN[1]	P5_IEN[0]	SEG_EN[3]	SEG_EN[2]	SEG_EN[1]	SEG_EN[0]
SEG_CTRL1 (31H)	P5_IEN[7]	P5_IEN[6]	P5_IEN[5]	P5_IEN[4]	SEG_EN[7]	SEG_EN[6]	SEG_EN[5]	SEG_EN[4]
SEG_CTRL2 (32H)	P6_IEN[3]	P6_IEN[2]	P6_IEN[1]	P6_IEN[0]	SEG_EN[11]	SEG_EN[10]	SEG_EN[9]	SEG_EN[8]
SEG_CTRL3 (33H)	P6_IEN[7]	P6_IEN[6]	P6_IEN[5]	P6_IEN[4]	SEG_EN[15]	SEG_EN[14]	SEG_EN[13]	SEG_EN[12]
SEG_CTRL4 (34H)	P7_IEN[3]	P7_IEN[2]	P7_IEN[1]	P7_IEN[0]	SEG_EN[19]	SEG_EN[18]	SEG_EN[17]	SEG_EN[16]
SEG_CTRL5 (35H)	P7_IEN[7]	P7_IEN[6]	P7_IEN[5]	P7_IEN[4]	SEG_EN[23]	SEG_EN[22]	SEG_EN[21]	SEG_EN[20]
SEG_CTRL6 (36H)	P8_IEN[3]	P8_IEN[2]	P8_IEN[1]	P8_IEN[0]	SEG_EN[27]	SEG_EN[26]	SEG_EN[25]	SEG_EN[24]
SEG_CTRL7 (37H)	P8_IEN[7]	P8_IEN[6]	P8_IEN[5]	P8_IEN[4]	SEG_EN[31]	SEG_EN[30]	SEG_EN[29]	SEG_EN[28]
INITIAL VALUE	0	0	0	0	1	1	1	1

- **PX_IEN [7：0]**

  This bit control 5 GPIO ports input/output; 0: output port; 1: input port.

- **COM_EN[3：0]**

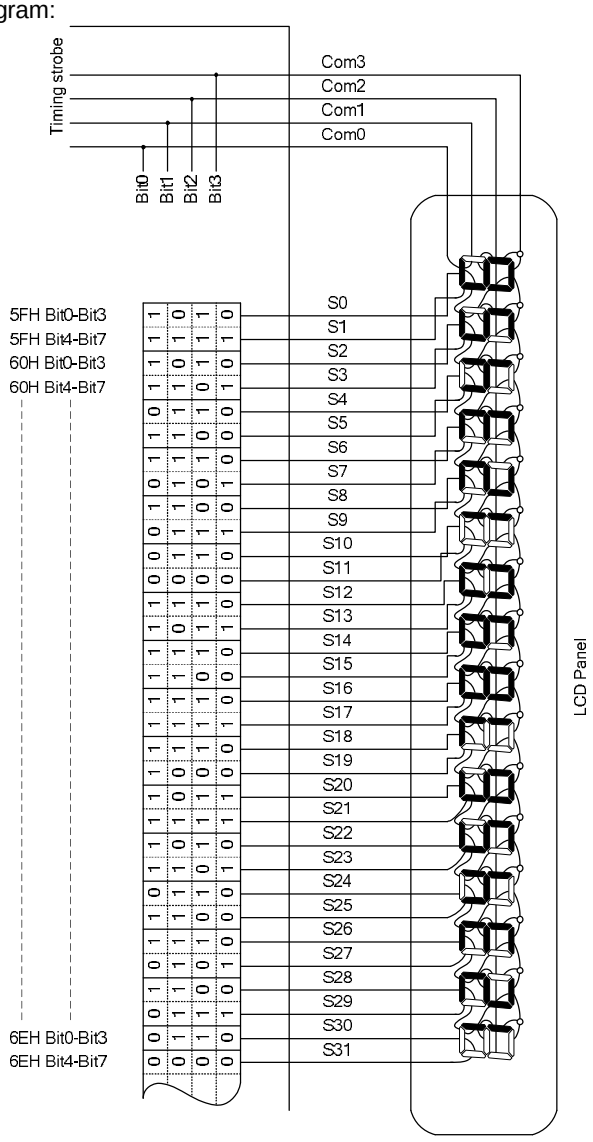
  This bit defines the corresponding PAD port: 0: GPIO; 1: COM.

- **SEG_EN[31：0]**

  This bit defines the PAD port: 0: GPIO; 1: SEG.

VLCD select									
Add	register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3DH	VLCD	--	--	VLCDS EL[5]	VLCDS EL[4]	VLCDS EL[3]	VLCDS EL[2]	VLCDS EL[1]	VLCDS EL[0]
LCD operating voltage select		--	--	3．0V	2.9V	2.8V	2.7V	2.6V	2.5V
		X	X	0	1	1	1	1	1

LCD board schematic diagram:



3. 16 bits Timer/Counter

The 16-bits Timer is divided by High Byte and Low Byte for the execution of 8 bits 6502 MCU-core. However, it is deserve reminding of the user there is only one 16 bits Timer.

Timer (16bits is divided by 2 8 bits partitions)									
Add.	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
60H	TIMER_TG1 (TIMER_TH)	Write time data to timer1(Timer High part), when count to this value, the timer generate interrupt.							
61H	TIMER_TG2 (TIMER_TL)	Write time data to timer2(Timer Low part), when count to this value, the timer generate interrupt.							
62H	TIMER_CON	X	X	X	X	TIMER_Enable ‘1’ Enable ‘0’ Disable	CLK_SEL		
							000	MClk	
							001	MClk_2	
							010	MClk_4	
							011	MClk_8	
							100	MClk_16	
							101	MClk_32	
							110	OSC32K	
							111	OSC4096T	

Note: MCLK : MCLK=RCOSC

4. PORT

The IC in 64-pin package has 53 I/O ports, where P2 can be input key, with pull-up resistor, 36 I/O ports shared with SEG and COM segments.

P1 port data register								
Add.	BIT7	BIT6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
64H	P17	P16	P15	P14	P13	P12	P11	P10

P1 port direction control register									
Add.	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
65H	P1CON	P17	P16	P15	P14	P13	P12	P11	P10
		“1” output; ”0” input							

P1 pull-up select register									
Add	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
3EH	P1UP	P17	P16	P15	P14	P13	P12	P11	P10
		“0” pull up; “1” not pull up							

P2 direction control register									
Add	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
69H	P2CON	P27	P26	P25	P24	P23	P22	P21	P20
		0: input; 1: output							

P2 port data register								
Add	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
68H	P27	P26	P25	P24	P23	P22	P21	P20

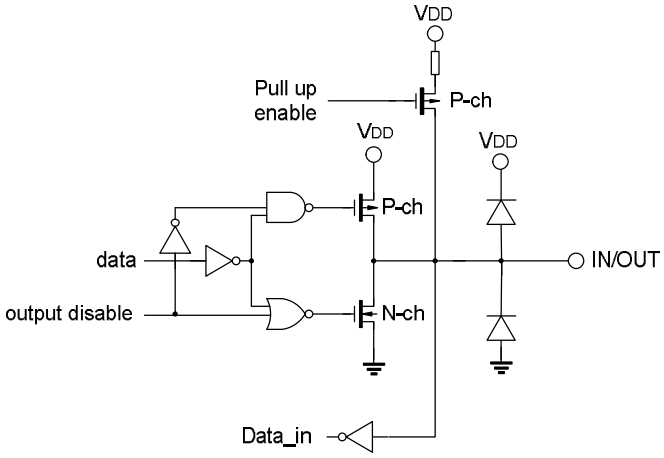
Data register for GPIO P4, P5, P6, P7, P8 (2AH-2EH).

The following 5 registers store 5 GPIO ports data.

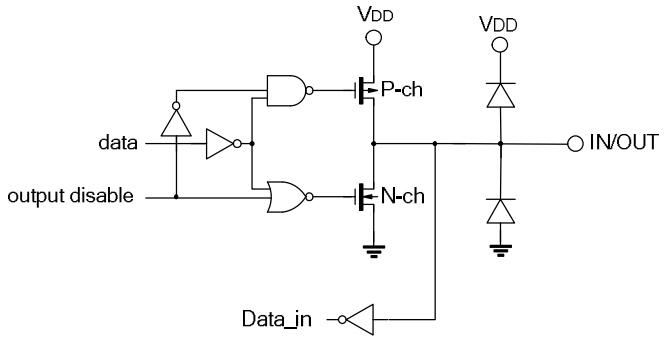
REG	B7	B6	B5	B4	B3	B2	B1	B0
DATA_P4	--	--	--	--	DATA_P4[3]	DATA_P4[2]	DATA_P4[1]	DATA_P4[0]
DATA_P5	DATA_P5[7]	DATA_P5[6]	DATA_P5[5]	DATA_P5[4]	DATA_P5[3]	DATA_P5[2]	DATA_P5[1]	DATA_P5[0]
DATA_P6	DATA_P6[7]	DATA_P6[6]	DATA_P6[5]	DATA_P6[4]	DATA_P6[3]	DATA_P6[2]	DATA_P6[1]	DATA_P6[0]
DATA_P7	DATA_P7[7]	DATA_P7[6]	DATA_P7[5]	DATA_P7[4]	DATA_P7[3]	DATA_P7[2]	DATA_P7[1]	DATA_P7[0]
DATA_P8	DATA_P8[7]	DATA_P8[6]	DATA_P8[5]	DATA_P8[4]	DATA_P8[3]	DATA_P8[2]	DATA_P8[1]	DATA_P8[0]
INITIAL VALUE	0	0	0	0	0	0	0	0

I/O circuit of respective pins

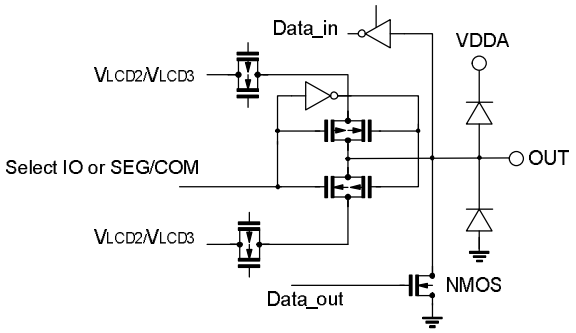
PORT1 pin description:



PORT2 pin description:



SEG/COM PINS:



5. Carrier generator

The carrier generator can provide the carrier with adjustable duty. The input clock is RC OSC output frequency, and the high or low level of carrier is determined by low 7 bits of register6BH,, 6CH. The carrier sending data is stored in the BIT7 of register 6BH and BIT7 of register6CH is enable bit.

CARRIER									
Add	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6BH	Carrier control register (CARRY_CON0)	Data bit	High level control bit						
6CH	Carrier control register (CARRY_CON1)	Enable bit	Low level control bit						

BIT7: carrier enable bit: “1”, enable carrier generator working; “0”, inactive

6. RC OSC frequency calculation

The module can calculate the frequency of RC OSC. It includes one 8 bits reference time counter(counter clock is32768Hz or 4096Hz) and 16 bits RC OSC frequency counter (count clock is RC OSC output frequency), the operation principle is as follows: first write data to reference time register 6DH, then start reference time counter, the counter adds 1(RC counter begin to count at the same time), when the reference time counter overflows, the system generates interrupt. Then read out the data of RC frequency counter（high 8 bits in register RCCOUNTH_LOAD, low 8 bits in register RCCOUNTL_LOAD）, and get the RC OSC frequency after calculation.

Reference time register of RC OSC counter									
Add	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6DH	OSCCOUNT_LOAD								

Register of RC OSC frequency counter									
Add	Register	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
6EH	RCCOUNTL_LOAD								
6FH	RCCOUNTH_LOAD								

Calculate control register of RC OSC				
Add	Register	Bit2	Bit1	Bit0
70H	RCOSC_CN	RC frequency counter overflow flag bit	Reference time counter frequency select bit: 32768HZ; 0:4096HZ	RC OSC calculate start bit

BIT0: RC OSC calculate start bit, “1” : start.

7. Real time clock RTC

The real-time clock circuit provides the timing of year, month, day, week, hour, minute, and second. It also has the function of leap year automatic switchover. And the alarm function can send alarm interrupts in given week, day, hour, and minute, also it can providing time alarm interrupt and timer interrupt. Its 8-bit timer can send timer interrupt.

RTC output a programmable clock pulse for high precision clock adjustment.

Calendar function

The calendar circuit providing clock/calendar function, the coding format is BCD. It also has leap year automatic switchover function. It can read and set the clock data through 6502 interface.

Alarm function

The alarm provides week, data, hour, minute time alarm function. When clear the alarm enable bit, the corresponding alarm is active, it will generate one time at every day or every week. If the condition is according with the alarm condition, set the alarm flag bit AF, produce the interrupt, AF only can be soft cleared. So , the alarm enable bit AIE control interrupt.

Timer

8 bits down counter is controlled by timer control register which is used to control timer ON/OFF, and set the count frequency (4096Hz, 64Hz, 1Hz, 1/60Hz) . The timer begins to count at the given value, after counts end, the timer set the flag TF which is only cleared by software. TF flag bit is used to produce interrupt, and time interrupt enable bit TIE control the interrupt.

Register address and definition

Control/status register (RTC_CS), address: 50H

BIT	Signal	Descriptions
5	STOP	STOP=0: chip clock run; STOP=1: the divider of chip clock stop run, chip clock stop. And no calendar clock at this time.
4	TI/TP	TI/TP=0: edge interrupt; TI/TP=1: level interrupt. Note: if AF and AIE are all active, INT is level interrupt (because the alarm interrupt is level interrupt, and the alarm has been shielded)
3	AF(alarm flag bit)	When alarm occurs, AF is set up, and it only can cleared by software After one second.
2	TF(timer flag bit)	When timer count end, TF is set up, and it only can cleared by software.
1	AIE(alarm interrupt enable bit)	AIE=0: alarm interrupt inactive; AIE=1: alarm interrupt active;
0	TIE(Timer interrupt enable bit)	TIE=0: timer interrupt inactive; TIE=1: timer interrupt active.

Calendar/clock register, address: 51H~58H

58H	YEARL	00 ~ 99 BCD code format					
57H	MON				01 ~ 12 BCD code		
56H	WEEK						0 ~ 6
55H	DAY			01 ~ 31 BCD code			
54H	HOUR			00 ~ 23 BCD code			
53H	MIN		00 ~ 59 BCD code				
52H	SEC		00 ~ 59 BCD code				
51H	YEARH	00 ~ 99 BCD code					

Alarm register, address: 59H~5CH

The alarm register includes minute, hour, day, and week register. When one or more alarm registers are wrote to minute, hour, day week data, and the corresponding AE bit is logical “0”, if these data is the same as the current minute, hour, day, week, the alarm flag bit AF is set up. AF remain high level until it is cleared by software, and only when the writing data (minute, hour, day and etc.) is match to the alarm conditions, the AF is set up again. When the AE bit is logical “1”, the alarm conditions can be ignored.

Minute alarm register : address: 59H

BIT	Signal	Descriptions
7	AE	AE=0: minute alarm active; AE=1: minute alarm inactive;
6~0	min_alarm	BCD code format minute alarm data

Hour alarm register : address: 5AH

BIT	Signal	Descriptions
6	AE	AE=0: hour alarm active; AE=1: hour alarm inactive;
5~0	hour_alarm	BCD code format hour alarm data

Day alarm register : address: 5BH

BIT	Signal	Descriptions
6	AE	AE=0: day alarm active; AE=1: day alarm inactive;
5~0	day_alarm	BCD code format day alarm data

Week alarm register: address: 5CH

BIT	Signal	Descriptions
3	AE	AE=0: week alarm active; AE=1: week alarm inactive;
2~0	week_alarm	BCD code format week alarm data

CLKOUT frequency register, address: 5DH

BIT	Signal	Descriptions
7-3	-----	Inactive
2	FE	FE=0: CLKOUT output inhibit, and it is set to high resistance output; FE=1:CLKOUT output active(select 1, 32, 1024, 32768Hz)
1	FD1	FD1, FD0 select CLKOUT output frequency: {FD1, FD0}=11: 1Hz {FD1, FD0}=10 : 32Hz {FD1, FD0}=01: 1024Hz {FD1, FD0}=00: 32768Hz
0	FD0	

Count down timer register, address: 5EH-5FH

Timer control register, address: 5EH

BIT	Signal	Descriptions
7-3	—	Invalidation
2	TE	TE=0: timer inactive and stop; TE=1: timer active
1	TD1	TD1,TD0 select timer count frequency: {TD1, TD0}=1 1 :1/60Hz {TD1, TD0}=1 0 :1Hz {TD1, TD0}=0 1 : 64Hz {TD1, TD0}=0 0 : 4096Hz
0	TD0	

Timer/counter register, address: 5FH

BIT	Signal	Descriptions
7~0	Timer count down register	When count to preset value , restart count from 0.

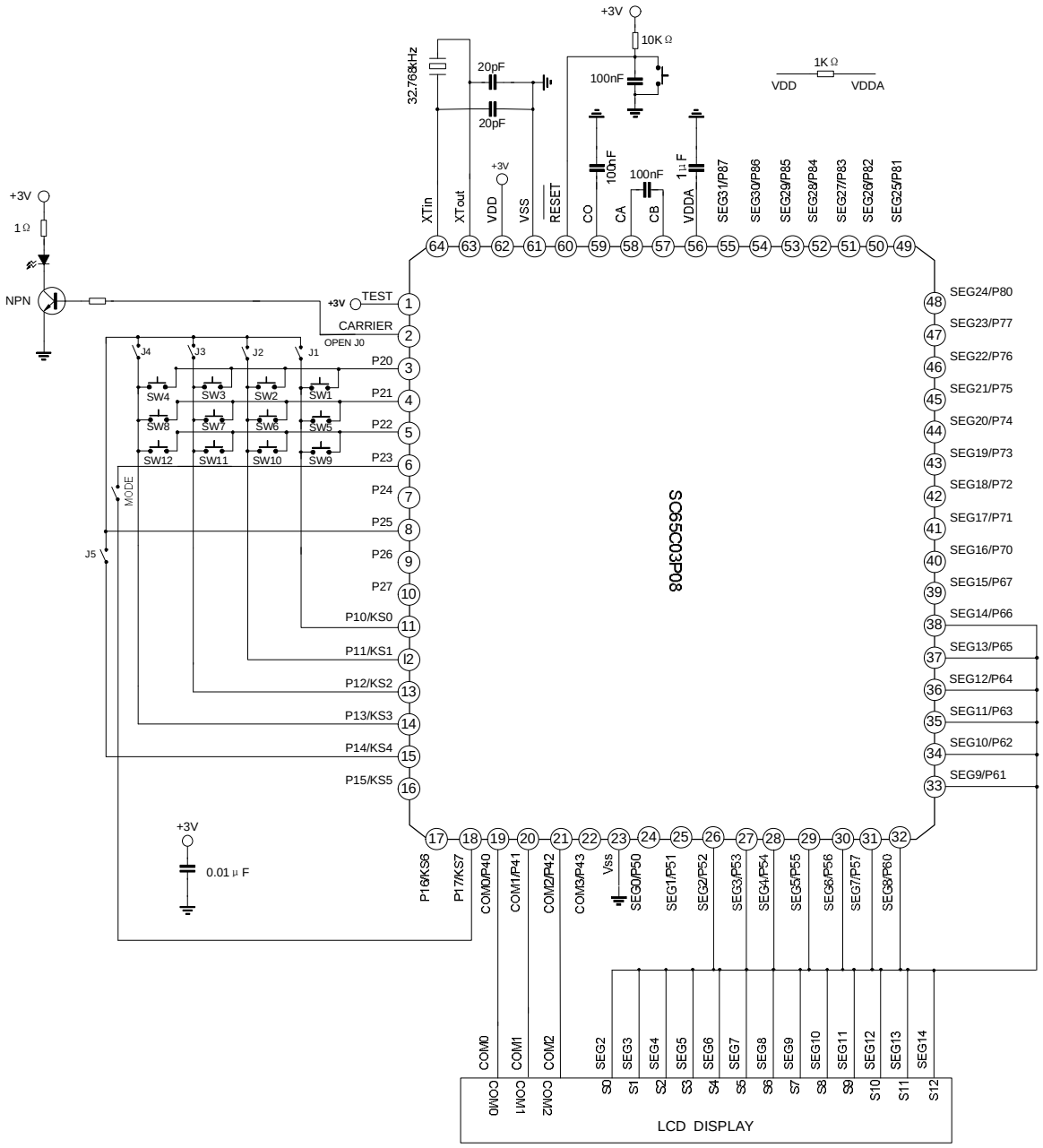
8. power-on reset and power drop detect reset

Reset can be automatically performed at power on by the built-in power-on reset circuit. The power-on reset time is about 10ms.

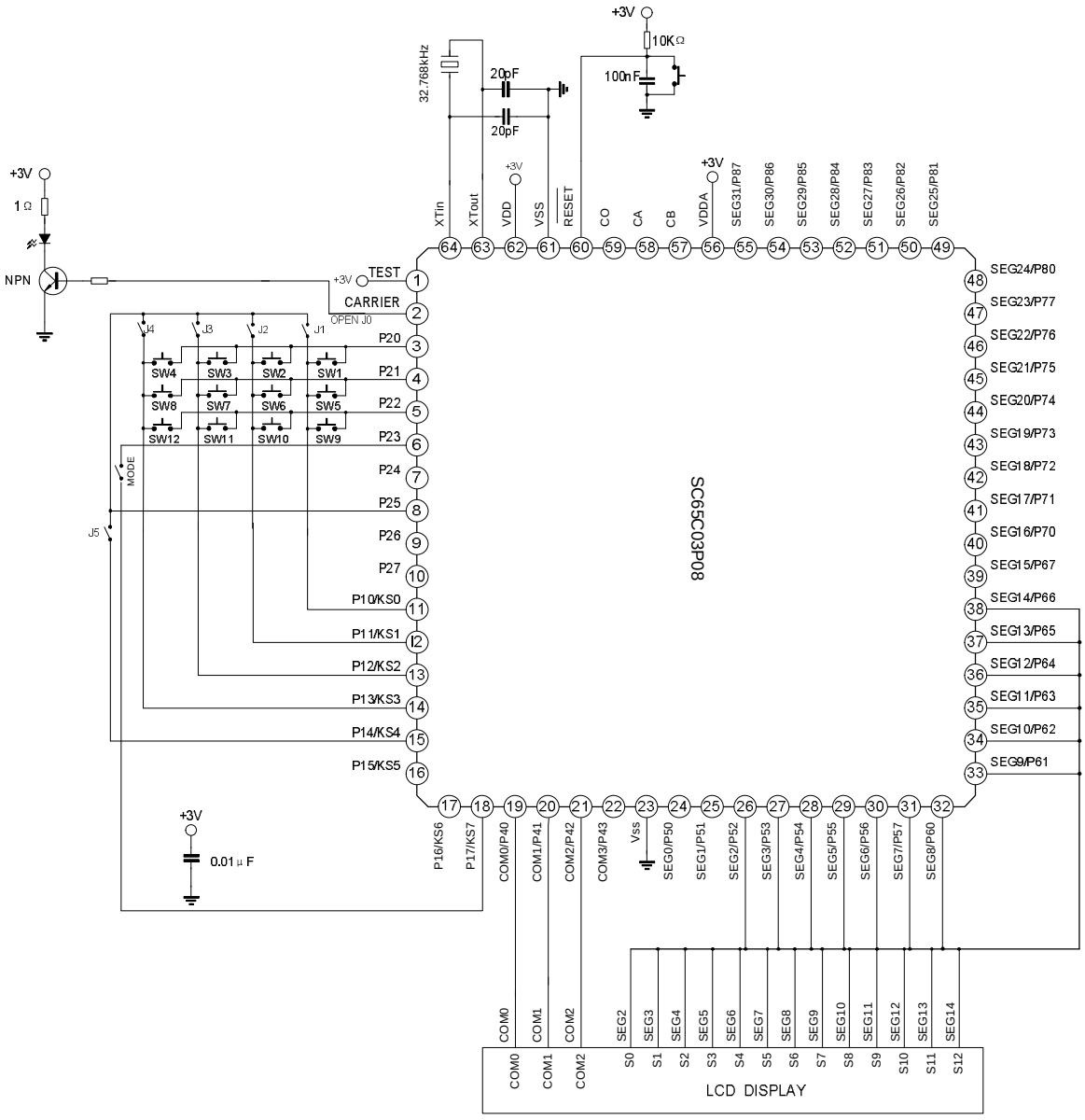
The built-in voltage drop detection circuit is designed to detect a drop in voltage and to reset the chip if the supply voltage drops below a set value(1.9V). The voltage rise to a set value(2.0V), the chip can work normally.

TYPICAL APPLICATION CIRCUIT

1. CHARGE PUMP USED

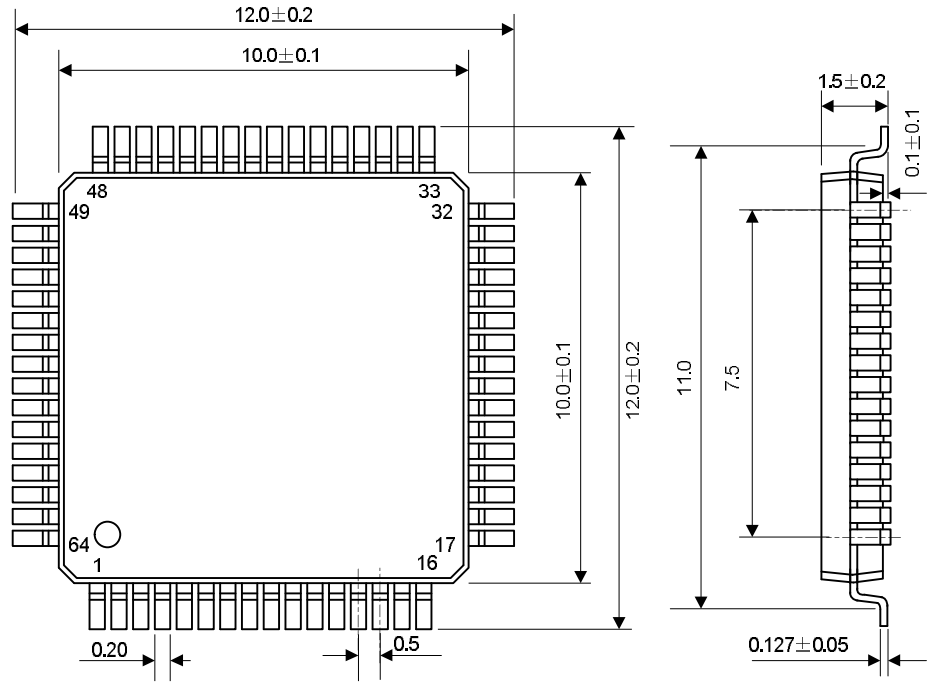


2. CHARGE PUMP NOT USED

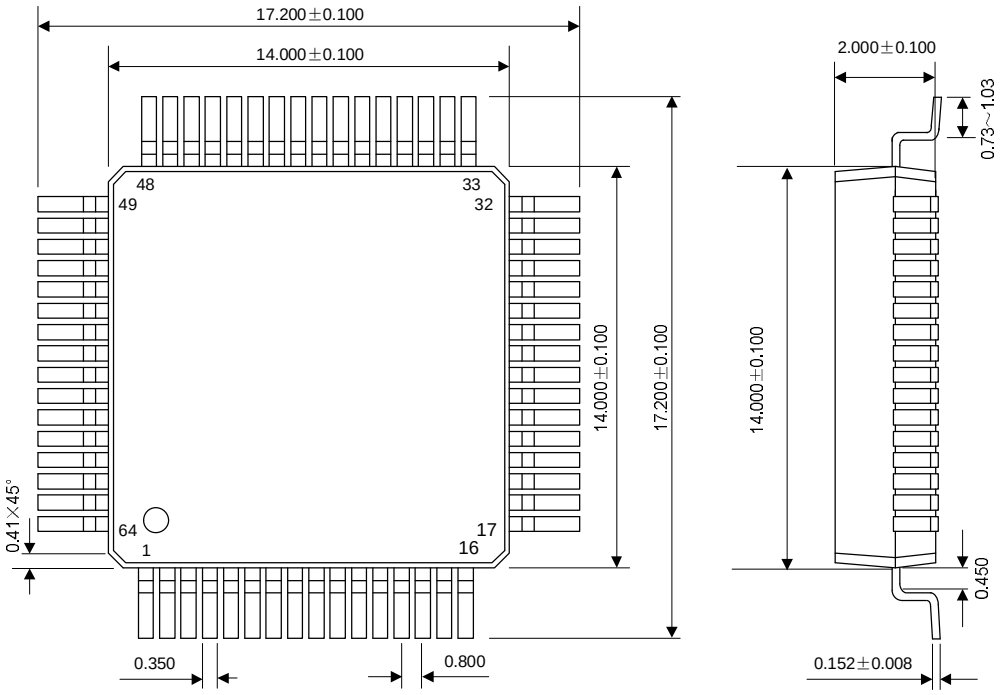


PACKAGE OUTLINE

LQFP-64-10x10-0.5 Unit：mm

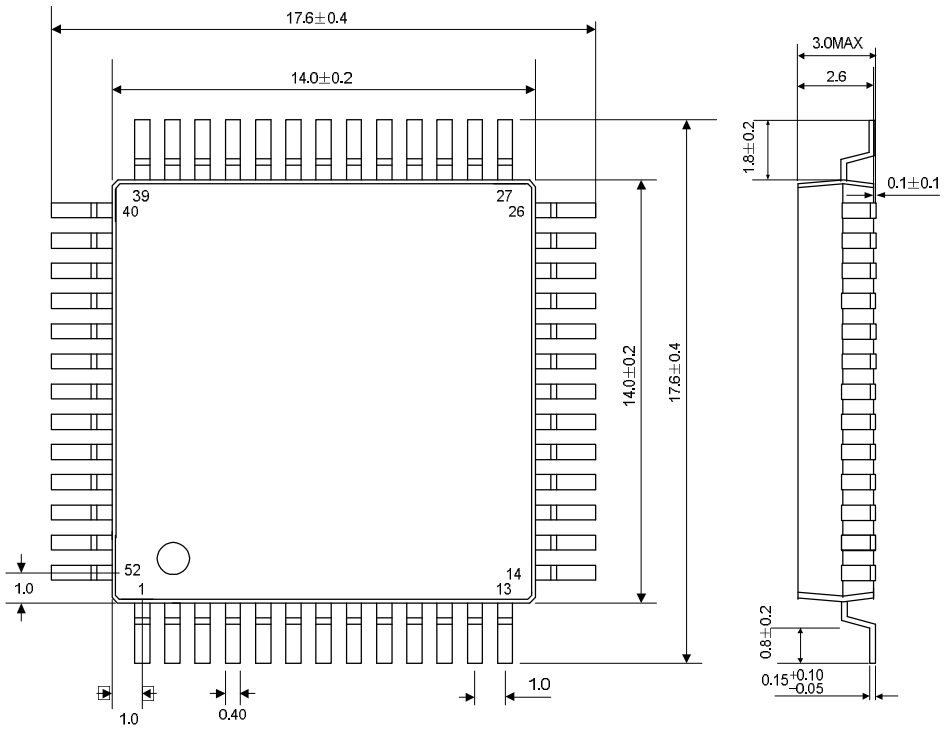


QFP-64-14x14-0.8 Unit：mm

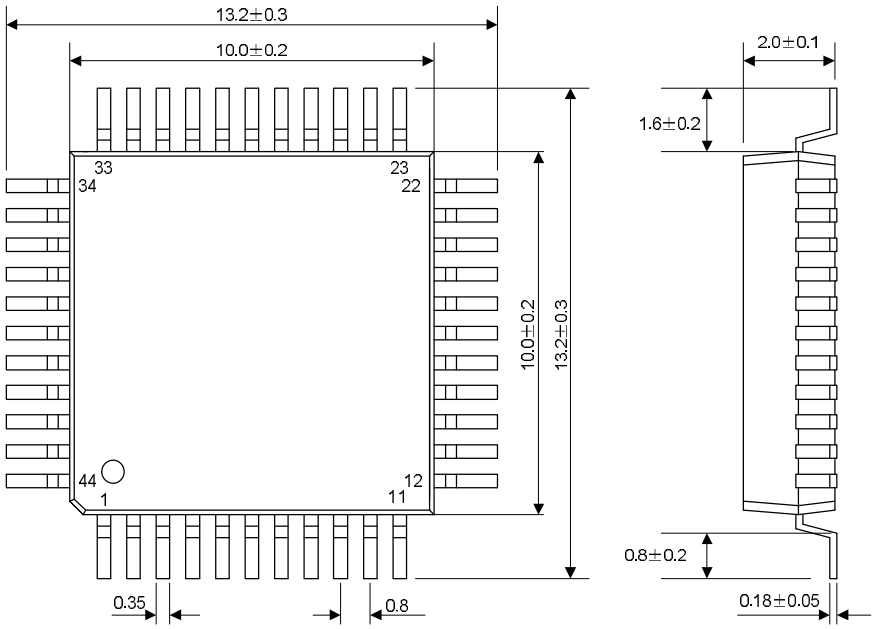


PACKAGE OUTLINE

QFP-52-14x14-1.0 Unit:mm



QFP-44-10x10-0.8 Unit:mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

Note: Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers.

ATTACH

Revision History

Data	REV	Description	Page
2006.12.29	1.0	Original	
2007.03.15	1.1	Add the package of “QFP44-10×10-0.8” and “QFP52-14×14-1.0”	
2007.06.04	1.2	SC65PB0108 change to SC65C03P08	
2007.11.15	1.3	Modify “FUNCTION DESCRIPTION”	