October 1990
Edition 2.0

FUJITSU

DATA SHEET

MB98A9060-25/9070-25/9080-25/9090-25
SRAM Memory Card

Static Random Access Memory Card
64K/128K/256K/512K-Byte

The Fujitsu MB98A9060, MB98A9070, MB98A9080, and MB98A9090 are Static Random Access Memory (SRAM) cards capable of storing and retrieving large amounts of data. Each SRAM card contains a replaceable lithium battery and an on-board rechargeable battery for data retention. The battery can easily be replaced without loss of data because the on-board cell keeps power applied to the memory circuits at all times

The SRAM memory circuits are housed in a credit-card sized 68-pin package. Internal circuitry is protected by metal plates on the top and bottom of the card to help reduce chip damage from electro-static discharge.

A unique feature of the Fujitsu memory cards allows the user to organize the card into either an 8-bit or a 16-bit organization. All cards are portable and operate at high speed with low power needs.

- Card Dimensions: 85.6 length x 43.0 width x 3.3 thickness (mm)
- Connector Type: Two-piece 68-pin (Built-in 68-pin receptacle, 2-row type)
- Complete static operation: No clock required
- TTL compatible inputs/outputs
- Three-state outputs
- Single + 5.0 V ±5% power supply
- Built-in battery backup IC
- Battery alarm function
- Replaceable battery

CRD-68P-M04

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AVAILABLE ORGANIZATIONS

Part Number	Mounted Memory Device	Access Time	Memory Organization*
MB98A9060-25	256K SRAM x 2 pcs.	250 ns	64K x 8 bits/32K x 16 bits
MB98A9070-25	256K SRAM x 4 pcs.	250 ns	128K x 8 bits/64K x 16 bits
MB98A9080-25	256K SRAM x 8 pcs.	250 ns	256K x 8 bits/128K x 16 bits
MB98A9090-25	256K SRAM x 16 pcs.	250 ns	512K x 8 bits/256K x 16 bits

*Configuration to be done by user.

ABSOLUTE MAXIMUM RATINGS (see Note)

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	V
Input Voltage	V_{IN}	−0.5 to V_{CC} +0.5	V
Output Voltage	$V_{I/O}$	−0.5 to V_{CC} +0.5	V
Temperature under Bias	T_{BIAS}	−10 to +60*	°C
Storage Temperature	T_{STG}	−10 to +60*	°C
Ambient Humidity	HA	37.5 to 62.5	RH

*0°C to +40°C when the card is operated or kept for more than 20 consecutive days.

Note: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

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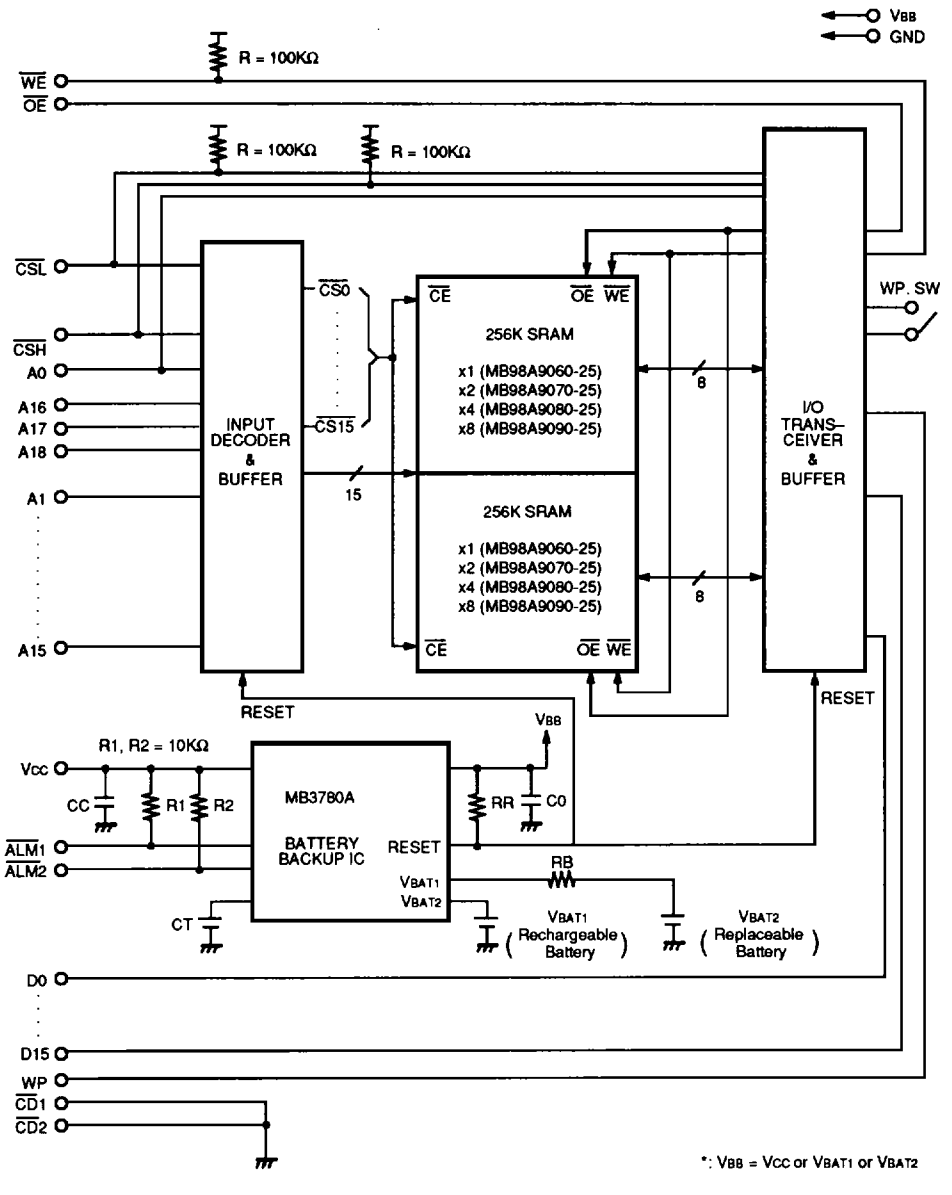
Fig. 1 — MB98A9060/9070/9080/9090 BLOCK DIAGRAM



PIN ASSIGNMENTS

MB98A9060	MB98A9070	MB98A9080	MB98A9090	Pin No.		MB98A9060	MB98A9070	MB98A9080	MB98A9090
GND	GND	GND	GND	1	35	GND	GND	GND	GND
D3	D3	D3	D3	2	36	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$	$\overline{CD1}$
D4	D4	D4	D4	3	37	D11	D11	D11	D11
D5	D5	D5	D5	4	38	D12	D12	D12	D12
D6	D6	D6	D6	5	39	D13	D13	D13	D13
D7	D7	D7	D7	6	40	D14	D14	D14	D14
$\overline{CSL}$	$\overline{CSL}$	$\overline{CSL}$	$\overline{CSL}$	7	41	D15	D15	D15	D15
A10	A10	A10	A10	8	42	$\overline{CSH}$	$\overline{CSH}$	$\overline{CSH}$	$\overline{CSH}$
$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	$\overline{OE}$	9	43	NC	NC	NC	NC
A11	A11	A11	A11	10	44	NC	NC	NC	NC
A9	A9	A9	A9	11	45	NC	NC	NC	NC
A8	A8	A8	A8	12	46	A17 *	A17 *	A17	A17
A13	A13	A13	A13	13	47	A18 *	A18 *	A18 *	A18
A14	A14	A14	A14	14	48	NC	NC	NC	NC
$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	$\overline{WE}$	15	49	NC	NC	NC	NC
NC	NC	NC	NC	16	50	NC	NC	NC	NC
Vcc	Vcc	Vcc	Vcc	17	51	Vcc	Vcc	Vcc	Vcc
NC	NC	NC	NC	18	52	NC	NC	NC	NC
A16 *	A16	A16	A16	19	53	NC	NC	NC	NC
A15	A15	A15	A15	20	54	NC	NC	NC	NC
A12	A12	A12	A12	21	55	NC	NC	NC	NC
A7	A7	A7	A7	22	56	NC	NC	NC	NC
A6	A6	A6	A6	23	57	NC	NC	NC	NC
A5	A5	A5	A5	24	58	NC	NC	NC	NC
A4	A4	A4	A4	25	59	NC	NC	NC	NC
A3	A3	A3	A3	26	60	NC	NC	NC	NC
A2	A2	A2	A2	27	61	NC	NC	NC	NC
A1	A1	A1	A1	28	62	$\overline{ALM1}$	$\overline{ALM1}$	$\overline{ALM1}$	$\overline{ALM1}$
A0	A0	A0	A0	29	63	$\overline{ALM2}$	$\overline{ALM2}$	$\overline{ALM2}$	$\overline{ALM2}$
D0	D0	D0	D0	30	64	D8	D8	D8	D8
D1	D1	D1	D1	31	65	D9	D9	D9	D9
D2	D2	D2	D2	32	66	D10	D10	D10	D10
WP	WP	WP	WP	33	67	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$	$\overline{CD2}$
GND	GND	GND	GND	34	68	GND	GND	GND	GND

Note: *A16, A17 and A18 pins marked " * " are non connection.*

PIN DESCRIPTIONS

Symbol	Pin Name	Input/Output	Function
A0 to A18	Address Input	Input	Address Inputs, A0–A18.
D0 to D15	Data Input/Output	Input/Output	Data Inputs/Outputs. This data bus size (8-bit or 16-bit)selected with $\overline{CSL}$ and $\overline{CSH}$.
$\overline{CSL}$	Chip Select for Lower Byte	Input	Active Low. –Lower byte (D0–D7) is selected for read/write function.
$\overline{CSH}$	Chip Select for Upper Byte	Input	Active Low. –Upper byte (D8–D15) is selected for read/write function.
$\overline{OE}$	Output Enable	Input	Active Low. –Output enable for SRAM cards.
$\overline{WE}$	Write Enable	Input	Active Low. –Write enable for SRAM cards.
$\overline{CD1}$, $\overline{CD2}$	Card Detect	Output	These pins detect if the card has been correctly inserted. Both pins are tied to GND internally.
WP	Write Protect	Output	Write controller for SRAM cards. This pin outputs the On/Off status of "WP Switch".
$\overline{ALM1}$	Battery Alarm1	Output	These pins indicate the battery condition of the SRAM cards. a) $\overline{ALM1}$ = $\overline{ALM2}$ = V_{OH} –Battery voltage is a safe level. b) $\overline{ALM1}$ = V_{OL}, $\overline{ALM2}$ = V_{OH} –Battery voltage is lower than 2.65V. Battery should be replaced. c) $\overline{ALM1}$ = $\overline{ALM2}$ = V_{OL} –Battery voltage is lower than 2.37V.
$\overline{ALM2}$	Battery Alarm2	Output	
Vcc	Power Supply	–	Power Supply Voltage. (+5.0V ±5%)
GND	Ground	–	System Ground.
NC	Non Connection	–	

FUNCTION TRUTH TABLE

$\overline{CSH}$	$\overline{CSL}$	A0 (Byte)	$\overline{OE}$	$\overline{WE}$	WP	Mode	Data Input/Output		WP SW.
							D15–D8	D7–D0	
H	H	X	X	X	L	Standby	High–Z		OFF
H	L	L	L	H	L	Read (x8)	High–Z	D_{OUT} (Lower Byte)	OFF
H	L	H	L	H	L	Read (x8)	High–Z	D_{OUT} (Upper Byte)	OFF
H	L	L	X	L	L	Write (x8)	High–Z	D_{IN} (Lower Byte)	OFF
H	L	H	X	L	L	Write (x8)	High–Z	D_{IN} (Upper Byte)	OFF
L	H	X	L	H	L	Read (x8)	D_{OUT} (Upper Byte)	High–Z	OFF
L	H	X	X	L	L	Write (x8)	D_{IN} (Upper Byte)	High–Z	OFF
L	L	X	L	H	L	Read (x16)	D_{OUT}		OFF
L	L	X	X	L	L	Write (x16)	D_{IN}		OFF
X	X	X	H	H	L	Output Disable	High–Z		OFF
H	H	X	X	X	H	Standby	High–Z		ON
H	L	L	L	H	H	Read (x8)	High–Z	D_{OUT} (Lower Byte)	ON
H	L	H	L	H	H	Read (x8)	High–Z	D_{OUT} (Upper Byte)	ON
H	L	L	X	L	H	Output Disable	High–Z		ON
H	L	H	X	L	H	Output Disable	High–Z		ON
L	H	X	L	H	H	Read (x8)	D_{OUT} (Upper Byte)	High–Z	ON
L	H	X	X	L	H	Output Disable	High–Z		ON
L	L	X	L	H	H	Read (x16)	D_{OUT}		ON
L	L	X	X	L	H	Output Disable	High–Z		ON
X	X	X	H	H	H	Output Disable	High–Z		ON

Definition: H = V_{IH}, L = V_{IL}, X = Either V_{IL} or V_{IH}

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ADDRESS CONFIGURATIONS USING 8-BIT BUS ($\overline{CSH}$ = H, $\overline{CSL}$ = L)

A18 to A0	$\overline{CSH}$	$\overline{CSL}$	D15–D8	D7–D0
000 0000 0000 0000 0000	H	L	-----	0 Add.
000 0000 0000 0000 0001	H	L	-----	1 Add.
000 0000 0000 0000 0010	H	L	-----	2 Add.
000 0000 0000 0000 0011	H	L	-----	3 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 1100	H	L	-----	524284 Add.
111 1111 1111 1111 1101	H	L	-----	524285 Add.
111 1111 1111 1111 1110	H	L	-----	524286 Add.
111 1111 1111 1111 1111	H	L	-----	524287 Add.

ADDRESS CONFIGURATIONS USING 8-BIT BUS ($\overline{CSH}$ = L, $\overline{CSL}$ = H)

A18 to A0	$\overline{CSH}$	$\overline{CSL}$	D15–D8	D7–D0
000 0000 0000 0000 000X	L	H	1 Add.	-----
000 0000 0000 0000 001X	L	H	3 Add.	-----
000 0000 0000 0000 010X	L	H	5 Add.	-----
000 0000 0000 0000 011X	L	H	7 Add.	-----
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 100X	L	H	524281 Add.	-----
111 1111 1111 1111 101X	L	H	524283 Add.	-----
111 1111 1111 1111 110X	L	H	524285 Add.	-----
111 1111 1111 1111 111X	L	H	524287 Add.	-----

Definition: X = Either "0" or "1". Even addresses are not available in this mode.

ADDRESS CONFIGURATIONS USING 16-BIT BUS ($\overline{CSH}$ = L, $\overline{CSL}$ = L)

A18 to A0	$\overline{CSH}$	$\overline{CSL}$	D15–D8	D7–D0
000 0000 0000 0000 000X	L	L	1 Add.	0 Add.
000 0000 0000 0000 001X	L	L	3 Add.	2 Add.
000 0000 0000 0000 010X	L	L	5 Add.	4 Add.
000 0000 0000 0000 011X	L	L	7 Add.	6 Add.
↓ ↓ ↓ ↓ ↓	↓	↓	↓ ↓	↓ ↓
111 1111 1111 1111 100X	L	L	524281 Add.	524280 Add.
111 1111 1111 1111 101X	L	L	524283 Add.	524282 Add.
111 1111 1111 1111 110X	L	L	524285 Add.	524284 Add.
111 1111 1111 1111 111X	L	L	524287 Add.	524286 Add.

Definition: X = Either "0" or "1".

RECOMMENDED OPERATING CONDITIONS

(Referenced to GND)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Ground	GND		0		V
Input High Voltage	V_{IH}	2.4		$V_{CC+0.3}$	V
Input Low Voltage	V_{IL}	−0.3		0.8	V
Ambient Temperature*	TA	0		50	°C
Ambient Humidity	HA	37.5	50.0	62.5	RH

*: 0°C to +40°C when the card is operated or kept for more than 20 consecutive days.

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DC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

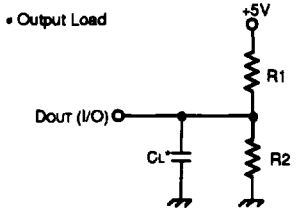
Parameter	Test Condition	Symbol	Min	Max	Unit
Standby Supply Current	$\overline{CSL}$ = $\overline{CSH}$ ≥ V_{CC} −0.2V	I_{SB1}		8.0	mA
	$\overline{CSL}$ = $\overline{CSH}$ = V_{IH}	I_{SB2}		15.0	mA
Active Supply Current	V_{IN} = V_{IH} or V_{IL} $\overline{CSL}$ = $\overline{CSH}$ = V_{IL}, I_{OUT} = 0mA	I_{CC1}		100	mA
Operating Supply Current	Cycle = Min. Duty = 100%, I_{OUT} = 0mA	I_{CC2}		120	mA
Input Leakage Current (except $\overline{CSL}$, $\overline{CSH}$, $\overline{WE}$)	V_{IN} = 0V to V_{CC}	I_{LI}	−10	10	µA
Output Leakage Current (except $\overline{ALM1}$, $\overline{ALM2}$, $\overline{CD1}$, $\overline{CD2}$)	$V_{I/O}$ = 0V to V_{CC} $\overline{CSL}$ = $\overline{CSH}$ = V_{IH} $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	$I_{LI/O}$	−10	10	µA
Output High Voltage (except $\overline{ALM1}$, $\overline{ALM2}$)	I_{OH} = −1.0mA	V_{OH}	2.4		V
Output Low Voltage (except $\overline{CD1}$, $\overline{CD2}$)	I_{OL} = 2.1mA	V_{OL}		0.4	V

Note: All voltages are referenced to GND.

CAPACITANCE (T_A=25°C, f=1MHz, V_{IN}=$V_{I/O}$=GND)

Parameter	Symbol	Min	Typ	Max	Unit
Input Capacitance (except $\overline{CSL}$, $\overline{CSH}$, $\overline{WE}$)	C_{IN}			50	pF
I/O Capacitance (except $\overline{ALM1}$, $\overline{ALM2}$, $\overline{CD1}$, $\overline{CD2}$)	C_{OUT}			50	pF

Fig. 2 – AC TEST CONDITIONS



- Input Pulse Levels: 0.6V to 2.6V
- Input Pulse Rise and Fall Times: 5ns (Transient between 0.8V and 2.4V)
- Timing Reference Levels
  Input: V_{IL} = 0.8V, V_{IH} = 2.4V
  Output: V_{OL} = 0.8V, V_{OH} = 2.0V

* Including Jig and stray capacitance

	R1	R2	CL	Parameters Measured
Load I	1.8kΩ	990Ω	100pF	except t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}
Load II	1.8kΩ	990Ω	5pF	t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{WLZ} and t_{WHZ}

AC CHARACTERISTICS

(Recommended operating conditions unless otherwise noted.)

READ CYCLE *1

Parameter	Symbol	Min	Max	Unit
Read Cycle Time	t_{RC}	250		ns
Address Access Time	t_{AA}		250	ns
Chip Select Access Time	t_{ACS}		250	ns
Output Enable Access Time	t_{OE}		120	ns
Output Hold from Address Change	t_{OH}	5		ns
Chip Select to Output Low-Z *2*3	t_{CLZ}	5		ns
Output Enable to Output Low-Z *2*3	t_{OLZ}	5		ns
Chip Select to Output High-Z *2*3	t_{CHZ}		60	ns
Output Enable to Output High-Z *2*3	t_{OHZ}		60	ns

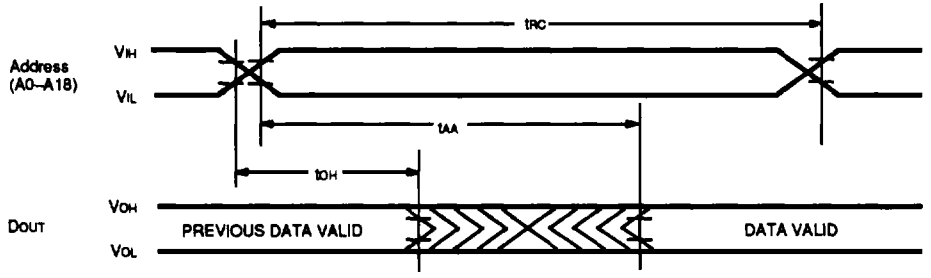
Note: *1 $\overline{WE}$ is high for Read cycle.
*2 Transition is measured at the point of ±500mV from steady state voltage.
*3 This parameter is specified using Load II in Fig. 2.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

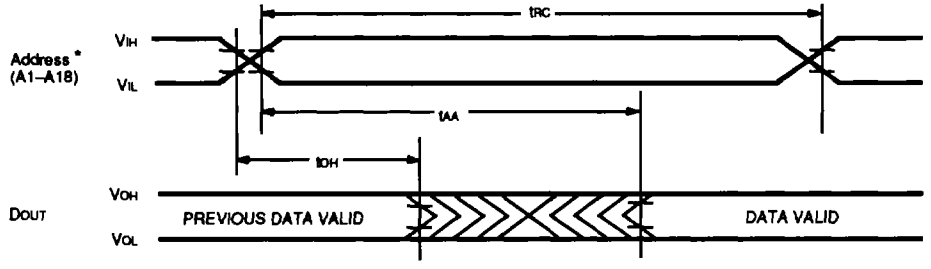
READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = V_{IH})

READ CYCLE 1: $\overline{CSH}$ = V_{IH}, $\overline{CSL}$ = $\overline{OE}$ = V_{IL}: x 8-bit Bus Organization



READ CYCLE 2: $\overline{CSL}$ = V_{IH}, $\overline{CSH}$ = $\overline{OE}$ = V_{IL}: x 8-bit Bus Organization

$\overline{CSL}$ = $\overline{CSH}$ = $\overline{OE}$ = V_{IL}: x 16-bit Bus Organization



:Undefined

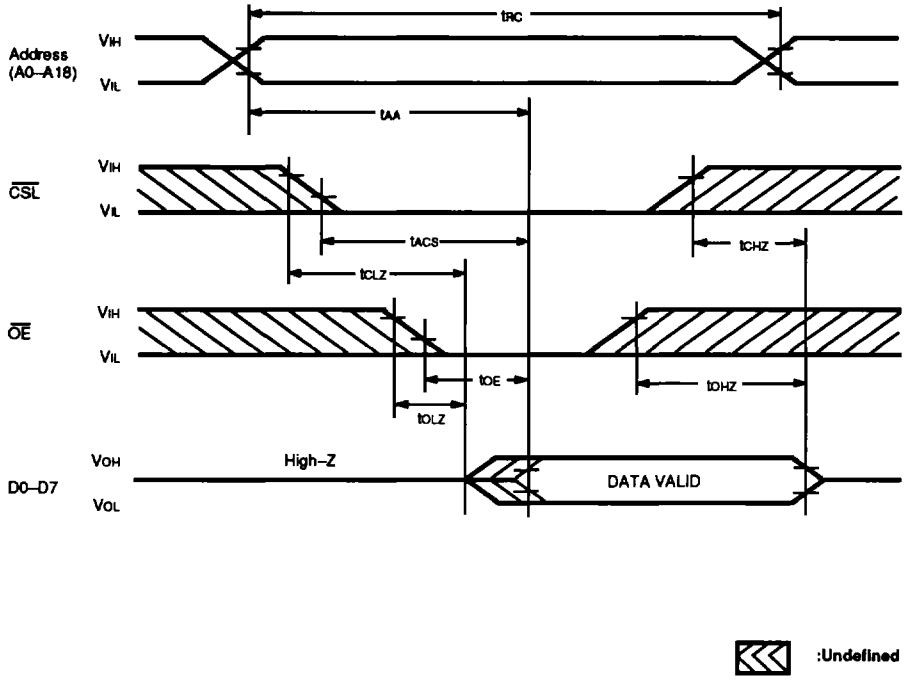
*A0 = Either V_{IH} or V_{IL}.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH)

READ CYCLE 3: $\overline{CSH}$ = VH: x 8-bit Bus Organization

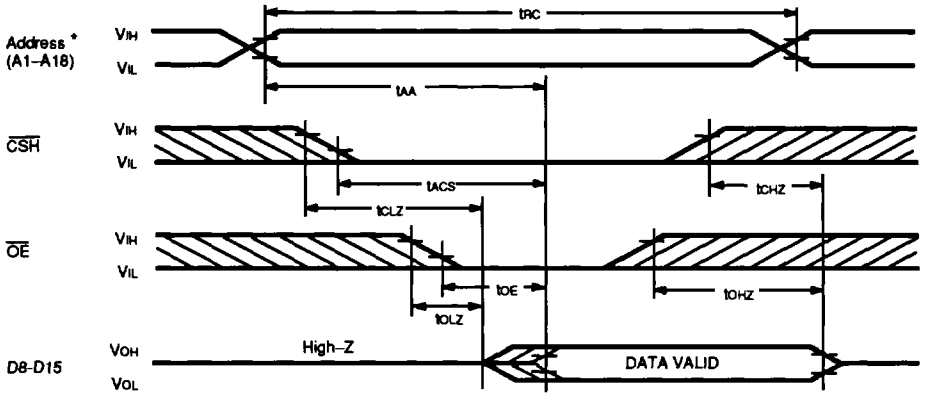


AC CHARACTERISTICS (Continued)

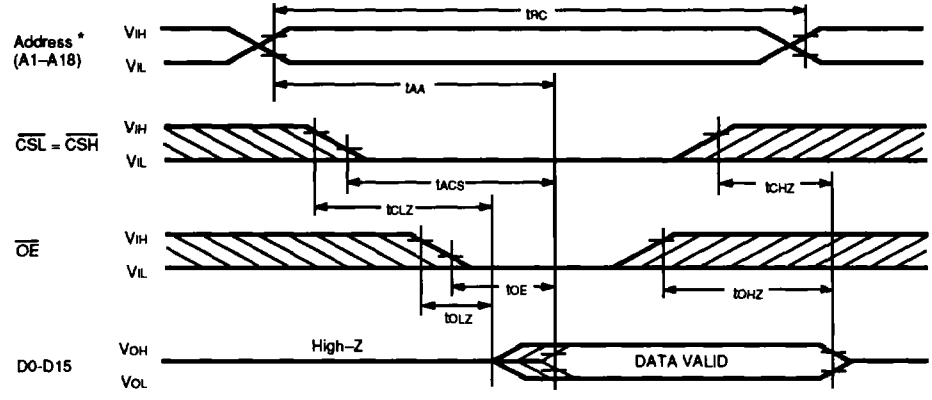
(Recommended operating conditions unless otherwise noted.)

READ CYCLE TIMING DIAGRAM ($\overline{WE}$ = VIH)

READ CYCLE 4: $\overline{CSL}$ = VIH: x 8-bit Bus Organization



READ CYCLE 5: $\overline{CSL}$ = $\overline{CSH}$ = VIL: x 16-bit Bus Organization



Note: * A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE *1

Parameter	Symbol	Min	Max	Unit
Write Cycle Time	t_{WC}	250		ns
Address Valid to End of Write	t_{AW}	180		ns
Chip Select to End of Write	t_{CW}	180		ns
Data Valid to End of Write	t_{DW}	80		ns
Data Hold Time	t_{DH}	30		ns
Write Pulse Width	t_{WP}	150		ns
Address Setup Time	t_{AS}	30		ns
Write Recovery Time	t_{WR}	30		ns
Output High-Z from Write Enable *2*3	t_{WHZ}	5		ns
Output Low-Z from Write Enable *2*3	t_{WLZ}		60	ns

Note: *1 If $\overline{OE}$, $\overline{CSL}$ and $\overline{CSH}$ in the READ Mode during this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must be applied.

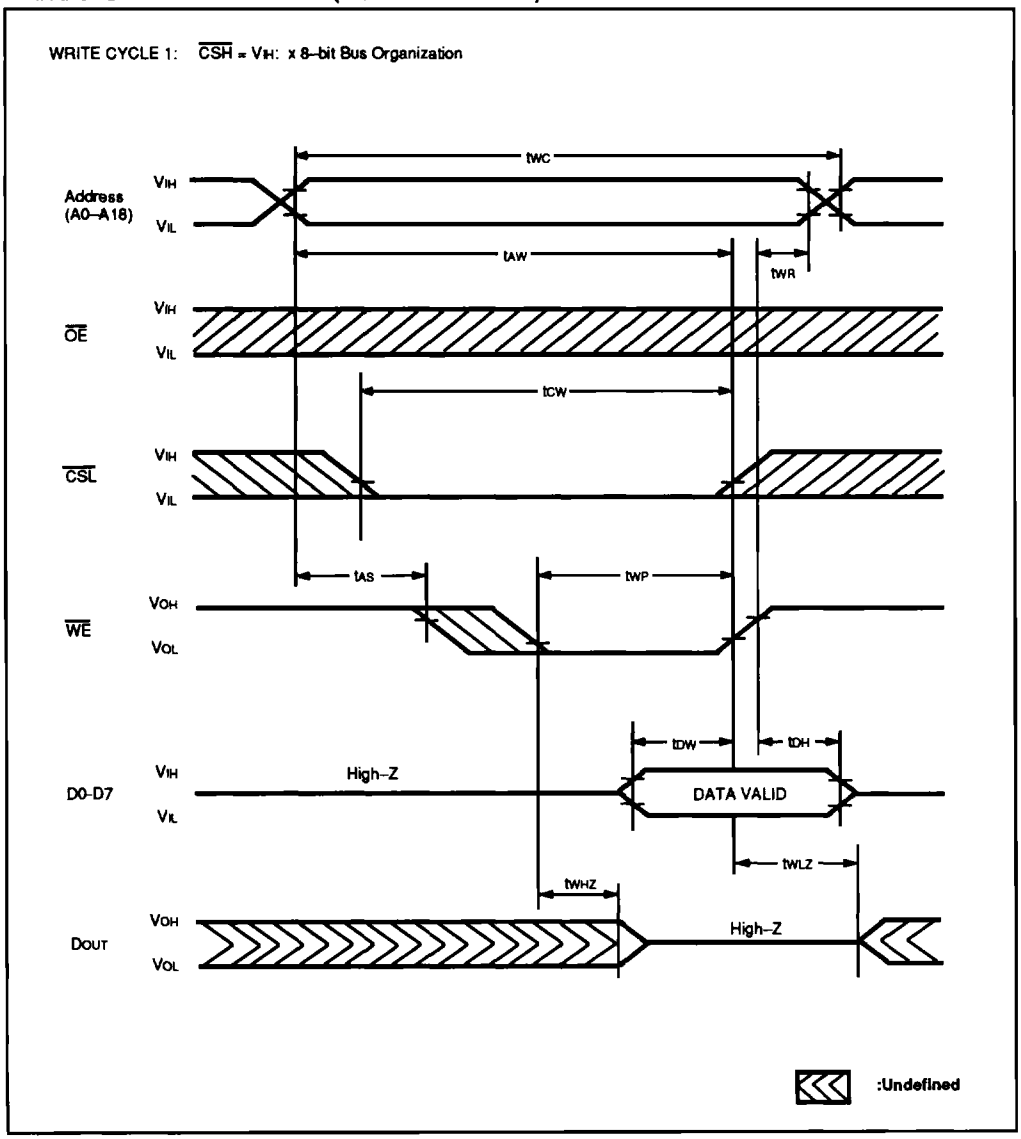
*2 Transition is measured at the point of ±500mV from steady state voltage.

*3 This parameter is specified using Load Π in Fig. 2.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

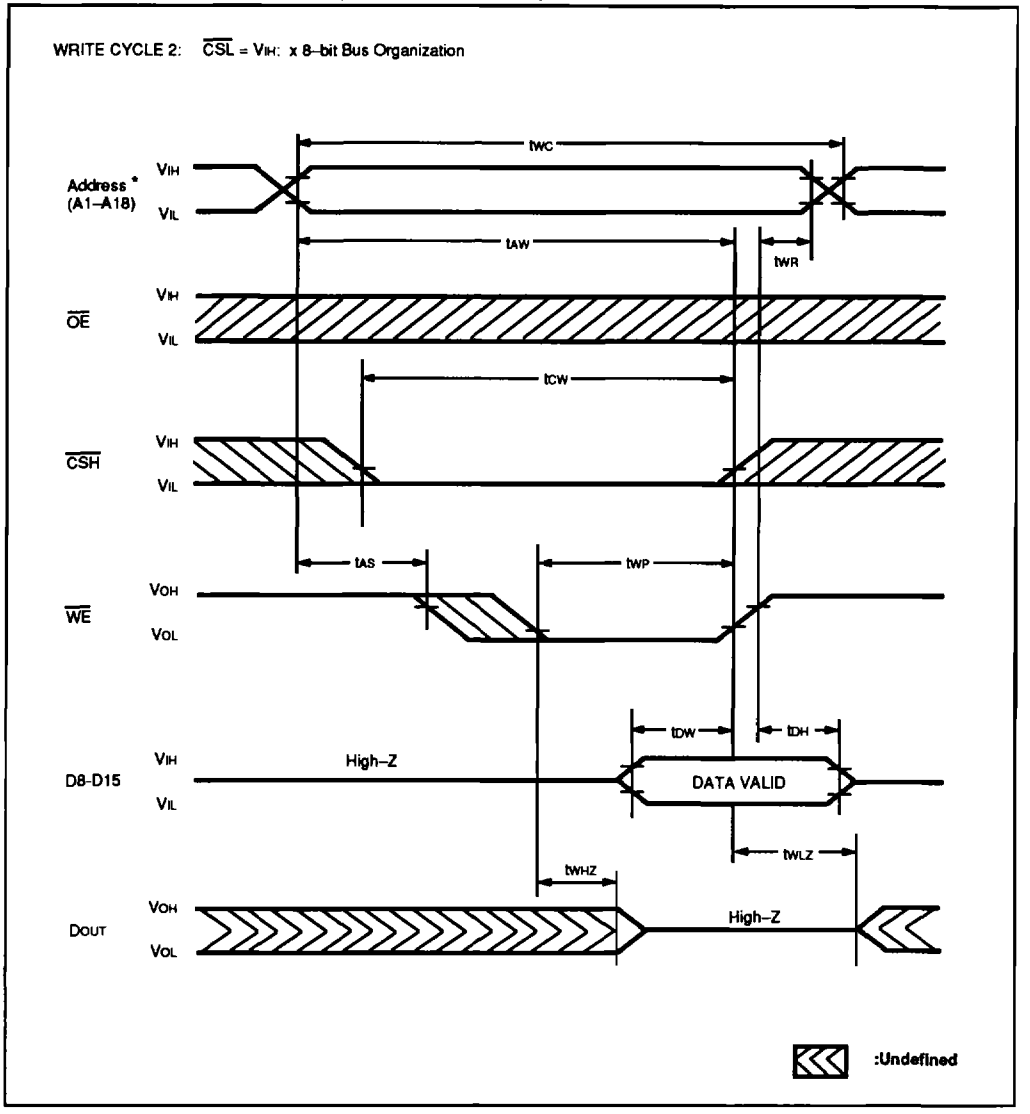
WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED)



AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED)



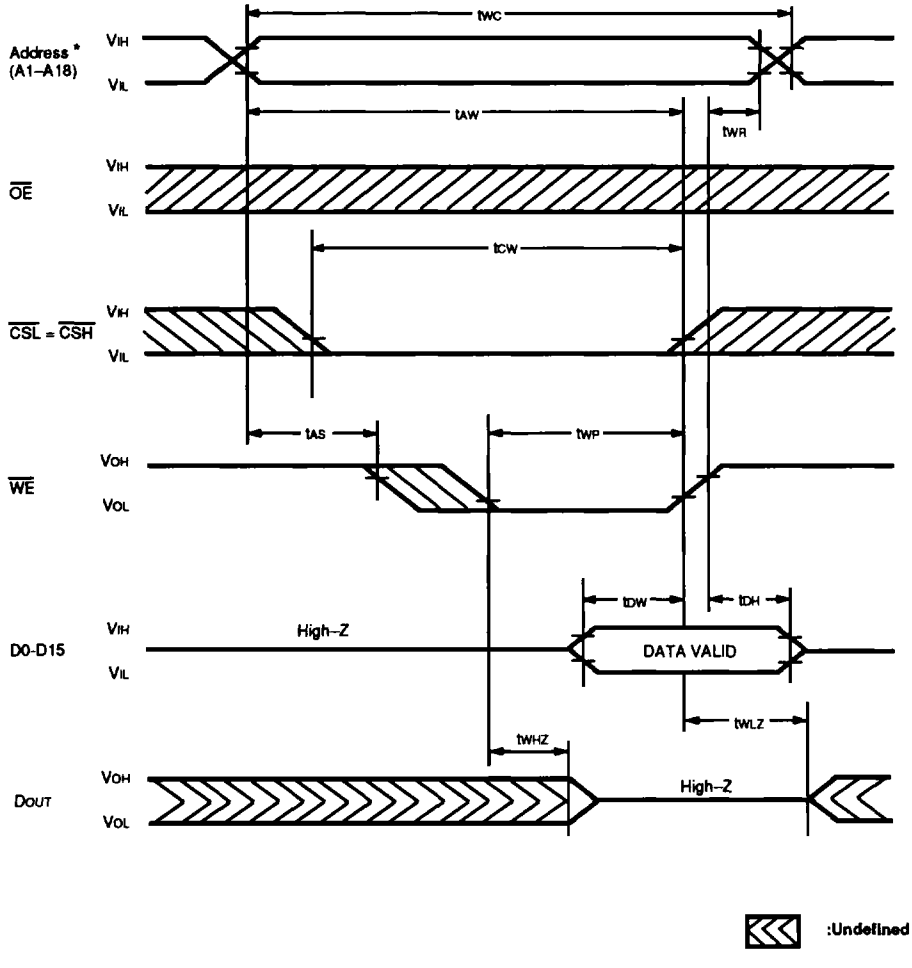
Note: *A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM ($\overline{WE}$ = CONTROLLED)

WRITE CYCLE 3: $\overline{CSL}$ = $\overline{CSH}$ = V_{IL}: x 16-bit Bus Organization

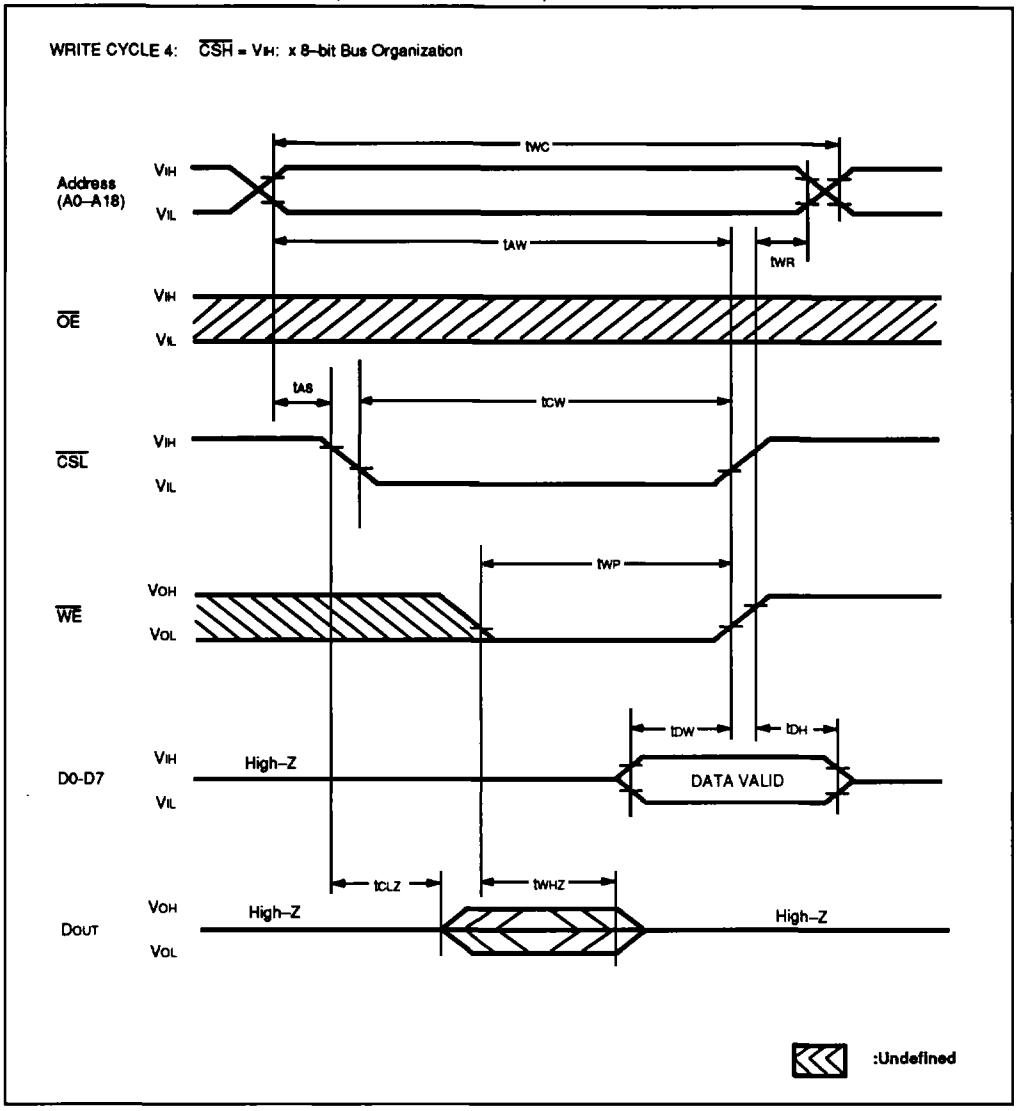


Note: *A0 = Either V_{IL} or V_{IH}.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

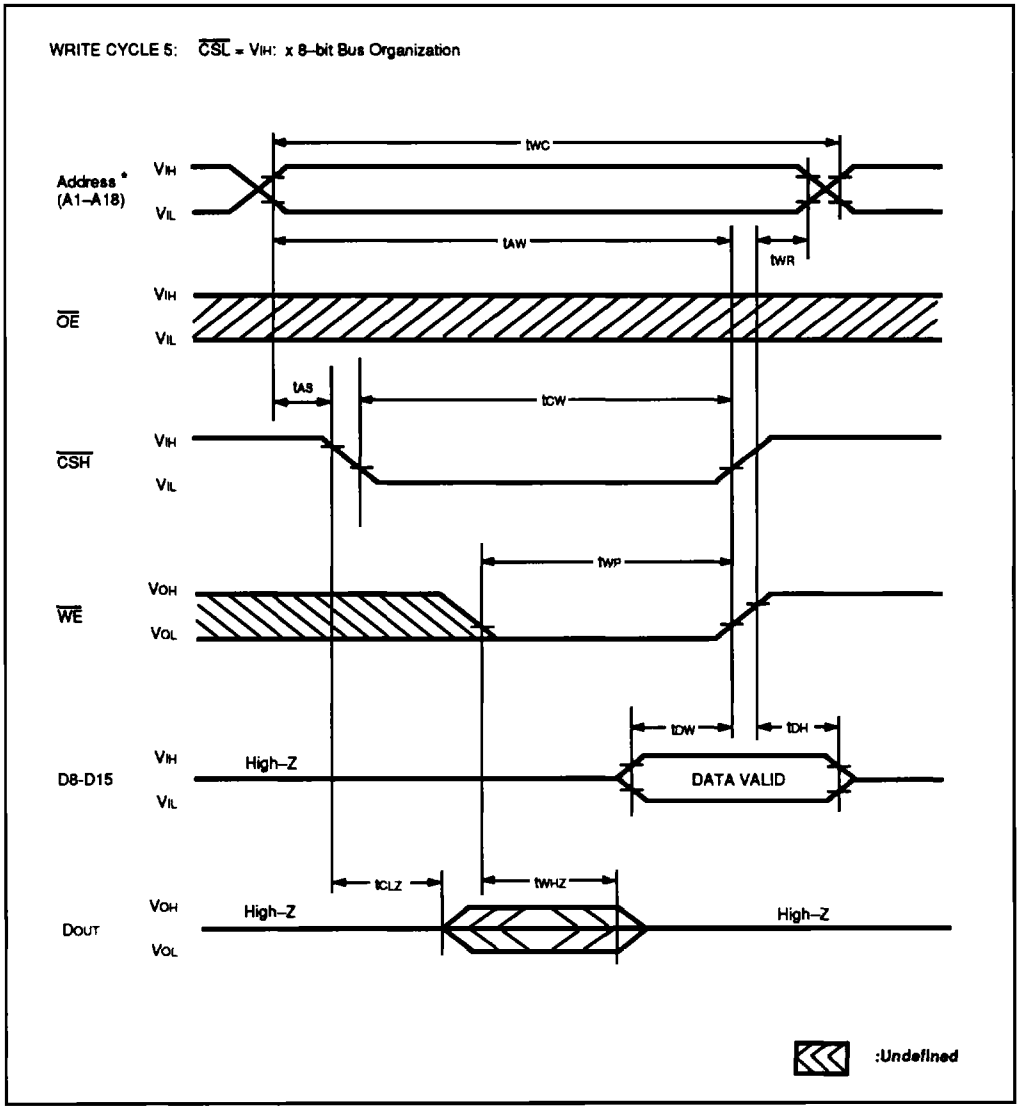
WRITE CYCLE TIMING DIAGRAM ($\overline{CSL}$ = CONTROLLED)



AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM ($\overline{CSH}$ = CONTROLLED)

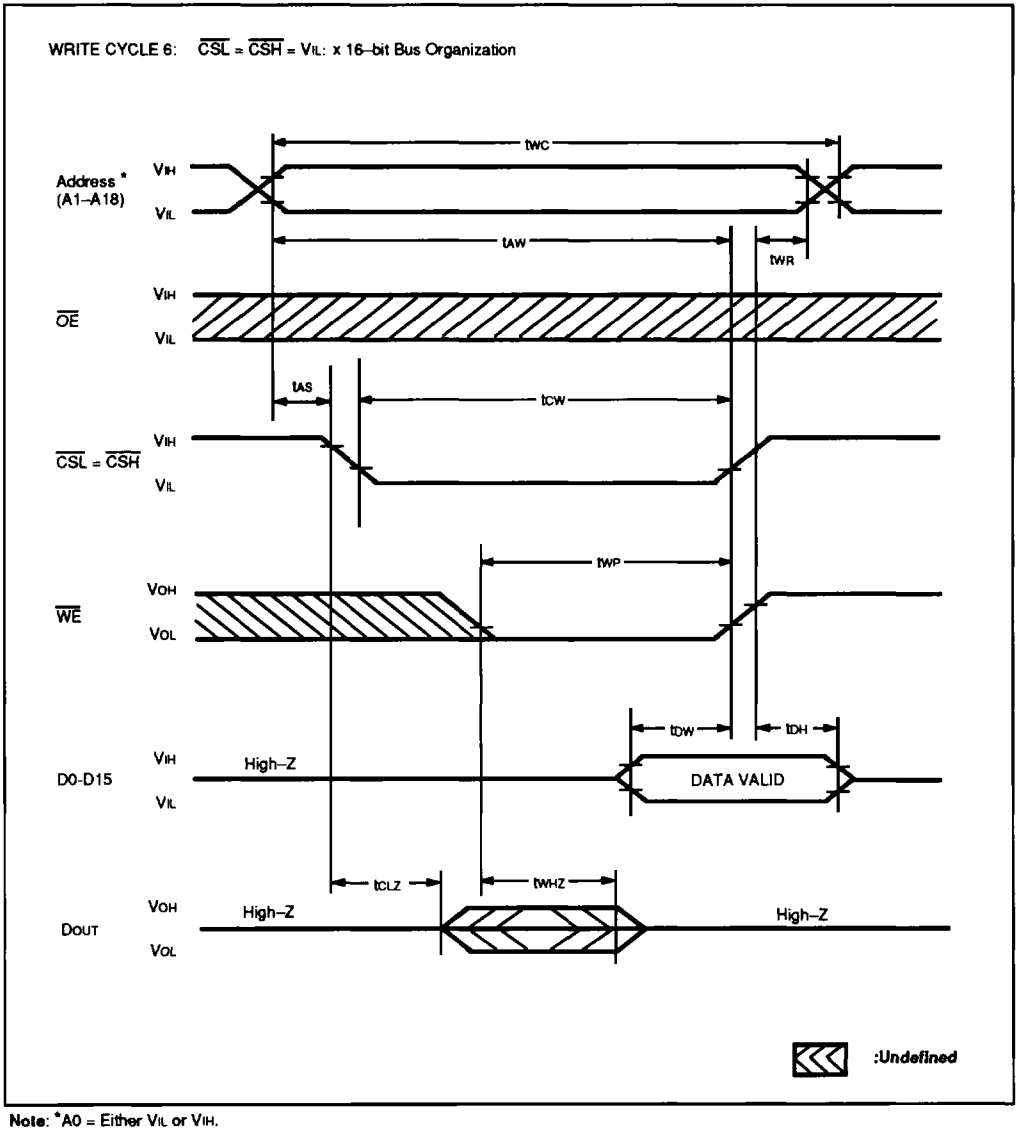


Note: *A0 = Either VIL or VIH.

AC CHARACTERISTICS (Continued)

(Recommended operating conditions unless otherwise noted.)

WRITE CYCLE TIMING DIAGRAM ($\overline{CSL}$, $\overline{CSH}$ = CONTROLLED)

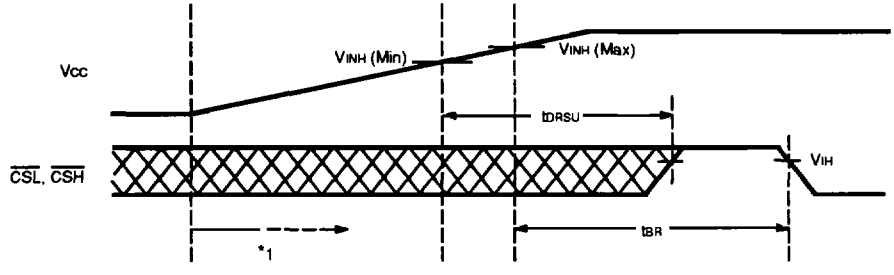


Note: *A0 = Either VIL or VIH.

POWER SUPPLY SEQUENCE CHARACTERISTICS

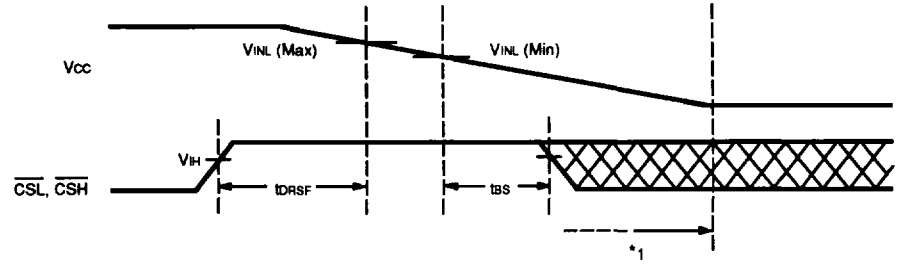
Parameter	Symbol	Min	Typ	Max	Unit
Detection Rising Voltage	V_{INH}	4.2	4.3	4.4	V
Detection Falling Voltage	V_{INL}	4.1	4.2	4.3	V
Battery Backup Recovery Time	t_{BR}	3.0			ms
Data Retention Rising Time	t_{DRSU}			0.5	ms
Battery Backup Setup Time	t_{BS}	10			µs
Data Retention Falling Time	t_{DRSF}	0			ns

POWER -ON TIMING DIAGRAM



Note: *1 Insertion/ Removal of the card should be prohibited.

POWER -OFF TIMING DIAGRAM



Note: *1 Insertion/ Removal of the card should be prohibited.

UNIQUE FEATURES FOR SRAM CARD

1. REPLACEABLE BATTERIES FOR SRAM MEMORY CARD

The battery used in the SRAM Memory Card is a 3V Lithium battery (coin type) with the following specifications:

Diameter : 23.0 (mm)
Thickness : 2.5 (mm)
Weight : 3.2 (g) Approx.

Some manufacturers of this type of battery include:

Vendor	Part Number
FDK	CR2325
Panasonic (National)	BR2325
Ray-O-Vac	BR2325

2. APPROXIMATE DATA RETENTION TIME WITH BATTERY SUPPORT ONLY

Part Number	Approx. Data Retention Time * (T_A=20°C)
MB98A9060-25	4 years min.
MB98A9070-25	2 years min.
MB98A9080-25	1 year min.
MB98A9090-25	6 months min.

* Determined by the memory density of the card;
i.e., greater card density means less battery time.

3. REPLACING THE BATTERY IN THE SRAM MEMORY CARD

a. Insert a slender pointed object, such as the end of a paper clip, into the hole on the upper side of the card. (See Fig. 3.)

b. Release the battery holder by pressing the paper clip against the catch and pulling the battery holder straight out from the card. (The battery cavity is located at the top of the card. See Fig. 4.) When the battery holder is free from the card the battery will fall out.

c. Replace the old battery with a fresh one. Be certain to match battery polarity to the + and – shown on the holder.

d. Place the new battery into the holder, squeeze the holder containing the new battery tightly, and reinsert it into the battery cavity.

WARNING
Battery MUST be replaced within 30 minutes or data will be lost.

Fig. 3 – SRAM CARD DRAWING (TOP VIEW)

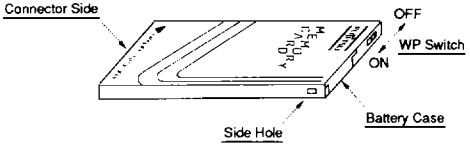
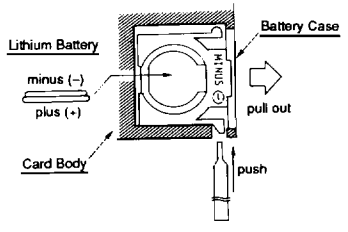


Fig.4 – BATTERY CASE DRAWING (TOP VIEW)



UNIQUE FEATURES FOR SRAM CARD (Continue)

4. SPECIAL MONITORING PINS

4.1 $\overline{ALM}1$, $\overline{ALM}2$: Voltage Monitoring Pins

These pins monitor the voltage of the battery which must be maintained at 2.65V or greater for data retention. The condition of the battery is determined by reading the output signals on $\overline{ALM}1$ and $\overline{ALM}2$.

1. When $\overline{ALM1}=\overline{ALM2}=V_{OH}$
Battery voltage is sufficient to guarantee data retention; i.e., ≥2.65V.

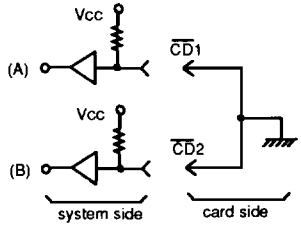
2. When $\overline{ALM1}=V_{OL}$, $\overline{ALM2}=V_{OH}$
Battery voltage is lower than 2.65V and should be replaced to safeguard data.

3. When $\overline{ALM1}=\overline{ALM2}=V_{OL}$
Battery voltage is less than 2.37V: the level is dangerous. The battery must be replaced immediately to retain the data.

* If the battery is removed, $\overline{ALM}1$, $\overline{ALM}2$ will not function.

4.2 $\overline{CD}1$, $\overline{CD}2$: Card Detection Pins

These pins detect the insertion of the card into the system. (See Fig. 5.)
When the memory card has been correctly inserted, $\overline{CD}1$ and $\overline{CD}2$ are detected by the system. $\overline{CD}1$, $\overline{CD}2$ are tied to ground on the card side as shown in Fig. 5.



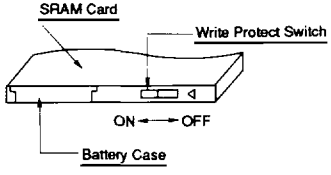
– Fig. 5 –

4.3 WP: Write Protect Pins

This pin monitors the position of the Write Protect switch. As shown in Fig. 6, the SRAM card has a Write Protect switch at the top of the card.

To write to the card, the switch must be turned to the OFF position and the $\overline{WE}$ pin low. L–level is output on the WP pin.

To prevent writing to the card, the switch must be turned to the ON position. H–level is output on the WP pin.

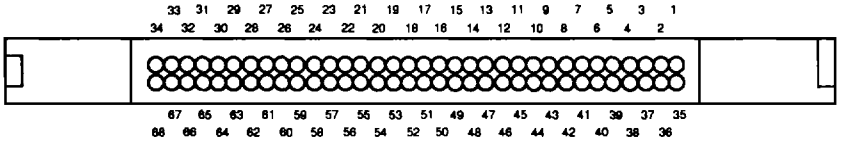


– Fig. 6 –

WP Switch	WP
ON	H
OFF	L

PIN LOCATIONS

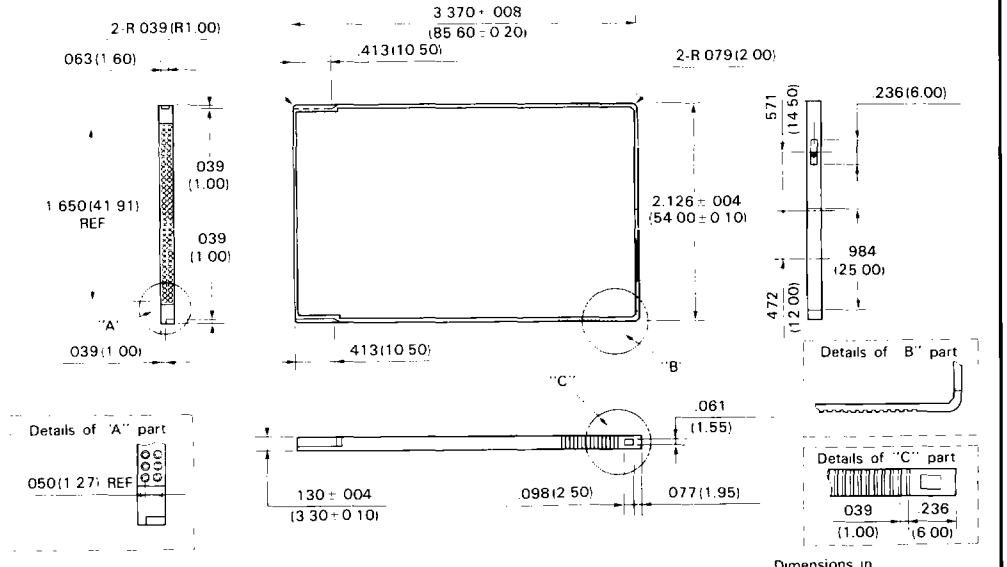
Fig. 7 – BOTTOM VIEW (CONNECTOR SIDE)



1

PACKAGE DIMENSIONS

68-PIN MEMORY CARD
(CASE No.: CRD-68P-M04)



Dimensions in
inches (millimeters)