



## **Functional Overview**

The VSC9112 is a dual mode SONET/SDH framing device. In the Packet over SONET (POS) mode, this device can be used in equipment interconnecting Packet/PPP/HDLC equipment over public or private SONET/SDH networks. Similarly, in the ATM over SONET (ATM) mode, this device can be used in equipment interconnecting ATM switches. When used in conjunction with a high-speed Mux/Demux transceiver, this device provides a complete physical layer solution for Packet/ATM over SONET at the OC-48 rate. In addition, this device provides the interface for further mux/demux applications at the OC-192/STM-64 rate. By using this device, highly integrated and versatile OC-48 single line card solutions can be developed. The basic features of the receive and transmit datapaths and features of other interfaces are listed below.

### **Receive SONET/SDH Section Processor**

- Two mechanisms for frame alignment are provided: A1 and A2 framing pattern search, and external frame pulse. Each mechanism programmable for transitions in/out of the Out of Frame (OOF) state.
- It is possible to force an OOF condition on the incoming data stream.
- Loss of Frame (LOF) declaration is programmable.
- The incoming data stream is descrambled using the generating polynomial  $1 + x^6 + x^7$  with a sequence length of 127. The A1, A2, and J0/Z0 bytes are not descrambled. Descrambling can be disabled.
- Section BIP-8 (B1) errors are detected and accumulated. Both individual and block mode accumulation of B1 error indications are supported.
- Two criterias for LOS detection and two criterias for LOS termination are provided and programmable.
- It is possible to force insert all "1"s into the data stream with the exception of the section overhead. The Line AIS (AIS-L) condition can be automatically inserted in case of LOS, LOF, and LOPC events.
- The entire section overhead is extracted to the Receive Overhead Access Port (ROAP).

### **Transmit SONET/SDH Section Processor**

- It is possible to forced insert all "1"s into the data stream, before scrambling, with the exception of the section overhead. The AIS-L condition can be automatically inserted through activity from the special purpose serial interfaces.
- The Section BIP-8 code is computed and can be placed in the B1 byte of the current frame. It is possible to insert B1 errors for diagnostics purposes.
- The A1 and A2 framing bytes can be inserted into the frame. It is also possible to introduce bit errors in the framing word.
- The J0 byte supports both SONET and SDH formats. The J0 byte can be programmed to a fixed value for interworking with older equipment implementing the C1 identification byte.
- The Z0 growth bytes supports both SONET and SDH formats. The Z0 bytes can be programmed to carry the C1 identification bytes for interworking with older equipment.

## **Preliminary Datasheet** **VSC9112**

## *STS-48c Physical Layer* *Packet/ATM Over SONET/SDH Device*

- The outgoing data stream is scrambled using the generating polynomial  $1 + x^6 + x^7$  with a sequence length of 127. The A1, A2, and J0/Z0 bytes are not scrambled. Scrambling can be disabled.
- It is possible to force insert all "0"s in the outgoing data stream after scrambling.
- The data extracted from the special purpose serial interface ports can be inserted into the D1-D3, E1, F1 and J0 bytes.
- All bytes in the section overhead that are reserved for national use can be overwritten with 0x00.
- All bytes in the section overhead that are reserved for future international standardization can be overwritten with 0x00.
- A frame pulse is provided for the outgoing data stream and is programmable.

### **Receive SONET/SDH Line Processor**

- The Line Remote Defect Indication (RDI-L) carried in the K2 byte is detected and programmable.
- The Line Alarm Indication Signal (AIS-L) carried in the K2 byte is detected and programmable.
- Line BIP-384 errors carried in the B2 byte are detected and accumulated. Up to 3072000 errors can be detected per second. Both individual and block mode accumulation of B2 errors are supported.
- Line REI error indications carried in the M1 byte are accumulated. Up to 2040000 error indications can be detected per second. Both individual and block mode accumulation of M1 error indications are supported.
- The Synchronization Status carried in the S1 byte is detected and programmable.
- The K1 and K2 byte is checked and alarmed for persistency. This mechanism is programmable.
- The entire line overhead is extracted to the Receive Overhead Access Port (ROAP).

### **Transmit SONET/SDH Line Processor**

- It is possible to insert programmable sets of K1 and K2 bytes into the outgoing data stream.
- It is possible to force insert RDI-L into the outgoing datastream. The RDI-L can be automatically inserted during the detection of an LOS, LOF, or AIS-L alarm in the incoming data stream, or through activity from the special purpose serial interfaces.
- It is possible to force insert AIS-L into the outgoing data stream.
- The Line BIP-384 code is computed and placed in the B2 bytes of the current frame. It is possible to insert B2 errors for diagnostics purposes.
- The number of Line BIP-384 errors detected in the Receive Line Overhead Processor (RLOP) is backreported as Line REI in the M1 byte. Up to 255 errors can be backreported per frame in individual mode. Both individual and block mode backreporting for M1 are supported. It is possible to insert M1 error indications for diagnostics purposes.
- The Synchronization Status value inserted in the S1 byte is programmable.

- The TLDCC (D4-D12), TLOW (E2), TSYNC (S1) and TAPS (K1, K2) data extracted from the special purpose serial interface ports can be inserted into the D4-D12, E2, S1, K1 and K2 bytes, respectively.
- All bytes in the line overhead that are reserved for national use can be overwritten with 0x00.
- All bytes in the line overhead that are reserved for future international standardization can be overwritten with 0x00.
- The H1, H2, and H3 bytes from the Transmit Overhead Access Port (TOAP) can be inserted into the H1, H2, and H3 overhead bytes, or applied as an error mask to the H1, H2, and H3 overhead bytes.

**Receive SONET/SDH Path Processor**

- The H1 and H2 pointer bytes are detected and interpreted according to T1.105 and G.707. The mechanism is programmable to support both SONET and SDH. Path Alarm Indication Signal (AIS-P) and Loss of Pointer (LOP-P) alarm declarations are provided. Several pointer functions are also provided for diagnostic purposes.
- The H1 and H2 pointer bytes are monitored for Concatenation Indication (CI). Loss of Pointer (LOPX) and AIS (AISX) alarm declarations are provided.
- Path BIP-8 errors carried in the B3 byte are detected and accumulated. Both individual and block mode accumulation of B3 errors are supported.
- Path REI error indications carried in the G1 byte are detected and accumulated. Up to 64000 individual errors can be detected per second. Both individual and block mode accumulation of Path REI error indications are supported.
- The Path RDI carried in the G1 byte is detected and programmable.
- The Signal Label carried in the C2 byte is detected, alarmed and is programmable.

**Transmit SONET/SDH Path Processor**

- The H1 and H2 pointer byte values are programmable to support both SONET and SDH. Several pointer functions are provided for diagnostics purposes. The remaining 47 H1 and H2 bytes are programmable.
- The Path BIP-8 is computed and placed in the B3 byte of the current frame. It is possible to insert B3 errors for diagnostic purposes.
- The number of Path BIP-8 errors detected in the Receive Path Overhead Processor (RPOP) is backreported as Path REI in the G1 byte. Both individual and block mode backreporting for G1 are supported.
- It is possible to enable/disable RDI-P insertion for each of the following alarms: LOS, LOF, AIS-L, AIS-P, LOP-P, TIM-P, UNEQ-P, LCD-P and PLM-P. Both the latest and earlier definitions of RDI-P are supported.
- The Path Signal Label (C2) byte value is programmable.
- The Path Trace (J1) byte value is programmable.
- The F2, H4, Z3, Z4, and Z5 bytes are programmable.

#### Receive PPP/HDLC Processor

- The byte value used to identify the HDLC Flag Sequence is programmable.
- The detection and discarding of invalid frames are programmable.
- The expected Control Escape byte value and the Octet Destuffing Masking byte are programmable.
- The expected Address and Control Field values are programmable.
- The Protocol Field declaration and processing is programmable.
- The Abort Sequence is detected in the incoming HDLC frames.
- The received Frame Check Sequence (FCS) field is verified. The FCS checksum is calculated using either a 16-bit, CRC-CCITT generating polynomial  $1 + x^5 + x^{12} + x^{16}$ , or a 32-bit, CRC-32 generating polynomial  $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$ .
- The received data is descrambled with the self synchronizing scrambler (SSS) polynomial  $1 + x^{43}$ . Full and/or partial descrambling can be independently enabled/disabled.
- Long and short packet checking are provided and are programmable.
- Self Describing Padding is supported and programmable.
- The storage of the PPP Protocol Field in the Rx FIFO may be enabled/disabled.
- The size of the Rx FIFO size is 4095 words, which may accommodate storage for a total of 16380 PPP Protocol/Information Field bytes.
- The definition of received “errored” HDLC frames is programmable. For these errored HDLC frames two different procedures can be applied.
- The following statistics are provided in the performance monitoring 32-bit counters:
  - Received Aborted HDLC frames
  - Received FCS errored HDLC frames
  - Received Empty HDLC frames
  - Received HDLC frames where Address-and-Control-Field-Compression was found
  - Received HDLC frames with mismatching Protocol Field
  - Received Long packets
  - Received Short packets
  - Received Invalid Frames
  - Received bytes pre-octet destuffing
  - Received bytes post-octet destuffing
  - Received number of frames excluding Invalid Frames
  - Packets stored in the Rx FIFO
  - Packets stored in the Rx FIFO that are error marked
  - Packet bytes stored in the Rx FIFO

- Number of received PPP padding bytes
- The SPE Transparent Mode is provided to allow all of the SPE payload to pass directly to the Rx FIFO without further processing.
- A filtering function is provided to perform packet discartion and error marking based on a set of programmable labels. There are four programmable label matching triggers, and one complement word matching trigger that functions the packet discard and TERR marking.

#### **Transmit PPP/HDLC Processor**

- The inserted HDLC Flag Sequence byte and the minimum number of Flag Sequence bytes separating HDLC frames are programmable.
- The insertion of the Address and Control fields can be controlled by the HDLC Address-and-Control-Field-Compression mechanism.
- The Address Field inserted after the beginning Flag Sequence is programmable.
- The Control Field inserted after the the Address Field is programmable.
- The Frame Check Sequence (FCS) can be generated using either a 16-bit, CRC-CCITT generating polynomial  $1 + x^5 + x^{12} + x^{16}$ , or a 32-bit CRC-32 generating polynomial  $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$ .
- Octet Stuffing, or “escaping”, can be applied after the FCS generation and partial scrambling, if enabled. The Control Escape byte and the Octet Stuffing Masking byte are programmable. The Async-Control-Character-Map (ACCM) can accommodate a maximum of 5 byte values. Each value can be individually enabled/disabled.
- The transmitted data is scrambled with a self-synchronizing scrambler (SSS) polynomial  $1 + x^{43}$ . Full and/or partial scrambling can be independently enabled/disabled.
- The PPP Protocol Field can be generated internally or extracted from the transmit FIFO. The size and value of the inserted Protocol Field are programmable when generated internally.
- The Tx FIFO is programmable in the range from 1 to 4095 words or 16380 bytes of data storage. All valid packet bytes stored in the Tx FIFO are read out and mapped into the PPP Protocol/Information Fields of generated PPP/HDLC frames.
- Two Tx PIF packet transfer modes are supported: packet transfer mode and word transfer mode.
- The TXF\_ERR signal is provided to force insertion of errors into the FCS, or to force abort the transmitted HDLC frame.
- It is possible to force XOR'ing of the transmitted Address, Control or Protocol Fields with a programmable mask value via the CPU interface for diagnostic purposes.
- The following statistics are provided in the performance monitoring 32-bit counters:
  - Bytes read from Tx FIFO

- Transmitted good HDLC frames (non-aborted, non-FCS errored)
  - Transmitted Aborted HDLC frames
  - Transmitted FCS Errored HDLC frames
  - Long packets read from Tx FIFO
  - Short packets read from Tx FIFO
  - Transmitted empty HDLC frames
  - Bytes pre octet-stuffing (excluding Abort sequences)
  - Bytes post octet-stuffing (excluding Abort sequences)
- The SPE Transparent Mode is provided to allow the Tx FIFO content to be passed directly into the SPE payload without further processing.

#### **Receive ATM Processor**

- Cell Delineation is provided using shortened cyclic code with a generating polynomial  $1 + x + x^2 + x^8$ . The coset polynomial  $1 + x^2 + x^4 + x^8$  can be added to the calculated HEC check bits before comparison.
- Single-bit header error correction is supported. The dropping of cells during single or multiple error detection is programmable.
- The 48 byte information field is descrambled with a self-synchronizing descrambler polynomial  $1 + x^{43}$ . Descrambling can be enabled/disabled.
- Cells can be filtered based on a programmable cell header pattern in the GFC, PTI, or CLP fields.
- The number of correctable and uncorrectable HEC errors detected, and the number of cells written to the Rx FIFO are monitored.
- The Rx FIFO can accommodate storage of eight ATM cells.

#### **Transmit ATM Processor**

- The ATM cells are mapped into the STS-48c SPE or equivalent SDH VC-16-16c. Programmable idle/unassigned cells are inserted into the cell stream.
- The 48 byte information field is scrambled with a self-synchronizing descrambler polynomial  $1 + x^{43}$ . Scrambling can be enabled/disabled.
- The HEC generator performs a CRC-8 calculation over the first four header octets using the generating polynomial  $1 + x + x^2 + x^8$ . The coset polynomial  $1 + x^2 + x^4 + x^6$  can be added to the result. The HEC is optionally inserted into the fifth octet of the header of cells read from the Tx FIFO.
- The Tx FIFO can accommodate storage of eight ATM cells.

#### **Section and Path Trace Buffers**

- It is possible to perform read and write operations on every byte of the Section and Path Trace Buffers via the CPU interface and indirect addressing.
- The Section Trace Message (J0) and Path Trace Message (J1) bytes supports three different message formats: one byte (SONET) message, 16 byte (SDH) message, and 64 byte (SONET CLLI) message.

- The received section and path messages are checked for persistency by using internal counters. These counters are programmable.
- A mismatch in the accepted J0 and J1 bytes are alarmed and programmable.
- It is possible to insert a programmable section trace message and a path trace message in the three formats. It is possible to force insert all "0"s in the J0 and/or J1 bytes.

#### **Line Side Interface**

- A parity bit, programmable for even/odd parity, is provided each for the incoming and outgoing datapaths.
- The reference signal derived from the receive clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the receive clock. The 8kHz reference signal can also be phase locked to the incoming SONET/SDH frame.
- The reference signal derived from the transmit clock input can be programmed to be 8kHz, 19MHz, 38MHz, or 78MHz frequency locked to the transmit clock. The 8kHz reference signal can also be phase locked to the outgoing SONET/SDH frame.
- The Loss of Optical Carrier (LOPC) signal is monitored.
- The internal receive circuitry clock domain can be set equal to the internal transmit circuitry clock domain during Loss of Signal (LOS) or assertion of the LOPC input signal.
- The reset of the transmit and receive input clocks during a hardware/software master reset can be enabled/disabled.
- The transmit Line Side Interface provides a direct-looped version of the transmit clock input.
- The TLSYNC reset signal is intended to be used in STS-192/STM-64 applications. The generation of the SONET/SDH frame is aligned to the incoming TLSYNC signal.
- Frame pulses for both the transmit and receive Line Side Interfaces is intended to be used in STS-192/STM-64 applications.

#### **Drop Side Interface (POS/ATM Interface)**

- A parity bit, programmable for even/odd parity, is provided for each transmit and receive datapaths.
- The Drop Side Interface provides an industry compliant packet interface for POS operations.
- The packet interface supports word-level and packet-level transfer modes.
- The DTPA signal is provided to indicate the waterlevel of the Tx FIFO counted at word level and is programmable.
- It is possible to force reset/flush the contents in the Tx FIFO via the CPU interface.
- It is possible to force reset/flush the contents in the Rx FIFO via the CPU interface.
- The Drop Side Interface provides a Single-PHY UTOPIA-3 interface for ATM operations.
- Two formats of the ATM cells are supported: 52 byte cell or 56 byte cell containing the HEC.

- The UTOPIA-3 interface supports both word-level and cell-level flow control.

#### **CPU Interface**

- All configuration bits are both writeable and readable and can be used regardless of the device clock source status, except for the reset state. Configuration bits include selection bits, interrupt masking bits, and programmable counter/control values.
- The transfer of information between the CPU Interface and the receive/transmit transport blocks are made without loss across clock domains and with MTBF equal or greater than 100 years.
- Eight programmable General Purpose Input/Output (GPIO) ports are available for monitoring and controlling external signals. All GPIOs can be used as bistable interrupts when configured as input ports.
- Clock activity monitors are implemented for all input clocks.
- All PM counters are implemented to saturate.

#### **Receive Transport Overhead Access Port**

- Two identical, but independent, special purpose ports are provided for the extraction of special purpose bytes from the SONET/SDH transport overhead and of certain SONET/SDH alarms specific to automatic protection switching (APS) applications.
- The frame pulse RSPFP is synchronized to the receive drop side frame pulses RXFPOUTA-D.
- The entire serialized transport overhead can be extracted from the serial output port RTOH[3..0].
- A frame pulse is provided for the first bit of the serial outputs.
- A write enable signal, RTOHVALID, is provided when data is present on RTOH[3..0].

#### **Transmit Overhead Access Port**

- Two identical, but independent, special purpose ports are provided for the insertion of special purpose bytes into the SONET/SDH transport overhead and of certain SONET/SDH alarms specific to automatic protection switching (APS) applications.
- The entire transport overhead is captured from the serial input ports TTOH[3..0]. The captured data can be selectively inserted into the corresponding overhead bytes of the transmitted SONET/SDH frame.
- The latency of the captured inputs is programmable.

#### **Bit Error Rate Monitoring**

- The monitoring is based on the Line BIP (B2) error code and is capable of measuring to  $10^{-10}$  BER.
- There are four independent BER monitors with individual accumulation periods and alarm thresholds.
- A saturation threshold is implemented for each BER monitor to specify the maximum number of errors that can be accumulated.
- All BER monitors can be reset.
- The BER Signal Degrade (BER-SD) alarm is based on BER monitors 1 and 2.

- The BER Signal Fail (BER-SF) alarm is based on BER monitors 3 and 4.

#### **JTAG**

- All device TTL outputs can be forced to a tri-state level.
- The TAP Controller is used to capture and shift test data throughout the test registers.
- The 4-bit Instruction register and associated decode determines the type of operation to be performed and which data register is to be used for the operation.
- The 32-bit Device ID register is used to identify the manufacturer, part number, and version of the device through the test port.
- The Bypass register is a single bit register that provides the means for system serial test data to bypass the device with only one TCK cycle delay.
- The 138-bit Boundary Scan register (BSR) provides the means to force values onto the device outputs and to capture values on the device inputs and internal output signals.

#### **Loopback Modes**

- Equipment loopback is performed by looping the output from the Transmit Section Overhead Processor (TSOP), in the transmit direction, back to the input of the Receive Section Overhead Processor (RSOP), in the receive direction. The equipment loopback mode is enabled via a programmable register bit.
- Facility loopback is performed by looping the data received on the receive Line Side Interface back to the transmit Line Side Interface. The facility loopback mode is enabled via a programmable register bit.
- The output from the Receive Section Overhead Processor (RSOP), in the receive direction, can be looped back to the input of the Transmit Section Overhead Processor (TSOP), in the transmit direction. A small FIFO is used to phase synchronize the two clock domains.
- The output from the Receive Line Overhead Processor (RLOP), in the receive direction, can be looped back to the input of the Transmit Line Overhead Processor (TLOP), in the transmit direction. A small FIFO is used to phase synchronize the two clock domains.
- In packet loopback mode, the packets are looped directly from the Tx FIFO to the Rx FIFO. A small FIFO structure is used to phase synchronize the two clock domains.
- In UTOPIA loopback mode, the ATM cells are looped directly from the Tx FIFO to the Rx FIFO. A small FIFO structure is implemented to phase synchronize the two clock domains.

## Package Pin Descriptions

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
RLCLK+/-	Parallel Line Receive Clock	I	PECL	Clock reference for the 2.5Gb/s receive flow carried in RLIN[15..0]. The clock frequency is nominally 155.52MHz equivalent to STS-48/STM-16 operation.
RLIN[15..0]+/-	Parallel Line Receive Data	I	PECL	Parallel data bus for the incoming STS-48/STM-16 data stream. RLIN[15] is the most significant bit. RLIN[15] is the first arriving bit on the serial data stream.is sampled on the rising edge of RLCLK+.
RLPRTY+/-	Parallel Line Receive Parity	I	PECL	Parity input (even/odd parity) for the parallel receive line data, RLIN[15..0] (optionally include RLFP). RLPRTY is sampled on the rising edge of RLCLK+.
RLFP+/-	Parallel Line Receive Frame Pulse	I	PECL	Frame pulse for the receive line interface. RLFP can be used instead of the internal framing circuit (based on A1A2 patterns) for synchronizing the receive processor. RLFP is sampled on the rising edge of RLCLK+.  RLFP is intended for use in STS-192/STM-64 applications.
RXRCLK	Receive Reference Clock	O	TTL	Reference clock derived from RLCLK in a 78MHz/38MHz/19MHz/8kHz version.
LOPC	Loss of Optical Carrier	I	TTL	LOPC is monitored and changes in the signal status may cause generation of an interrupt. This allows monitoring of optical failures via the device CPU interface. When LOPC is asserted, the receive processor is optionally clocked by the transmit clock (derived from TLCLK).
TLCLK+/-	Parallel Line Transmit Clock	I	PECL	Clock reference for the 2.5Gb/s transmit flow carried in TLOUT[15..0]. The clock frequency is nominally 155.52MHz equivalent to STS-48/STM-16 operation.
TLCLKOUT+/-	Parallel Line Transmit Looped Clock	O	PECL	Looped TLCLK signal. Timing for this clock is defined with reference to the TLOUT data bus signals. The clock frequency is nominally 155.52MHz equivalent to STS-48/STM-16 operation (same as TLCLK).
TLOUT[15..0]+/-	Parallel Line Transmit Data	O	PECL	Parallel data bus for the outgoing STS-48/ STM-16 data stream. TLOUT[15] is the most significant bit.TLOUT[15] is the first transmitted bit on the serial data stream. TLOUT[15..0] is generated on the rising edge of the incoming TLCLK+.
TLPRTY+/-	Parallel Line Transmit Parity	O	PECL	Parity output (even/odd parity) for the parallel transmitdata, TLOUT[15..0] (optionally includes TLFP). TLPRTY is generated on the rising edge of TLCLK+.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
TLFP+/-	Parallel Line Transmit Frame Pulse	O	PECL	Frame pulse for the transmit line interface. TLFP is a one clock cycle wide pulse coincident with either the first framing byte (A1), the first payload byte (first byte following Z0) or a 24 clock cycle wide pulse coincident with the A2 framing bytes. TLFP is generated on the rising edge of TLCLK+. TLFP is intended for use in STS-192/STM-64 applications.
TXRESET+/-	Transmit Reset	I	PECL	TXRESET is used for synchronously resetting the device transmit processor only. TXRESET is intended for use in STS-192/STM-64 applications.
TXRCLK	Transmit Reference Clock	O	TTL	Reference clock derived from TLCLK in a 78MHz/38MHz/19MHz/8kHz version.
LOS	Loss Of Signal	O	TTL	Status signal indicating if Loss Of Signal (LOS) has been detected. The LOS status is also available in an internal status register bit. The signal is active high.
LOF	Loss Of Frame	O	TTL	Status signal indicating if Loss Of Frame (LOF) has been detected. The LOF status is also available in an internal status register bit. The signal is active high.
RSPFP	Receive Special Purpose Frame Pulse	O	TTL	Frame reference for special purpose serial output ports RSPDAT_x. The frame pulse is a one clock cycle wide pulse coincident with the first bit on the serial dataActive high. RSPFP changes on the falling edge of RSPCLK_x. X = [1,2].
RSPCLK_1	Receive Special Purpose Clock 1	O	TTL	Clock reference for receive special purpose serial output port 1. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of RSPDAT_1.
RSPDAT_1	Receive Special Purpose Data 1	O	TTL	Data output for special purpose serial port 1. RSPDAT_1 changes on the falling edge of RSPCLK_1.
RSPVALID_1	Receive Special Purpose Valid 1	O	TTL	Valid qualifier for special purpose serial port 1. RSPVALID_1 is asserted (programmable level) when there is valid data on RSPDAT_1. RSPVALID_1 changes on the falling edge of RSPCLK_1.
RSPCLK_2	Receive Special Purpose Clock 2	O	TTL	Clock reference for receive special purpose serial output port 2. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of RSPDAT_2.
RSPDAT_2	Receive Special Purpose Data 2	O	TTL	Data output for special purpose serial port 2. RSPDAT_2 changes on the falling edge of RSPCLK_2.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
RSPVALID_2	Receive Special Purpose Valid 2	O	TTL	Valid qualifier for special purpose serial port 2. RSPVALID_2 is asserted (programmable level) when there is valid data on RSPDAT_2. RSPVALID_2 changes on the falling edge of RSPCLK_2.
RTOHCLK	Receive Transport Overhead Clock	O	TTL	Clock reference for the receive transport overhead port. The clock is a 38.88MHz, 50% duty-cycle signal.
RTOHVALID	Receive Transport Overhead Valid	O	TTL	Valid qualifier for the receive transport overhead port. RTOHVALID is asserted (programmable level) when there is valid data on RTOH[3..0]. RTOHVALID changes on the falling edge of RTOHCLK.
RTOHFP	Receive Transport Overhead Frame Pulse	O	TTL	Frame reference for the receive transport overhead port. RTOHFP is a one clock cycle wide pulse coincident with the first bit(s) of the first A1 being output on RTOH[3..0]. RTOHFP changes on the falling edge of RTOHCLK.
RTOH[3..0]	Receive Transport Overhead Data	O	TTL	Data output for the receive transport overhead (section and line) bytes extracted from the incoming STS-48 signal. RTOH[3..0] changes on the falling edge of RTOHCLK. Mode 1: RTOH[3] carries the transport overhead from STS-12 #1 (first interleaved STS-12), RTOH[2] carries the transport overhead from STS-12 #2, etc. Mode 2: RTOH[3..0] carries the entire transport overhead in the order the overhead bytes are received. The most significant nibble (first received) is output first. RTOH[3] is most significant bit.
TSPCLK_1	Transmit Special Purpose Clock 1	O	TTL	Clock reference for the transmit special purpose serialport 1. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of TSPDAT_1).
TSPFP_1	Transmit Special Purpose Frame Pulse 1	O	TTL	Frame reference for the special purpose serial output port TSPDAT_1. Mode 1 (TSPCLK_1 continuous): The frame pulse is a one clock cycle wide pulse indicating the start of a new data stream on TSPDAT_1. When TSPFP_1 is asserted, the first bit of TSPDAT_1 is sampled on the second rising edge thereafter. TSPFP_1 changes on the falling edge of TSPCLK_1. Mode 2 (TSPCLK_1 gapped): The frame pulse is a one clock cycle wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT_1. When TSPFP_1 is asserted, the first bit of TSPDAT_1 is sampled on the second rising edge thereafter. TSPFP_1 changes on the falling edge of TSPCLK_1.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
TSPREN_1	Transmit Special Purpose Read Enable 1	O	TTL	Read enable signal for the TSPDAT_1 data stream. The response latency from TSPREN_1 is asserted until TSPDAT_1 is sampled is programmable. TSPREN_1 changes on the falling edge of TSPCLK_1.
TSPDAT_1	Transmit Special Purpose Data 1	I	TTL	Serial data input for transmit special purpose port 1. TSPDAT_1 is sampled on the rising edge of TSPCLK_1.
TSPCLK_2	Transmit Special Purpose Clock 2	O	TTL	Clock reference for the transmit special purpose serialport 2. The clock is a 2.16MHz, 50% duty-cycle signal (optionally gapped to match the bandwidth of TSPDAT_2).
TSPFP_2	Transmit Special Purpose Frame Pulse 2	O	TTL	Frame reference for the special purpose serial output port TSPDAT_2. Mode 1 (TSPCLK_2 continuous): The frame pulse is a one clock cycle wide pulse indicating the start of a new data stream on TSPDAT_2. When TSPFP_2 is asserted, the first bit of TSPDAT_2 is sampled on the second rising edge thereafter. TSPFP_2 changes on the falling edge of TSPCLK_2. Mode 2 (TSPCLK_2 gapped): The frame pulse is a one clock cycle wide pulse (variable width due to the gapped clock) indicating the start of a new data stream on TSPDAT_2. When TSPFP_2 is asserted, the first bit of TSPDAT_2 is sampled on the second rising edge thereafter. TSPFP_2 changes on the falling edge of TSPCLK_2.
TSPREN_2	Transmit Special Purpose Read Enable 2	O	TTL	Read enable signal for the TSPDAT_2 data stream. The response latency from TSPREN_2 is asserted until TSPDAT_2 is sampled is programmable. TSPREN_2 changes on the falling edge of TSPCLK_2.
TSPDAT_2	Transmit Special Purpose Data 2	I	TTL	Serial data input for transmit special purpose port 2. TSPDAT_2 is sampled on the rising edge of TSPCLK_2.
TTOHCLK	Transmit Transport Overhead Clock	O	TTL	Clock reference for the transmit transport overhead port. The clock is a 38.88MHz, 50% duty-cycle signal.
TTOHFP	Transmit Transport Overhead Frame Pulse	O	TTL	Frame reference for the transmit transport overhead port. TTOHFP is a one clock cycle wide pulse indicating the start of a new data stream on TTOH[3..0]. The response latency from TTOHFP is asserted until the first bit on TTOH[3..0] is sampled is programmable (see TTOHREN). TTOHFP changes on the falling edge of TTOHCLK.
TTOHREN	Transmit Transport Overhead Read Enable	O	TTL	Read enable signal for the TTOH[3..0] data stream. The response latency from TTOHREN is asserted until TTOH[3..0] is sampled is programmable. TTOHREN changes on the falling edge of TTOHCLK.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
TTOHEN	Transmit Transport Overhead Enable	I	TTL	<p>Enable signal for the TTOH[3..0] data stream. If TTOHEN is asserted, the corresponding byte will be inserted in the corresponding transport overhead byte of the outgoing STS-48 data stream.</p> <p>Mode 1: Transport overhead for each of the four STS-12 channels will be input in bit-serial format on the four data inputs (see TTOH[3..0] description). If TTOHEN is asserted during the first bit of an overhead byte, the corresponding overhead byte on TTOH[3] will be enabled, if TTOHEN is asserted during the third bit of an overhead byte, the corresponding overhead byte on TTOH[2] will be enabled (similar for TTOHEN assertion during fifth and seventh bits).</p> <p>Mode 2: Transport overhead for the entire STS-48 is input as 4-bit nibbles on the TTOH[3..0] port (see TTOH[3..0] description). If TTOHEN is asserted during the first nibble of an overhead byte, the corresponding overhead byte is enabled.</p> <p>Note: The transmit section and line processing blocks can selectively overwrite/modify overhead bytes inserted through the TTOH interface.</p>
TTOH[3..0]	Transmit Transport Overhead Data	I	TTL	<p>Data input for the transport overhead (section and line) bytes to be inserted in the outgoing STS-48 signal. TTOH[3..0] is sampled on the rising edge of TTOHCLK.</p> <p>Mode 1: TTOH[3] carries the transport overhead for STS-12 #1 (first interleaved STS-12), TTOH[2] carries the transport overhead for STS-12 #2, etc.</p> <p>Mode 2: TTOH[3..0] carries the entire STS-48 transport overhead in the order the overhead bytes are to be inserted. The most significant nibble (first received) is input first. TTOH[3] is the most significant bit.</p>
D[7..0]	CPU Data	B	TTL	Bidirectional data bus is used to transfer data for microcontroller read/write access to internal UNI registers.
A[7..0]	CPU Address	I	TTL	Address bus selects specific internal registers during register read/write access.
ALE	CPU Address Latch Enable	I	TTL	Controls internal latching of the address bus signals. When low the address bus A[7..0] is latched internal. When high the internal address bus latches are transparent. This will allow for interfacing to a multiplexed address/data. The ALE signal has an internal pull-up resistor.
CSB	CPU Chip Select (active low)	I	TTL	Must always be asserted during register read/write access cycles. The CSB signal is used in conjunction with either the RDB or the WRB signal. The CSB signal has an internal pull-up resistor.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
WRB	CPU Write Enable (active low)	I	TTL	Used for register write operations. The D[7..0] content is written into the by A[7..0] selected register when WRB and CSB are both asserted (low). The WRB signal has an internal pull-up resistor.
RDB	CPU Read Enable (active low)	I	TTL	Used for register read operations. The D[7..0] will drive register content of the by A[7..0] selected register when RDB and CSB are both asserted (low). The RDB signal has an internal pull-up resistor.
INTB	CPU Interrupt (active low)	O	TTL	Asserted when an internal interrupt source is pending and the interrupt is unmasked (enabled). The INTB signal is deasserted when the interrupt pending bits have been cleared. The INTB is an open drain signal.
RSTB	Chip Reset (active low)	I	TTL	Asynchronous reset of the device. The device is held in a reset state while the RSTB signal is low. The signal is triggered with an internal pull-up resistor. All outputs are tristated when RSTB is asserted.
PMTICK	Performance Monitoring Tick	B	TTL	Output. Asserted when the internal PMTICK timer generates a tick for latching performance counters in the device. Input: A low-to-high transition will (optionally) trigger latching of performance monitoring counters in the device.
GPIO[7..0]	General Purpose Input/Output	BI	TTL	Individually configurable as inputs or outputs. Intended for controlling monitoring external devices.
TDO	JTAG Test Data Output	O	TTL	This signal carries test data out of the device via the IEEE P1149.1 test access port. TDO is updated on the falling edge of TCK. The TDO signal is a tristate output which is inactive except when data scan shifting is in progress.
TDI	JTAG Test Data Input	I	TTL	The signal carries test data into the device via the IEEE P1149.1 test access port. TDI is sampled on the rising edge of TCK. TDI has an internal pull-up resistor.
TCK	JTAG Test Clock	I	TTL	This signal provides timing for test operations that are carried out using the IEEE P1149.1 test access port.
TMS	JTAG Test Mode Select	I	TTL	This signal controls the test operations that are carried out using the IEEE P1149.1 test access port. TMS is sampled on the rising edge of TCK. TMS has an internal pull-up resistor.
TRSTB	JTAG Test Reset (active low)	I	TTL	This signal provides an asynchronous test access port reset via the IEEE P1149.1 test access port. TRSTB is a schmitt triggered input with an internal pull-up resistor.
OE	Chip Output Enable (active high)	I	TTL	When deasserted (set low), all TTL device outputs are tristated. The OE signal has an internal pull-up.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
POS Mode: TDAT[31..0] ATM Mode: TUDATA[31..0]	Transmit Packet Data Bus / UTOPIA Transmit Data Bus	I	TTL	POS Mode: Four-octet true data driven from Packet to PHY layer. TDAT[31] is MSB. Packets are aligned to 32 bit TDAT boundary. ATM Mode: Four-octet true data driven from ATM to PHY layer. TUDATA[31] is MSB.
POS Mode: TPRTY ATM Mode: TUPRTY	Transmit Bus Parity / UTOPIA Transmit Bus Parity	I	TTL	POS Mode: TPRTY is the odd/even (programmable, default odd) parity bit over TDAT[31..0]. The signal is only valid when asserted simultaneously with TXENB. ATM Mode: TUPRTY is the odd/even (programmable, default odd) parity bit over TUDATA[31..0], driven by the ATM layer. The signal is only valid when asserted simultaneously with TUPRTY*.
POS Mode: TMOD[1..0]	Transmit Word Modulo	I	TTL	POS Mode only: Data Qualifier. Qualifier for the four TDAT bytes. Defines which of the four TDAT bytes contains valid data.
POS Mode: TSOP ATM Mode: TUSOC	Transmit Start Of Packet / UTOPIA Transmit Start Of Cell	I	TTL	POS Mode: Active high signal asserted by the packet layer when TDAT contains the first valid byte of the packet. The signal is invalid when asserted simultaneously with TXENB. The packet interface can be operated without using this signal. ATM Mode: Start Of Cell. Active high signal asserted by the ATM layer when TUDATA contains the first valid byte of the cell. The signal is only valid when asserted simultaneously with TUPRTY*.
POS Mode: TEOP	Transmit End Of packet	I	TTL	POS Mode only: Is asserted by the packet layer when TDAT contains the last valid byte of the packet. The signal is only valid when asserted simultaneously with TXENB. Active high signal.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
POS Mode: DTPA ATM Mode: TUFULL*/ TUCLAV	Transmit Polled- PHY Packet Available / Transmit Full/Cell Available	O	TTL	POS Mode: DTPA transitions high when a programmable minimum number of bytes are available in the Tx FIFO. Once high, the PTPA indicates that the Tx FIFO is not full. WHEN DTPA transitions low, it optionally indicates that the Tx FIFO is full or near full. ATM Mode: For UTOPIA flow control. The TUFULL* definition applies to word level flow control, and TUCLAV definition applies to cell level flow control.
POS Mode: TERR	Transmit Error Indicator	I	TTL	POS Mode only: May be used to force HDLC frame abortion of insertion of FCS error in the transmitted HDLC/PPP frames. The TX-ERR value is only relevant for the TXEOP marked word, and ingored for all other word writes.
POS Mode: TENB ATM Mode: TUENB	Transmit Write Enable / Transmit Write Enable	I	TTL	POS Mode: Active low signal asserted by the packet layer during cycles when TDAT contains valid packet data. ATM Mode: Active low signal asserted by the ATM layer during cycles when TUDATA contains valid cell data.
POS Mode: TFCLK ATM Mode: TUCLK	Transmit FIFO Write Clock / Transmit Write Clock	I	TTL	POS Mode: Transfer/synchronization clock provided by the packet layer to the PHY layer for synchronizing transfers on TDAT. ATM Mode: Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on TUDATA.
POS Mode: TFCLKO ATM Mode: TUCLKO	Transmit FIFO Write Clock Looped / Transmit Clock Looped	O	TTL	POS Mode: The TFCLK input looped back out. ATM Mode: The TUCLK input looped back out.
POS Mode: RDAT[31..0] ATM Mode: RUDATA[31..0]	Receive Packet Data Bus / Receive Cell Data Bus	O	TTL	POS Mode: Four-octet true data driven from PHY to packet layer. RDAT[31] is MSB. Packets are aligned to 32 bit RDAT boundary. ATM Mode: Four-octet wide data driven from PHY to ATM layer. RUDATA[31] is the MSB.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
POS Mode: RPRTY ATM Mode: RUPRTY	Receive Bus Parity / Receive Bus Parity	O	TTL	POS Mode: RXPRTY is the odd/even (programmable, default odd) parity bit over RDAT[31..0]. ATM Mode: RUPRTY is the odd/even (programmable, default odd) parity for RUDATA[31..0].
POS Mode: RMODE[1..0]	Receive Word Module	O	TTL	POS Mode only: Data Qualifier. Qualifier for the four RDAT bytes. Defines which of the four RDAT bytes contains valid data.
POS Mode: RSOP ATM Mode: RUSOC	Receive Start Of Packet / Receive Start Of Cell	O	TTL	POS Mode: Start Of Packet. Is asserted when TXDATA contains the first valid byte of the packet. Active high signal. The interface can be operated without using this signal. ATM Mode: Active high signal asserted by the PHY layer when RUDATA contains the first valid byte of a cell. To support multiple PHY configurations.
POS Mode: REOP	Receive End Of Packet	O	TTL	POS Mode only: Start Of Packet. Is asserted when RDAT contains the first valid byte of the packet. Active high signal.
POS Mode: PRPA ATM Mode: RUEMPTY*/ RUCLAV	Receive Packet Available / Receive Empty/ Cell Available.	O	TTL	POS Mode: PRPA indicates when data is available in the polled receive FIFO. When PRPA is high, the receive FIFO has at least one end of packet or a programmable number of bytes to read. PRPA is low when the receive FIFO fill level is below the assertion threshold and the FIFO contains no end of packet ATM Mode: For UTOPIA flow control. The RUEMPTY* definition applies to word level flow control, and RUCLAV definition applies to cell level flow control.
POS Mode: RVAL	Receive Data Valid	O	TTL	POS Mode only: RVAL indicates the validity of the receive data signals. When RVAL is high, the receive signals (RDAT, RSOP, REOP, RMOD, RXPRTY and RERR) are valid. When RVAL is low, all receive signals are invalid and must be disregarded. RVAL will transition low on a FIFO empty condition or on an end of packet. No data will be removed from the receive FIFO while RVAL is deasserted. Once deasserted, RVAL will remain deasserted until current PHY has been deselected.

**Table 1: Signal Definitions**

<i>Signal</i>	<i>Name</i>	<i>I/O</i>	<i>IO Type</i>	<i>Description</i>
POS Mode: RERR	Receive Error Indicator	O	TTL	POS Mode only: Indicates if the packet contained an error (e.g. Abort/FCS error). Active high signal.
POS Mode: RENB ATM Mode: RUENB	Receive Read Enable / UTOPIA Read Enable	I	TTL	POS Mode: Active low signal asserted by the packet layer to indicate that RX* output signals will be sampled at the end of the next cycle. ATM Mode: Active low signal asserted by the ATM layer to indicate that RUDATA, RUSOC and RXPRTY will be sampled at the end of the next cycle.
POS Mode: RFCLK ATM Mode: RUCLK	Receive FIFO Write Clock / Receive Clock	I	TTL	POS Mode: Clock. Transfer/synchronization clock provided by the packet layer to the PHY layer for synchronizing transfers on TRDATA. ATM Mode: Clock. Transfer/synchronization clock provided by the ATM layer to the PHY layer for synchronizing transfers on RUDATA.
POS Mode: RFCLKO ATM Mode: RUCLKO	Receive FIFO Write Clock Looped / Receive Clock Looped	O	TTL	POS Mode: Looped clock. The RXCLK input looped back out. ATM Mode: The RUCLK looped back out.

## Package Pinout by Signal Name

**Table 2: Package Pinout**

<i>Signal</i>	<i>BGA pin</i>	<i>Signal</i>	<i>BGA Pin</i>	<i>Signal</i>	<i>BGA Pin</i>
RLIN[8]-	D3	GPIO[1]	K2	TLOUT[7]-	V2
RLIN[8]+	E4	GPIO[0]	L3	TLOUT[8]-	W1
RLIN[9]-	C1	VDD5	K1	TLOUT[8]+	U4
RLIN[9]+	D2	OE	L2	TLOUT[9]+	V3
RLIN[6]-	E3	TDO	M4	TLOUT[9]-	W2
RLIN[6]+	F4	TDI	L1	TLOUT[10]-	Y1
RLIN[7]-	D1	TCK	M3	TLOUT[10]+	W3
RLIN[7]+	E2	TMS	M2	TLOUT[12]+	Y2
RLIN[4]-	F3	TRSTB	M1	TLOUT[12]-	AA1
RLIN[4]+	G4	TLSYNC+	N3	TLOUT[11]+	W4
RLIN[5]-	E1	TLSYNC-	N2	TLOUT[11]-	Y3
RLIN[5]+	F2	TLOUT[0]-	P2	TLOUT[14]+	AA2
RLIN[2]-	G3	TLOUT[0]+	P3	TLOUT[14]-	AB1
RLIN[2]+	H4	TLOUT[2]+	P4	TLOUT[13]+	Y4
RLIN[3]-	F1	TLOUT[2]-	R1	TLOUT[13]-	AA3
RLIN[3]+	G2	TLOUT[1]+	R2	TLPRTY+	AB2
RLIN[1]+	H3	TLOUT[1]-	R3	TLPRTY-	AC1
RLIN[1]-	G1	TLOUT[3]-	T1	TLOUT[15]+	AA4
RLIN[0]-	H2	TLOUT[3]+	R4	TLOUT[15]-	AB3
RLIN[0]+	J3	TLOUT[5]+	T2	TLCLK-	AC2
GPIO[7]	K4	TLOUT[5]-	U1	TLCLK+	AD1
GPIO[6]	H1	TLOUT[4]+	T3	TLCLKOUT-	AB4
GPIO[5]	J2	TLOUT[4]-	U2	TLCLKOUT+	AC3
GPIO[4]	K3	TLOUT[6]+	T4	TLFP+	AD4
GPIO[3]	J1	TLOUT[6]-	V1	TLFP-	AC5
GPIO[2]	L4	TLOUT[7]+	U3	TXRCLK	AF3

**Table 2: Package Pinout**

<i>Signal</i>	<i>BGA pin</i>	<i>Signal</i>	<i>BGA Pin</i>	<i>Signal</i>	<i>BGA Pin</i>
RTOH[0]	AE4	TTOHFP	AF11	NC	AE20
RSPDAT1	AD5	TSPREN2	AD12	NC	AF21
RSPVALID1	AC6	NC	AE12	NC	AC19
RTOH[1]	AF4	NC	AF12	NC	AD20
RTOH[2]	AE5	NC_1	AD13	NC	AE21
RTOH[3]	AD6	NC	AE13	NC	AF22
RTOHVALID	AC7	NC	AE14	NC	AC20
RSPCLK1	AF5	NC	AD14	TFCLK	AD21
RSPFP	AE6	NC	AC14	TFCLKO	AE22
RSPCLK2	AD7	NC	AF15	TENB	AF23
RTOHFP	AC8	NC	AE15	DTPA	AC21
RSPDAT2	AF6	NC	AD15	TERR	AD22
RSPVALID2	AE7	NC	AF16	TEOP	AE23
RTOHCLK	AD8	NC	AC15	TSOP	AF24
TTOH[0]	AF7	NC	AE16	TPRTY	AC22
TTOH[1]	AE8	NC	AF17	TMOD[1]	AD23
TSPCLK1	AD9	NC	AD16	TMOD[0]	AC24
TSPDAT1	AC10	NC	AE17	TDAT[31]	AB23
TTOH[2]	AF8	NC	AC16	TDAT[30]	AD26
TTOH[3]	AE9	NC	AF18	TDAT[29]	AC25
TSPREN1	AD10	NC	AD17	TDAT[28]	AB24
TTOHEN	AF9	NC	AE18	TDAT[27]	AA23
TSPFP1	AC11	NC	AF19	TDAT[26]	AC26
TTOHREN	AE10	NC	AC17	TDAT[25]	AB25
TSPCLK2	AD11	NC_2	AD18	TDAT[24]	AA24
TTOHCLK	AF10	NC	AE19	TDAT[23]	Y23
TSPDAT2	AE11	NC	AF20	TDAT[22]	AB26
TSPFP2	AC12	NC	AD19	TDAT[21]	AA25

**Table 2: Package Pinout**

<i>Signal</i>	<i>BGA pin</i>	<i>Signal</i>	<i>BGA Pin</i>	<i>Signal</i>	<i>BGA Pin</i>
TDAT[20]	Y24	NC	M26	RDAT[8]	F23
TDAT[19]	W23	NC	M25	RDAT[7]	E24
TDAT[18]	AA26	NC	M24	RDAT[6]	D25
TDAT[17]	Y25	NC	M23	RDAT[5]	C26
TDAT[16]	W24	NC	L25	RDAT[4]	E23
TDAT[15]	Y26	RDAT[31]	K26	RDAT[3]	D24
TDAT[14]	W25	RDAT[30]	L24	RDAT[2]	C23
TDAT[13]	V24	RDAT[29]	K25	RDAT[1]	D22
TDAT[12]	U23	RDAT[28]	L23	RDAT[0]	A24
TDAT[11]	W26	RDAT[27]	J26	RMOD[1]	B23
TDAT[10]	V25	RDAT[26]	K24	RMOD[0]	C22
TDAT[9]	U24	RDAT[25]	J25	RPRTY	D21
TDAT[8]	V26	RDAT[24]	H26	RSOP	A23
TDAT[7]	T23	RDAT[23]	K23	RERR	B22
TDAT[6]	U25	RDAT[22]	J24	RVAL	C21
TDAT[5]	T24	RDAT[21]	H25	RENB	D20
TDAT[4]	U26	RDAT[20]	G26	RFCLK	A22
TDAT[3]	T25	RDAT[19]	H24	RFCLKO	B21
TDAT[2]	R23	RDAT[18]	G25	NC	C20
TDAT[1]	T26	RDAT[17]	F26	NC	D19
TDAT[0]	R24	RDAT[16]	H23	REOP	A21
NC	R25	RDAT[15]	G24	NC	B20
NC	R26	RDAT[14]	F25	NC_3	C19
NC	P24	RDAT[13]	E26	NC	A20
NC	P25	RDAT[12]	G23	NC	B19
NC	N25	RDAT[11]	F24	NC	C18
NC	N24	RDAT[10]	E25	NC	D17
NC	N23	RDAT[9]	D26	NC	A19

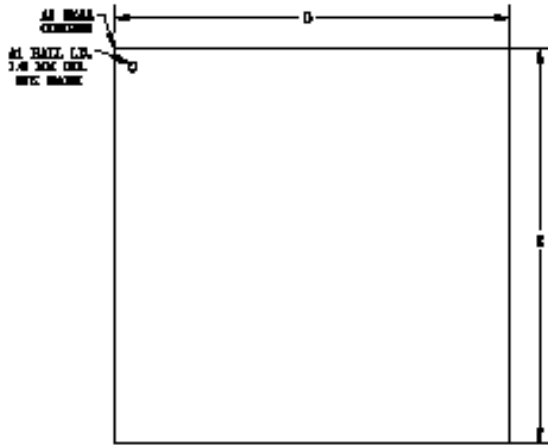
**Table 2: Package Pinout**

<i>Signal</i>	<i>BGA pin</i>	<i>Signal</i>	<i>BGA Pin</i>	<i>Signal</i>	<i>BGA Pin</i>
NC	B18	A[7]	A9	VDD	AC18
RXTS	C17	PMTICK	C10	VDD	AC23
TXTS	A18	LOF	B9	VDD	AD3
NC_0	D16	A[8]	A8	VDD	AD24
LCD-P	B17	CLKRSTEN	D10	VDD	AE2
LOS	C16	LOPC	C9	VDD	AE25
NC	A17	RXRCLK	B8	VDD	B2
D[0]	B16	RLFP-	A7	VDD	B25
RSTB	D15	RLFP+	C8	VDD	C3
D[1]	A16	RLPRTY-	B7	VDD	C24
D[2]	C15	RLPRTY+	A6	VDD	D4
D[3]	B15	RLCLK+	D8	VDD	D9
D[4]	A15	RLCLK-	C7	VDD	D14
D[5]	C14	RLIN[14]-	B6	VDD	D18
D[6]	B14	RLIN[14]+	A5	VDD	D23
D[7]	B13	RLIN[15]-	D7	VDD	J23
INTB	C13	RLIN[15]+	C6	VDD	J4
RDB	D13	RLIN[12]-	B5	VDD	N4
A[1]	A12	RLIN[12]+	A4	VDD	P23
A[2]	B12	RLIN[13]-	D6	VDD	V4
A[0]	C12	RLIN[13]+	C5	VDD	V23
A[3]	A11	RLIN[10]-	B4	GND	A1
WRB	D12	RLIN[10]+	A3	GND	A2
A[4]	B11	RLIN[11]-	D5	GND	A13
A[5]	A10	RLIN[11]+	C4	GND	A14
CSB	C11	VDD	AC4	GND	A25
A[6]	B10	VDD	AC9	GND	A26
ALE	D11	VDD	AC13	GND	B1

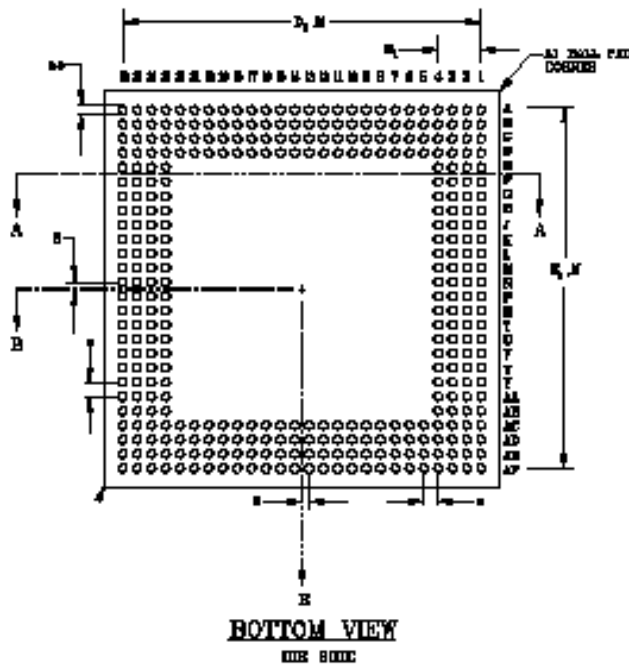
**Table 2: Package Pinout**

<i>Signal</i>	<i>BGA pin</i>	<i>Signal</i>	<i>BGA Pin</i>	<i>Signal</i>	<i>BGA Pin</i>
GND	B3				
GND	B24				
GND	B26				
GND	C2				
GND	C25				
GND	N1				
GND	N26				
GND	P1				
GND	P26				
GND	AD2				
GND	AD25				
GND	AE1				
GND	AE24				
GND	AE3				
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GND	AF1				
GND	AF2				
GND	AF13				
GND	AF14				
GND	AF25				
GND	AF26				

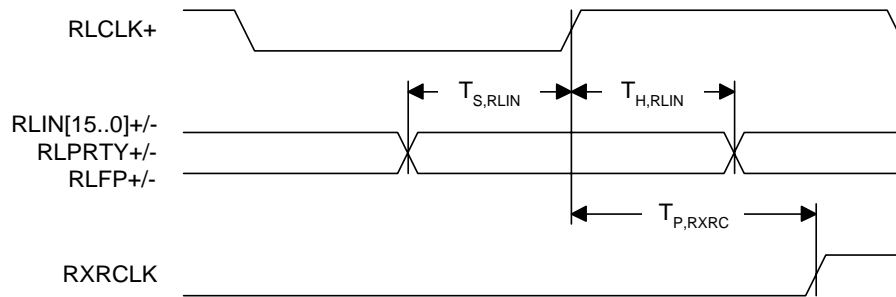
## Packaging Information



SYMBOL	MIN.	MOUL.	MAX.
A	1.41	1.64	1.87
A1	0.58	0.83	0.70
A2	0.05	0.01	0.07
D	24.80	25.00	25.10
D1	31.85	31.75	31.85
F	34.90	35.00	35.10
F1	31.88	31.78	31.88
MIN	P8 x P8		
UN	E-4		
b	0.80	0.75	0.90
e	1.27		
z	—	—	0.50



## AC Characteristics



**Table 1: Rx Line Interface**

<i>Symbol</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
fRFCLK	RFCLK clock frequency (nominal)	50	104	MHz
Tdc, RFCLK	RFCLK duty cycle	40	60	%
Tr/f, RFCLK	RFCLK rise/fall time	-	2.0	ns
Ts, RXIN	RENB setup time to RFCLK rising edge	1.5	-	ns
Th, RXIN	RENB hold time to RFCLK rising edge	1.0	-	ns
Tp, RXOUT	RFCLK rising edge to RDATA[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR valid	1.0	5.0	ns
Tp, RXCLKO	RFCLKO rising edge RDAT[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR valid.	0.0	1.5	ns

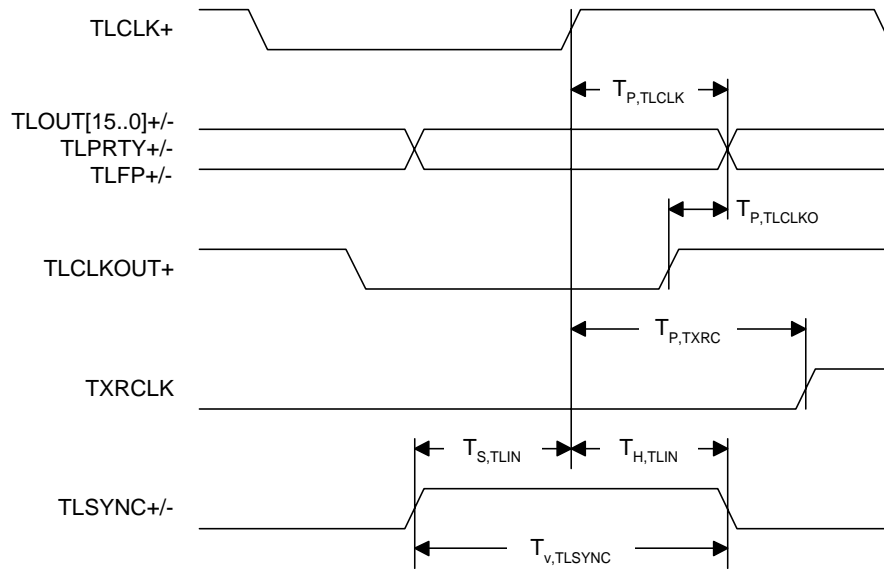
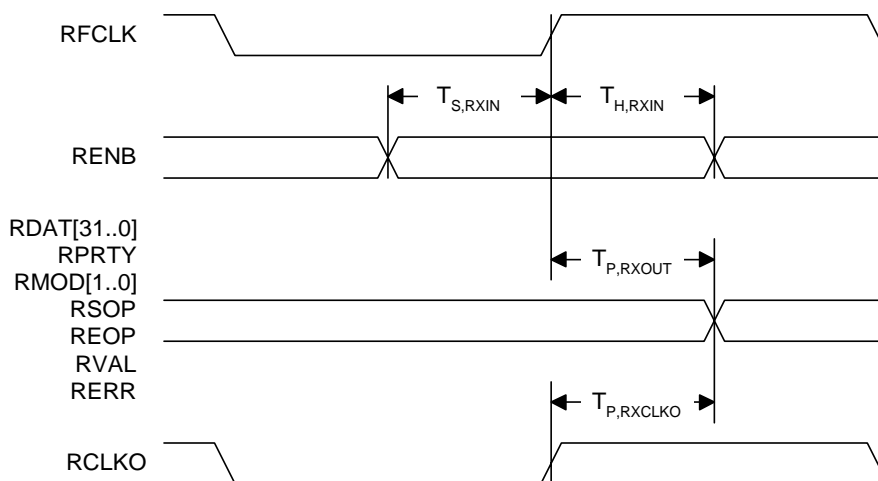


Table 2: Tx Line Interface

Symbol	Description	Min	Max	Unit
fTLCLK	TLCLK+/- clock frequency (nominal)	-	155.52	MHz
Tdc, TLCLK	TLCLK+/- duty cycle	35	65	%
Tdc, TLCLKO	TLCLKO+/- duty cycle	Tdc, TLCLK - (550ps x fTLCLK) %	%	
Tr/f, TLCLK	TLCLK+/- rise/fall time	-	1.0	ns
Tp, TLCLK	TLCLK+ rising edge to TLOUT[15..0]+/-. TLPRTY+/- and TLFP+/- valid *	1.0	4.0	ns
Tp, TLCLKO	TLCLKO+ rising edge to TLOUT[15..0]+/-. TLPRTY+/-, TLFP+/- valid	0	1.5	ns
Tp, TXRC	TLCLK+ rising edge to TXRCLK rising/falling edge	1.0	15	ns
fTXRCLK	fTLCLK divided by 2/4/8/19440	-	-	MHz
Tdc, TXRCLK	TXRCLK duty cycle	30	70	%
Ts, TLIN	TLSYNC+/- setup time to TLCLK+ rising edge 1)	2.0	-	ns
Th, TLIN	TLSYNC+/- hold time to TLCLK+ rising edge 1)	1.0	-	ns

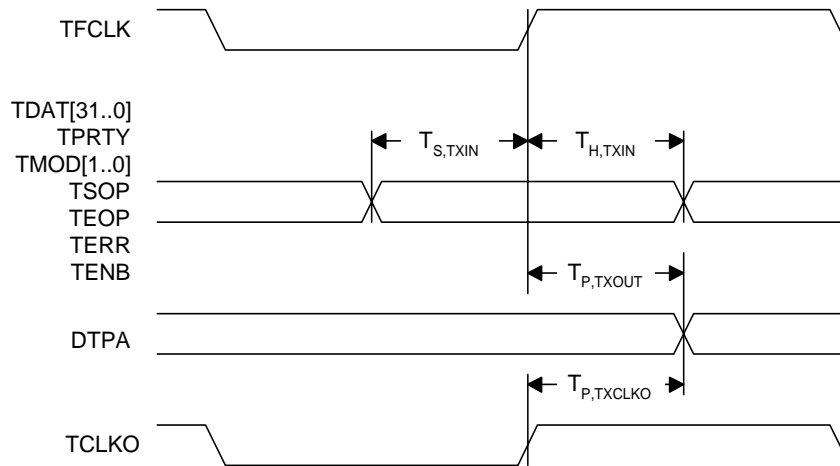
**Table 2: Tx Line Interface**

Symbol	Description	Min	Max	Unit
Tv, TLSYNC	Minimum required pulsewidth length	2 x		
1/ fTLCLK	-	-		



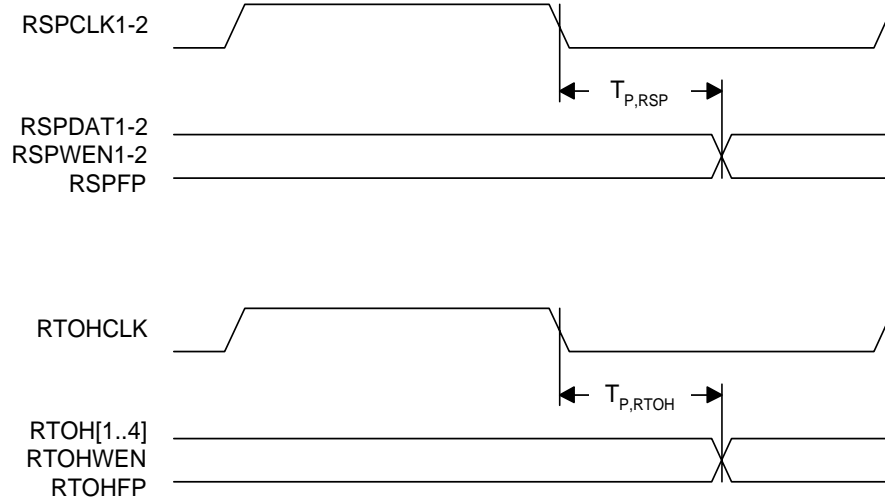
**Table 3: Rx Drop Interface**

Symbol	Description	Min	Max	Unit
fRFCLK	RFCLK clock frequency (nominal)	50	104	MHz
Tdc, RFCLK	RFCLK duty cycle	40	60	%
Tr/f, RFCLK	RFCLK rise/fall time	-	2.0	ns
Ts, RXIN	RENB setup time to RFCLK rising edge	2.0	-	ns
Th, RXIN	RENB hold time to RFCLK rising edge	1.0	-	ns
Tp, RXOUT	RFCLK rising edge to RDATA[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR valid	1.0	5.0	ns
Tp, RXCLKO	RFCLKO rising edge RDATA[31..0], RPRTY, RMOD[1..0], RSOP, REOP, RVAL and RERR valid.	0.0	1.5	ns



**Table 4: Tx Drop Interface**

<i>Symbol</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
fTFCLK	TFCLK clock frequency	50	104	MHz
Tdc, TFCLK	TFCLK duty cycle	40	60	%
Tr/f, TFCLK	TFCLK rise/fall time	-	2.0	ns
Ts, TXIN	TDAT[31..0], TPRTY, TMOD[1..0], TSOP, TEOP, TERR and TENB setup time to TFCLK rising edge	2.0	-	ns
Th, TXIN	TDAT[31..0], TPRTY, TMOD[1..0], TSOP, TEOP, TERR and TENB hold time to TFCLK rising edge	1.0	-	ns
Td, TXOUT	TFCLK rising edge to DTPA valid	1.0	5.0	ns
Tp, TXCLKO	TFCLKO rising edge to DTPA valid.	0.0	1.5	ns



**Table 5: Rx Overhead Access Port**

<i>Symbol</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
FRSPCLK	RSPCLK1-2 clock frequency (optionally gapped)	-	2.16	MHz
Tdc,RSPCLK	RSPCLK1-2 duty cycle	40	60	%
Tr/f, RSPCLK	RSPCLK1-2 rise/fall time	-	2.0	ns
TP,RSP	RSPCLK1-2 falling edge to RSPDAT1-2, RSPWEN1-2, RSPFP valid	-10	+10	ns
FRTOHCLK	RTOHCLK clock frequency (nominal)	-	38.88	MHz
Tdc, RTOHCLK	RTOHCLK duty cycle	40	60	%
Tr/f, RTOHCLK	RTOHCLK rise/fall time	-	2.0	ns
TP,RTOH	RTOHCLK falling edge to RTOH[1..4], RTOHWEN, RTOHFP valid	-4.0	+4.0	ns

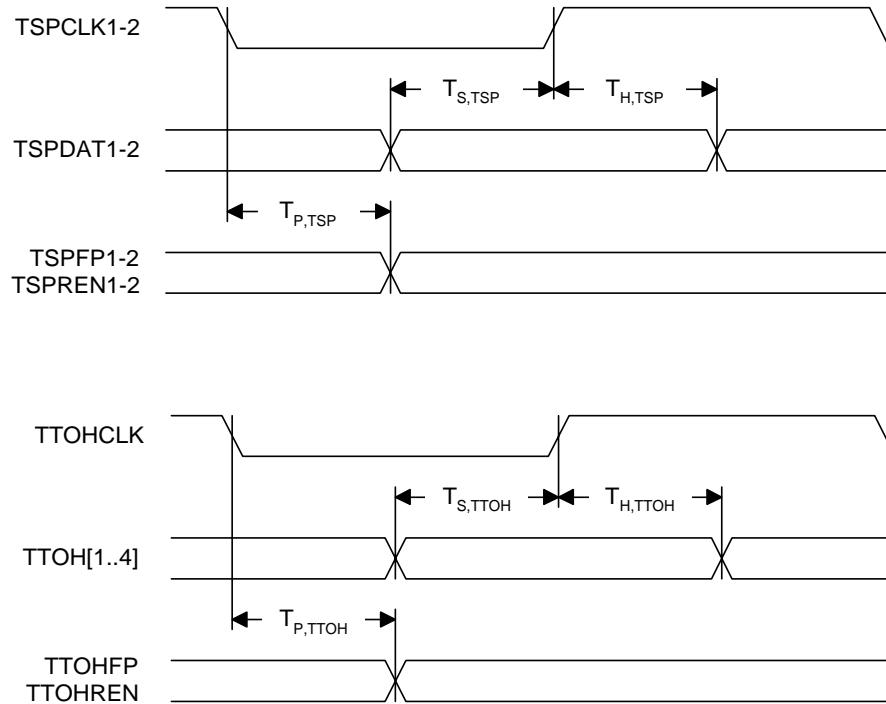
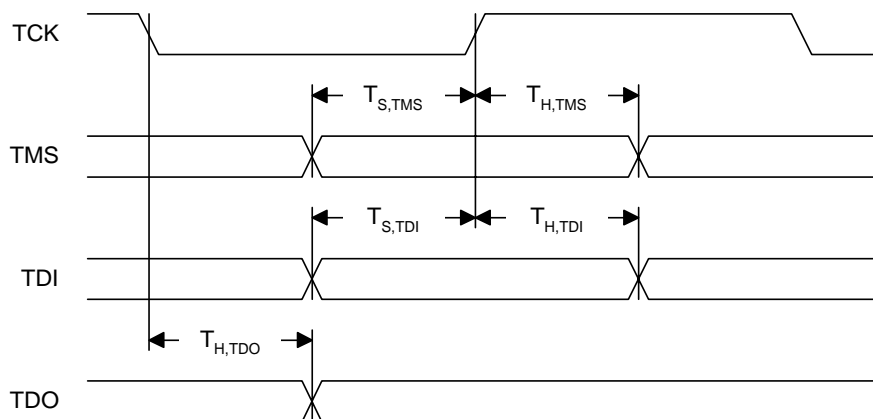


Table 6: Tx Overhead Access Port

Symbol	Description	Min	Max	Unit
FTSPCLK	TSPCLK1-2 clock frequency (optionally gapped)	-	2.16	MHz
Tdc,TSPCLK	TSPCLK1-2 duty cycle	40	60	%
Tr/f, TSPCLK	TSPCLK1-2 rise/fall time	-	2.0	ns
TS,TSP	TSPDAT1-2 setup time to TRSPCLK1-2 rising edge	10	-	ns
TH,TSP	TSPDAT1-2 hold time to TRSPCLK1-2 rising edge	10	-	ns
TP,TSP	TRSPCLK1-2 falling edge to TSPREN1-2, TSPFP1-2 valid	-10	+10	ns
FTTOHCLK	TTOHCLK clock frequency (nominal)	-	38.88	MHz
Tdc,TTOHCLK	TTOHCLK duty cycle	40	60	%
Tr/f,TTOHCLK	TTOHCLK rise/fall time	-	2.0	ns
TS,TTOH	TTOH[1..4] setup time to TTOHCLK rising edge	4.0	-	ns
TH,TTOH	TTOH[1..4] hold time to TTOHCLK rising edge	4.0	-	ns

**Table 6: Tx Overhead Access Port**

<i>Symbol</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
TP,TTIH	TTOHCLK falling edge to TTOHREN, TTOHFP valid	-4.0	+4.0	ns



**Table 7: JTAG Interface**

<i>Symbol</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
fTCK	TCK frequency	-	1	MHz
Tdc, TCK	TCK duty cycle	40	60	%
Ts, TMS	TMS setup time to rising TCK edge	50	-	ns
Th, TMS	TMS hold time to rising TCK edge	50	-	ns
Ts, TDI	TDI setup time to rising TCK edge	50	-	ns
Th, TDI	TDI hold time to rising TCK edge	50	-	ns
Ts, TDO	TCK falling edge to TDO valid	1.5	50	ns

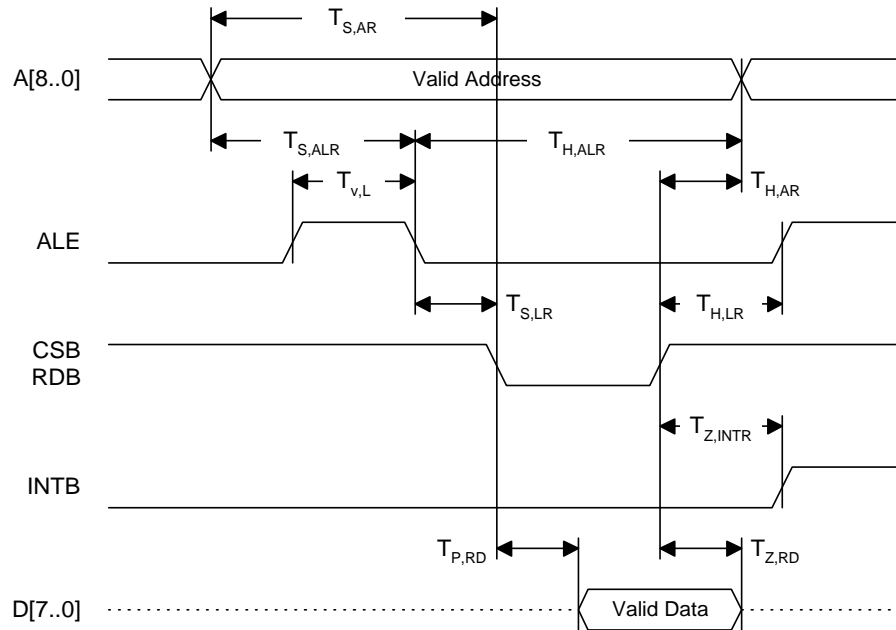
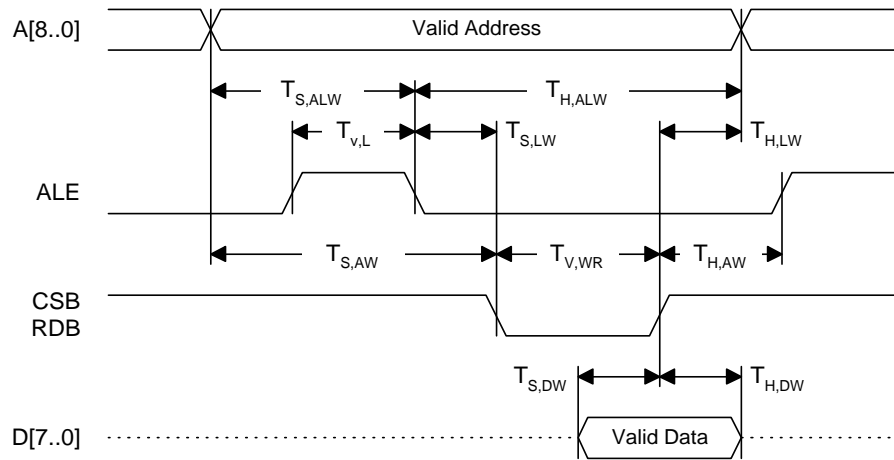


Table 8: CPU Read Access

Symbol	Description	Min	Max	Unit
$T_{s, AR}$	Address to valid read setup time	10	-	ns
$T_{h, AR}$	Address to valid read hold time (does not apply if ALE is used)	5	-	ns
$T_{s, ALR}$	Address to latch setup time	10	-	ns
$T_{h, ALR}$	Address to latch hold time	10	-	ns
$T_{v,L}$	Valid latch pulse width	20	-	ns
$T_{s, LR}$	Latch to read setup	0	-	ns
$T_{h, LR}$	Latch to read hold (does only apply if ALE is used)	5	-	ns
$T_{p, RD}$	Valid read to valid data propagation delay		80	ns
$T_{z, RD}$	Valid read negated to output tristate		25	ns
$T_{z, INTH}$	Valid read negated to interrupt release/pull-down	-	100	ns



**Table 9: CPU Write Access**

<i>Symbol</i>	<i>Description</i>	<i>Min</i>	<i>Max</i>	<i>Unit</i>
$T_{S, AW}$	Address to valid write setup time	10	-	ns
$T_{S, DW}$	Data to valid write setup time	20	-	ns
$T_{S, ALW}$	Address to latch setup time	10	-	ns
$T_{H, ALW}$	Address to latch hold time	10	-	ns
$T_{V, L}$	Valid latch pulse width	20	-	ns
$T_{S, LW}$	Latch to write setup	0	-	
$T_{H, LW}$	Latch to write hold (does not apply if ALE is used)	5	-	ns
$T_{H, DW}$	Data to valid write hold time	5	-	ns
$T_{H, AW}$	Address to valid write hold time (does only apply if ALE is used)	5	-	ns
$T_{V, WR}$	Valid write pulse width	25	-	ns

## DC Characteristics

Table 3: PECL and TTL Inputs and Outputs

Parameters	Description	Min	Max	Units	Conditions
$V_{OH}$	Output HIGH voltage (TTL)	2.4	—	V	$I_{OH} = -2, -4, -8, -16$ mA
$V_{OL}$	Output LOW voltage (TTL)	—	0.5	V	$I_{OL} = 2, 4, 8, 16$ mA
$V_{IH}$	Input HIGH voltage (TTL)	2.0	5.5	V	—
$V_{IL}$	Input LOW voltage (TTL)	0	0.8	V	—
$I_{IT}$	Input current (TTL)	—	10	$\mu$ A	$0V < V_{IN} < 5V$
$V_{OCM}$	O/P Common Mode Range (PECL)	1600	2300	mV	At Min $\Delta V_{OUT}$
$\Delta V_{OUT75}$	Differential Output Voltage (PECL)	1000	1500	mV	$75\Omega$ to $V_{DD} - 2.0$ V
$\Delta V_{OUT50}$	Differential Output Voltage (PECL)	900	1350	mV	$50\Omega$ to $V_{DD} - 2.0$ V
$V_{ICM}$	I/P Common Mode Range (PECL)	1500	1800	mV	At Min $\Delta V_{IN}$
$\Delta V_{IN}$	Differential Input Voltage (PECL)	300	2600	mV	—
$I_{IP}$	Input current (PECL)	—	1000	$\mu$ A	$0V < V_{IN} < 3.3V$

## Power Dissipation

Table 4: Power Supply Currents

Parameter	Description	(Typ)	(Max)	Units
$I_{DD}$	Power supply current from $V_{DD}$	833	972	mA
$P_D$	Power dissipation	2.5	3.0	W

## Absolute Maximum Ratings(1)

Power Supply Voltage ( $V_{DD}$ ) Potential to GND .....	-0.5V to +4V
Power Supply Voltage ( $V_{DD5}$ ) Potential to GND .....	-0.5V to +6V
DC Input Voltage (PECL inputs) .....	-0.5V to $V_{DD} + 0.5V$
DC Input Voltage (TTL inputs) .....	-0.5V to $V_{DD5} + 0.5V$
DC Output Voltage (TTL Outputs) .....	-0.5V to $V_{DD} + 0.5V$
DC Output Voltage (TTL 5V Tolerant Outputs) .....	-0.5V to $V_{DD5} + 0.5V$
Output Current (TTL Outputs) .....	+/-50mA
Output Current (PECL Outputs) .....	+/-50mA
Case Temperature Under Bias .....	-55° to +125°C
Storage Temperature .....	-65°C to +150°C
Maximum Input ESD (Human Body Model) .....	2000 V

*Note: Caution: Stresses listed under "Absolute Maximum" may cause permanent damage. Functionality at or exceeding the values listed may affect device reliability.*

## Recommended Operating Conditions

Power Supply Voltage ( $V_{DD}$ ) .....	+3.3V±10 %
Power Supply Voltage ( $V_{DD5}$ ) .....	+5.0V±10 %
Operating Temperature Range* ( $T$ ) .....	-40° to 85°C

\* Lower limit of specification is ambient temperature and upper

## Notice

This document contains information on products that are in the preproduction phase of development. The information contained in this document is based on test results and initial product characterization. Characteristic data and other specifications are subject to change without notice. Therefore, the reader is cautioned to confirm that this datasheet is current prior to placing orders.

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