21044
4M (1,048,576 x 4) BIT DYNAMIC RAM WITH FAST PAGE MODE

- **Performance Range**

Symbol	Parameter	21044-07	21044-08	Units
t_{RAC}	Access Time from $\overline{RAS}$	70	80	ns
t_{CAC}	Access Time from $\overline{CAS}$	20	25	ns
t_{RC}	Read Cycle Time	130	150	ns

- **Fast Page Mode Operation**
- **Common I/O Using "Early Write" Operation**
- **1024 cycles/16 ms Refresh**
- **$\overline{CAS}$-before-$\overline{RAS}$ refresh, $\overline{RAS}$-only Refresh, Hidden Refresh and Test Mode Capability**
- **Single 5V ± 10% Power Supply**
- **Available in Plastic SOJ (T) package**

Intel's 21044 is a CMOS high speed 1,048,576 x 4-bit dynamic RAM optimized for high performance applications such as mainframes, graphics and microprocessor systems.

21044 features Fast Page Mode operation which allow high speed random access of memory cells within the same row.

$\overline{CAS}$-before-$\overline{RAS}$ refresh capability provides on-chip auto refresh as an alternative to $\overline{RAS}$-only refresh. All Inputs, Output and clocks are fully CMOS and TTL compatible.

Multiplexed address inputs permit the 21044 device to be packaged in a standard 20-/26-pin plastic SOJ.

T21044 Plastic SOJ

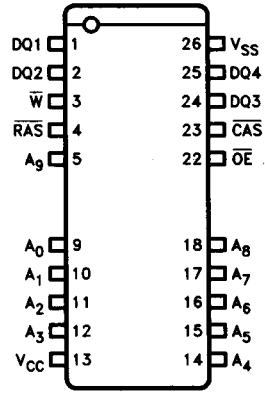

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FIGURE 1. Pin Configuration

Pin Name	Pin Function
A_0–A_9	Address Inputs
DQ1–4	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{OE}$	Data Output Enable
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
V_{CC}	Power (+5V)
V_{SS}	Ground

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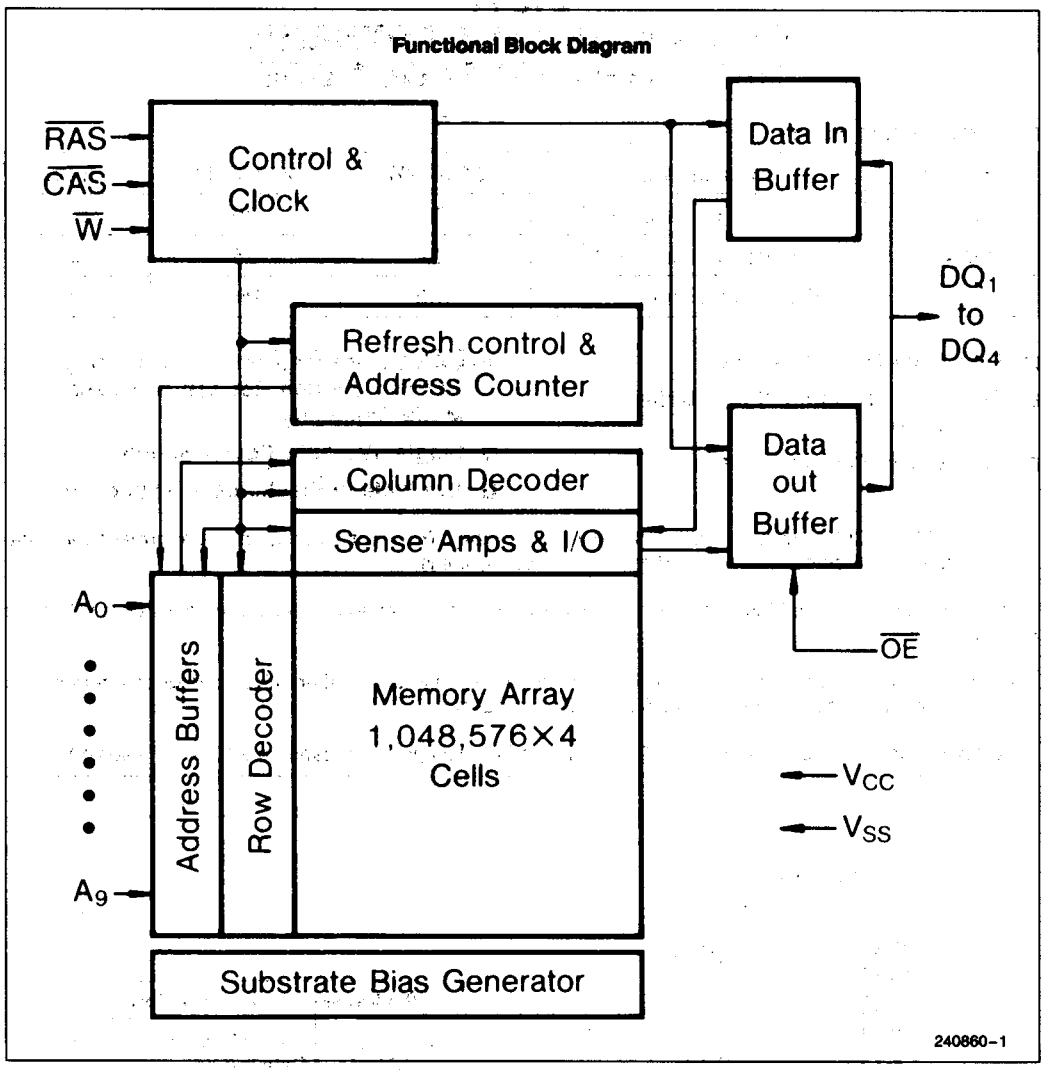
Order Number: 240860-004

Functional Block Diagram



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to V_{SS}	−1 to +7.0	V
V_{CC}	Voltage on Power Supply Relative to V_{SS}	−1 to +7.0	V
T_{stg}	Storage Temperature	−55 to +125	°C
T_{opr}	Operating Temperature	0 to 70	°C
P_d	Power Dissipation	1.0	W
I_{os}	Short Circuit Output Current	50	mA

*Permanent damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded. Functional Operation should be restricted to the conditions as defined in the operational sections of the Data Sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(Voltage referenced to V_{SS}. T_a = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	Units
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 1	V
V_{IL}	Input Low Voltage	−1.0	—	0.8	V

CAPACITANCE (T_a = 25°C)

Symbol	Parameter	Min	Max	Units
C_{in1}	Input Capacitance (A0 - A10)		6	pF
C_{in2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$)		7	pF
C_{out}	Output Capacitance (D_{in}/D_{out})		7	pF

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DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions unless otherwise noted)

Symbol	Parameter	Speed	Min	Max	Units
I_{CC1}	Operating Current ($\overline{RAS}$ and $\overline{CAS}$ cycling @ ^tRC = min)	−07 −08	— —	105 95	mA
I_{CC2}	Standby Current (TTL Power Supply Current)		—	2	mA
I_{CC3}	$\overline{RAS}$ Only Refresh Current ($\overline{CAS}$ = V_{IH}, $\overline{RAS}$ Cycling @ ^tRC = min)	−07 −08	— —	105 95	mA
I_{CC4}	Fast Page Mode Current ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$ Cycling @ ^tPC = min)	−07 −08	— —	100 90	mA
I_{CC5}	Standby Current (CMOS Power Supply Current)		—	1	mA
I_{CC6}	$\overline{CAS}$-before-$\overline{RAS}$ Refresh Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling @ ^tRC = min)	−07 −08	— —	105 95	mA
I_{CC7}	Standby Current ($\overline{RAS}$ = V_{IH}, $\overline{CAS}$ = V_{IL}, D_{OUT} = Enable)		—	5	mA
I_{IL}	Input Leakage Current (Any Input 0 < V_{in} < 6.5 Volts all other Pins = 0 Volts)		−10	10	μA
I_{OL}	Output Leakage Current (Data out is disabled and 0 < V_{out} < 5.5 V)		−10	10	μA
V_{OH}	Output High Voltage Level (I_{OH} = −5mA)		2.4	—	V
V_{OL}	Output Low Voltage Level (I_{OL} = 4.2 mA)		—	0.4	V

NOTE:

I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} are dependant on output loading and cycle rates. Specified values are obtained with the output open. I_{CC} is specified as average current.

AC CHARACTERISTICS (See Notes 1, 2)

(T_A = 0°C to 70°, V_{CC} = 5V ±10%)

Symbol	Parameter	21044-07		21044-08		Units	Notes
		Min	Max	Min	Max		
t_{REF}	Time between Refresh		16		16	ms	
t_{RC}	Random R/W Cycle Time	130		150		ns	
t_{RWC}	RMW Cycle Time	185		210		ns	
t_{RAC}	Access Time From $\overline{RAS}$		70		80	ns	3, 4, 10
t_{CAC}	Access Time From $\overline{CAS}$		20		25	ns	3, 4, 5
t_{AA}	Access Time From Column Address		35		40	ns	3, 10
t_{CLZ}	$\overline{CAS}$ to Output in low Z	5		5		ns	3
t_{OFF}	Output Buffer Turn-Off Delay Time	0	15	0	15	ns	6
t_T	Transition Time	3	50	3	50	ns	2
t_{RP}	$\overline{RAS}$ Precharge Time	50		60		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	70	10K	80	10K	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	20		25		ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	10		10		ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	20	55	ns	4
t_{CAS}	$\overline{CAS}$ Pulse Width	20	10K	25	10K	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	70		80		ns	
t_{CPN}	$\overline{CAS}$ Precharge Time	10		10		ns	
t_{ASR}	Row Address Set-up Time	0		0		ns	
t_{RAH}	Row Address Hold Time	10		10		ns	
t_{ASC}	Column Address Set-up Time	0		0		ns	
t_{CAH}	Column Address Hold Time	15		15		ns	
t_{AR}	Column Address Time referenced to $\overline{RAS}$	55		60		ns	
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	ns	10
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	35		40		ns	11
t_{RCS}	Read Command Set-up Time	0		0		ns	
t_{RRH}	Read Command Hold Time referenced to $\overline{RAS}$	0		0		ns	8
t_{RCH}	Read Command Hold Time referenced in $\overline{CAS}$	0		0		ns	8
t_{WCS}	Write Command Set-up Time	0		0		ns	7
t_{WCH}	Write Command Hold Time	15		15		ns	
t_{WCR}	Write Command Hold referenced to $\overline{RAS}$	55		60		ns	11
t_{WP}	Write Command Pulse Width	15		15		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		25		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		25		ns	
t_{DS}	Data Set-up Time	0		0		ns	9
t_{DH}	Data Hold Time	15		15		ns	9

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AC CHARACTERISTICS (See Notes 1, 2) (Continued)

(T_A = 0°C to 70°, V_{CC} = 5V ±10%)

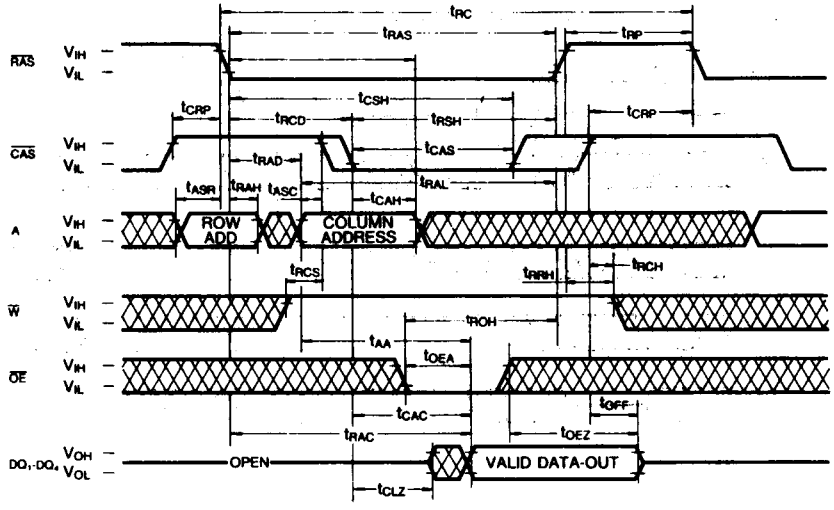
Symbol	Parameter	21044-07		21044-08		Units	Notes
		Min	Max	Min	Max		
t_{DHR}	Data-In Hold Time referenced to $\overline{RAS}$	55		60		ns	11
t_{RWD}	$\overline{RAS}$ to WRITE Delay Time	100		110		ns	7
t_{CWD}	$\overline{CAS}$ to WRITE Delay Time	50		55		ns	7
t_{AWD}	Column Address to WRITE Delay Time	65		70		ns	7
t_{RPC}	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time	10		10		ns	
t_{CSR}	$\overline{CAS}$ Set-up Time for $\overline{CAS}$ before $\overline{RAS}$ refresh	10		10		ns	
t_{CHR}	$\overline{CAS}$ Hold Time for $\overline{CAS}$ before $\overline{RAS}$ refresh	20		30		ns	
t_{CPT}	$\overline{CAS}$ Precharge Time (Refresh Counter Test)	40		40		ns	
t_{WTS}	Write Command Set-up Time (Test Mode in)	10		10		ns	
t_{WTH}	Write Command Hold Time (Test Mode in)	10		10		ns	
t_{WRP}	WRITE to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
t_{WRH}	WRITE to $\overline{RAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10		10		ns	
t_{PC}	Fast Page Mode Cycle Time	50		55		ns	
t_{PRWC}	Fast Page Mode RMW Cycle Time	105		120		ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge		40		45	ns	3
t_{CP}	Fast Page Mode $\overline{CAS}$ Precharge Time	10		10		ns	
t_{RASP}	$\overline{RAS}$ Pulse Width (Fast Page Mode)	70	100K	80	100K	ns	
t_{RHCP}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	45		45			
t_{ROH}	$\overline{RAS}$ Hold Time Referenced to $\overline{OE}$	20		20			
t_{OEA}	$\overline{OE}$ Accesss Time		20		20		
t_{OED}	$\overline{OE}$ to Data Delay	20		20			
t_{OEZ}	Output Buffer Turn Off Delay Time from $\overline{OE}$	0	20	0	20		
t_{OEH}	$\overline{OE}$ Command Hold Time	20		20			

NOTES:

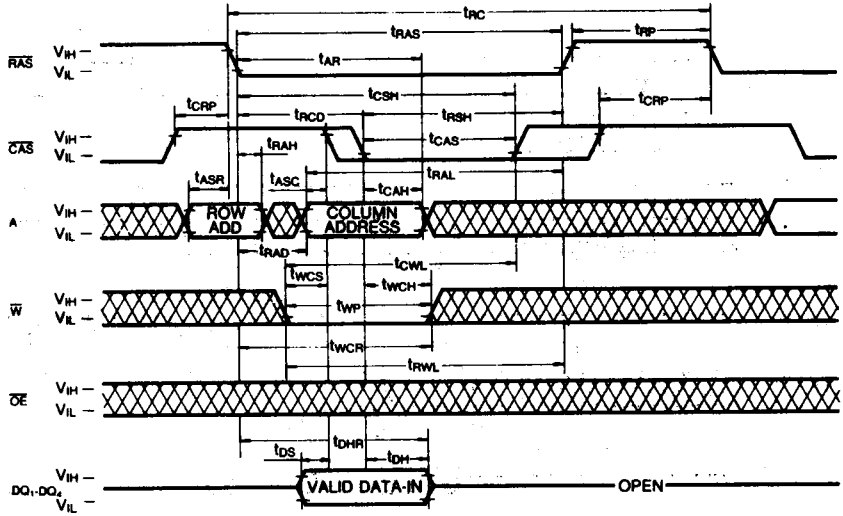
1. An initial pause of 200 Microseconds is required after power-up followed by an 8 $\overline{RAS}$-only cycles before proper device operation is achieved.
2. V_{ih} (min) and V_{il} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{ih} (min) and V_{il} (max) and are assumed to be 5 ns for all inputs.
3. Measured with a load equivalent to two 2 TTL loads and 100 pF.
4. Operation within the t_{RCD} (max) limit insures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC}.
5. Assumes that $t_{RCD} \geq t_{RCD}$ (max).
6. This parameter defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
7. t_{WCS}, t_{WD}, t_{RWD}, and t_{AWD} are non restrictive operating parameters. They are included in the Data Sheet as Electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and data out pin will remain open circuit through the entire cycle; If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min) and $t_{AWD} \geq t_{AWD}$ (min), the cycle is a read-write cycle and data out will contain data read from the selected cell; If neither of the above set of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
8. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
9. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to the W leading edge in read-write cycles.
10. Operation within the t_{RAD} (max) limit insures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled by t_{AA}.
11. t_{AR}, t_{WCR}, t_{DHR} are referenced to t_{RAD} (max).

TIMING DIAGRAMS

READ CYCLE



WRITE CYCLE (EARLY WRITE)



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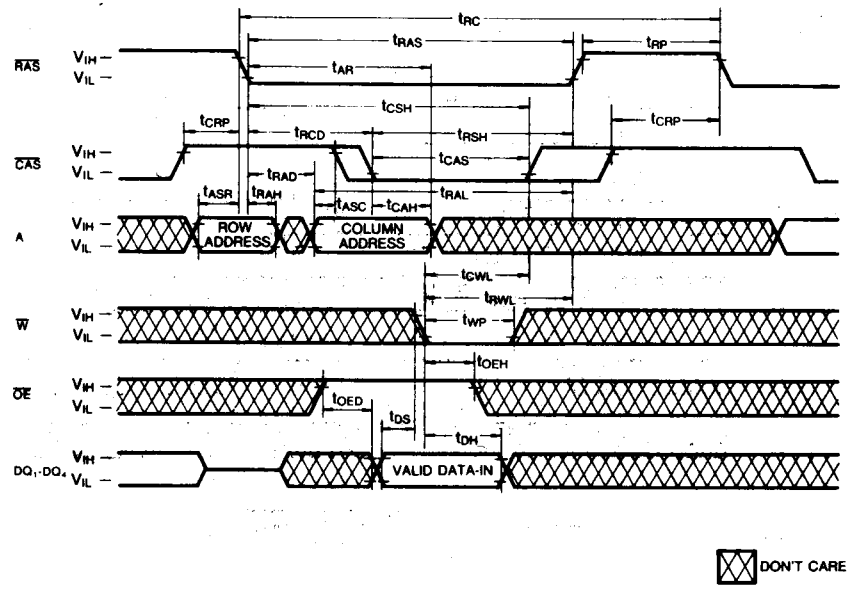
WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



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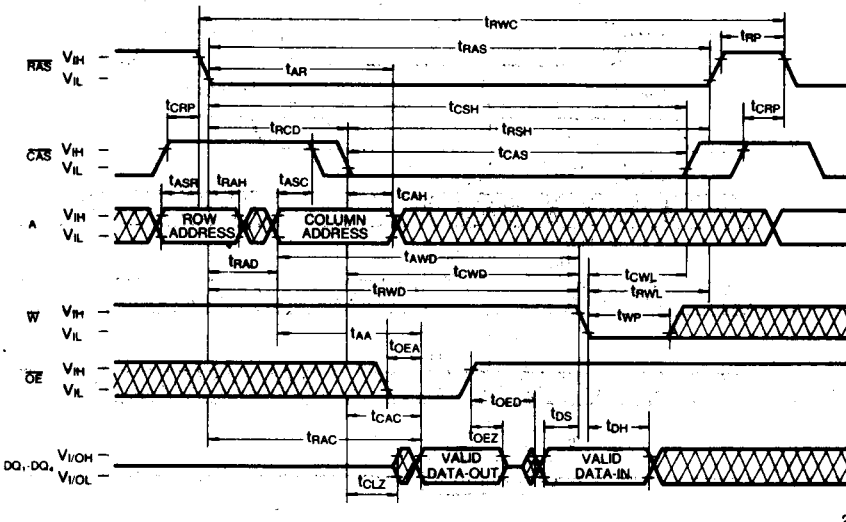
READ-MODIFY-WRITE CYCLE



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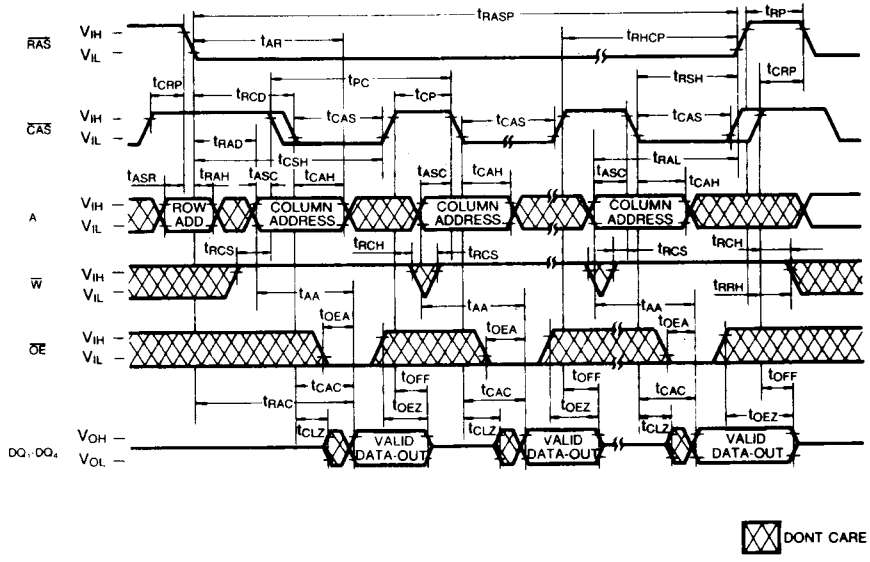
FAST PAGE MODE READ CYCLE



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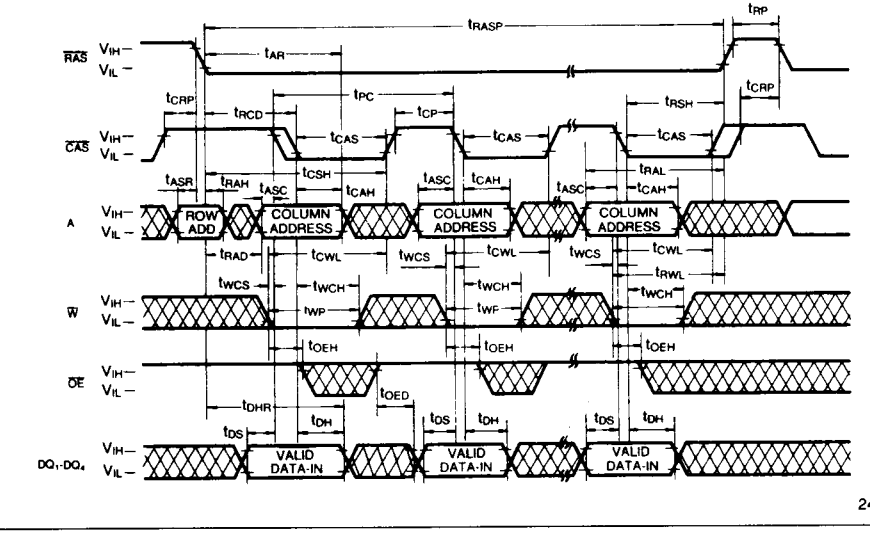
FAST PAGE MODE WRITE CYCLE



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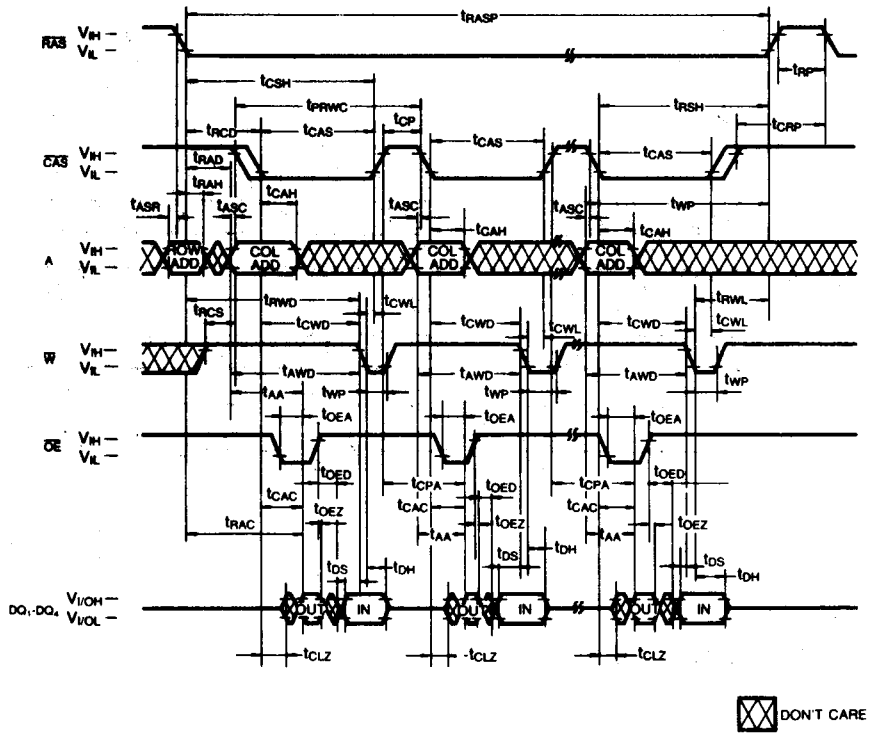
FAST PAGE MODE READ-MODIFY-WRITE



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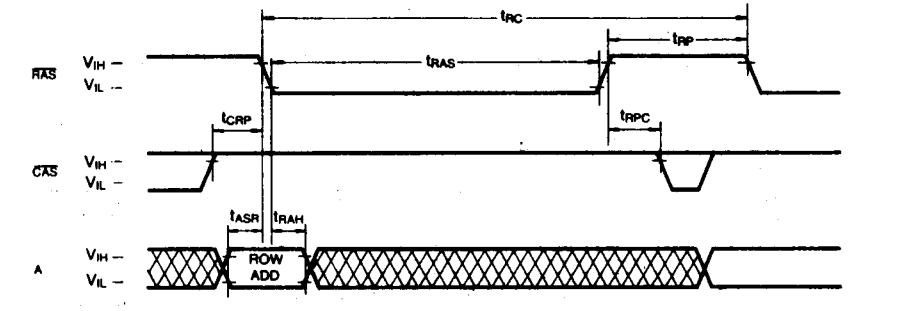
RAS-ONLY REFRESH CYCLE



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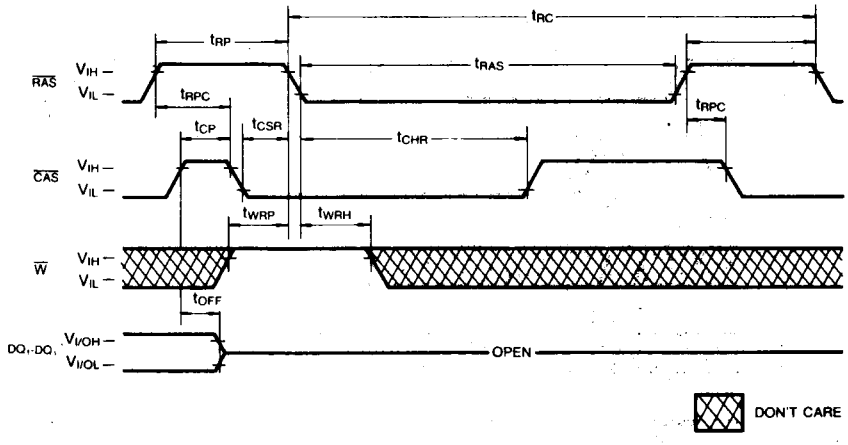
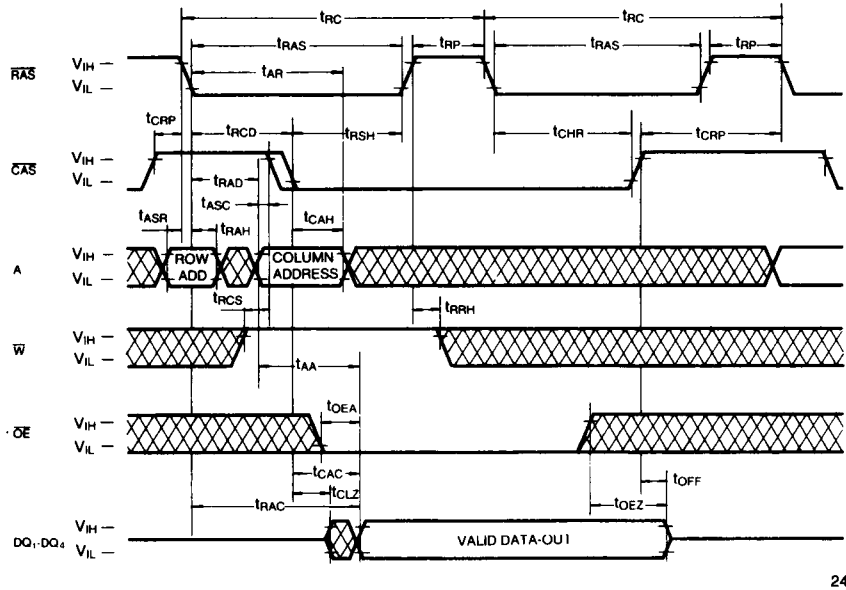
NOTE:
$\overline{W}$, $\overline{OE}$ = Don't care

CAS-BEFORE-RAS REFRESH CYCLE

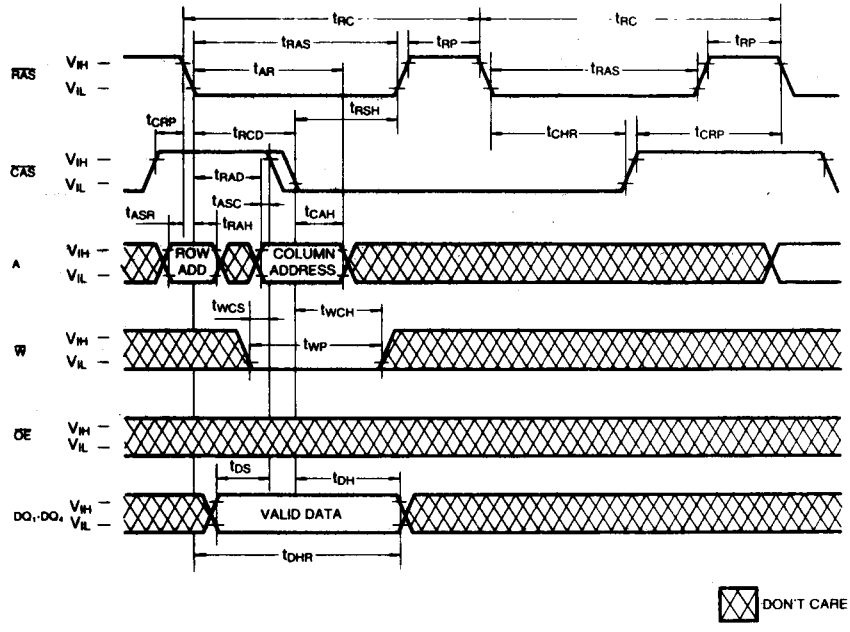


NOTE:
W, OE, A = Don't care

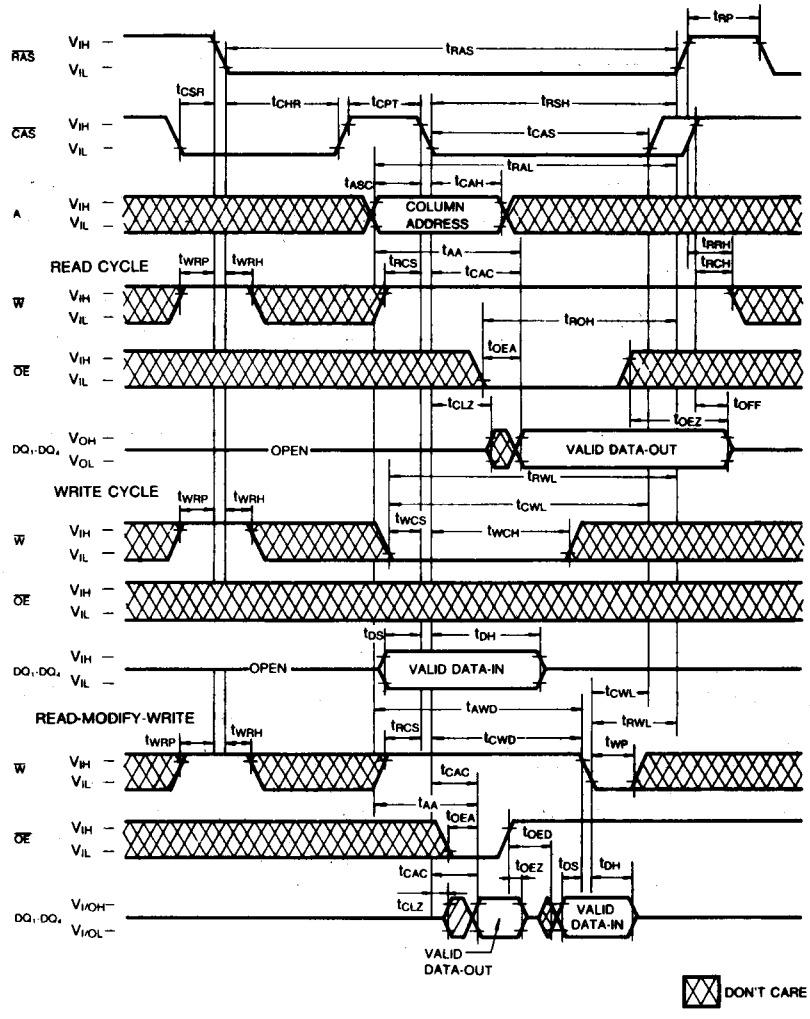
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)



CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE



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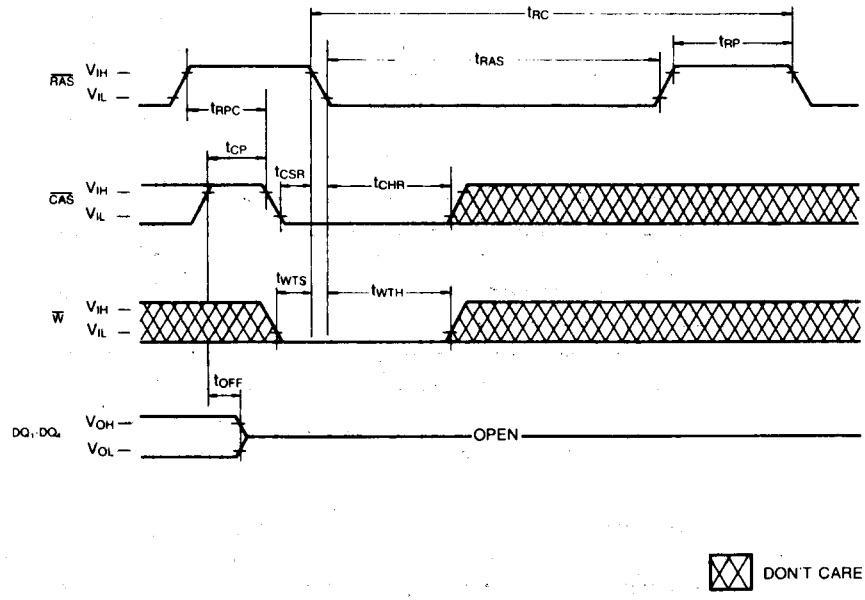
TEST MODE IN CYCLE



NOTE:
$\overline{OE}$, A = Don't care

240860-16

TEST MODE DESCRIPTION

The 21044 is the RAM organized 1,048,576 words by 4 bits, it is internally organized 524,288 words by 8 bits. In "Test Mode", data are written into 8 sectors in parallel and retrieved the same way. Column address bit A0 is not used. If, upon reading, two bits on one I/O pin are equal (all "1"s or "0"s), the I/O pin indicates a "1". If they were not equal, the I/O pin would indicate a "0". In "Test Mode", the 1M x 4 DRAM can be tested as if it were a 512K x 4 DRAM.

"$\overline{WRITE}$, $\overline{CAS}$-Before-$\overline{RAS}$ Cycle (Test Mode in Cycle) puts the device into "Test Mode". And "$\overline{CAS}$-Before-$\overline{RAS}$ Refresh Cycle" or "$\overline{RAS}$ Only Refresh Cycle" puts it back into "Normal Mode". The "Test Mode" function reduces test times (½ in case of N test pattern).

DEVICE OPERATION

The 21044 contains 4,194,304 memory locations. Twenty address bits are required to address a particular memory location. Since the 21044 has only 10 address input pins, time multiplexed addressing is used to input 10 row and 10 column addresses. The multiplexing is controlled by the timing relationship between the row address strobe ($\overline{RAS}$), the column address strobe ($\overline{CAS}$) and the valid address inputs.

Operation of the 21044 begins by strobing in a valid row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. Then the address on the 10 address input pins is changed from a row address to a column address and is strobed in by $\overline{CAS}$. This is the beginning of any 21044 cycle in which a memory location is accessed. The specific type of cycle is determined by the state of the write enable pin and various timing relationships. The cycle is terminated when both $\overline{RAS}$ and $\overline{CAS}$ have returned to the high state. Another cycle can be initiated after $\overline{RAS}$ remains high long enough to satisfy the $\overline{RAS}$ precharge time (t_{RP}) requirement.

$\overline{RAS}$ and $\overline{CAS}$ Timing

The minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths are specified by t_{RAS}(min) and t_{CAS}(min) respectively. These minimum pulse widths must be satisfied for proper device operation and data integrity. Once a cycle is initiated by bringing $\overline{RAS}$ low, it must not be aborted prior to satisfying the minimum $\overline{RAS}$ and $\overline{CAS}$ pulse widths. In addition, a new cycle must not begin until the minimum $\overline{RAS}$ precharge time, t_{RP}, has been satisfied. Once a cycle begins, internal clocks and other circuits within the 21044 begin a complex sequence of events. If the sequence is broken by violating minimum timing requirements, loss of data integrity can occur.

Read

A read cycle is achieved by maintaining the write enable input ($\overline{W}$) high during a $\overline{RAS}$/$\overline{CAS}$ cycle. The output of the 21044 remains in the Hi-Z state until valid data appears at the output. If $\overline{CAS}$ goes low before t_{RCD}(max), the access time to valid data is specified by t_{RAC}. If $\overline{CAS}$ goes low after t_{RCD}(max), the access time is measured from $\overline{CAS}$ and is specified by t_{CAC}. In order to achieve the minimum access time, t_{RAC}(min), it is necessary to bring $\overline{CAS}$ low before t_{RCD}(max).

Write

The 21044 can perform early write, late write and read-modify-write cycles. The difference between these cycles is in the state of data-out and is determined by the timing relationship between $\overline{W}$ and $\overline{CAS}$. In any type of write cycle, data-in must be valid at or before the falling edge of $\overline{W}$ or $\overline{CAS}$, whichever is later.

Early Write: An early write cycle is performed by bringing W low before $\overline{CAS}$. The data at the data input pin (D) is written into the addressed memory cell. Throughout the early write cycle the output remains in the Hi-Z state. This cycle is good for common I/O applications because the data-in and data-out pins may be tied together without bus contention.

Read-Modify-Write: In this cycle, valid data from the addressed cell appears at the output before and during the time that data is being written into the same cell location. This cycle is achieved by bringing $\overline{W}$ low after $\overline{CAS}$ and meeting the data sheet read-modify-write cycle timing requirements. This cycle requires using a separate I/O to avoid bus contention.

Late Write: If $\overline{W}$ is brought low after $\overline{CAS}$, a late write cycle will occur. The late write cycle is very similar to the read-modify-write cycle except that the timing parameters, t_{RWD} and t_{CWD}, are not necessarily met. The state of data-out is indeterminate since the output could be either Hi-Z or contain data depending on the timing conditions. This cycle requires a separate I/O to avoid bus contention.

Data Output

The 21044 has a tri-state output buffer which is controlled by $\overline{CAS}$ (and $\overline{W}$ for early write). Whenever $\overline{CAS}$ is high (V_{IH}) the output is in the high impedance (Hi-Z) state. In any cycle in which valid data appears at the output, the output first remains in the Hi-Z state until the data is valid and then the valid data appears at the output. The valid data remains at the output until $\overline{CAS}$ returns high. This is true even if a new $\overline{RAS}$ cycle occurs (as in hidden refresh). Each of the 21044 operating cycles is listed below after the corresponding output state produced by the cycle.

Valid Output Data: Read, Read-Modify-Write, Hidden Refresh, Page Mode Read, Page Mode Read-Modify-Write.

HI-Z Output State: Early Write, $\overline{RAS}$-only Refresh, Page Mode Write, $\overline{CAS}$-before-$\overline{RAS}$ Refresh, $\overline{CAS}$-only cycle.

Indeterminate Output State: Delayed Write

Refresh

The data in the 21044 is stored on a tiny capacitor within each memory cell. Due to leakage, the data will leak off after a period of time. To maintain data integrity it is necessary to refresh each of the rows every 16 ms. There are several ways to accomplish this.

$\overline{RAS}$-Only Refresh: This is the most common method for performing refresh. It is performed by strobing in a row address with $\overline{RAS}$ while $\overline{CAS}$ remains high. The cycle must be repeated for each row.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh: The 21044 has $\overline{CAS}$-before-$\overline{RAS}$ on-chip refreshing capability that eliminates the need for external refresh addresses. If $\overline{CAS}$ is held low for the specified setup time (t_{CSR}) before $\overline{RAS}$ goes low, the on-chip refresh circuitry is enabled. An internal refresh operation automatically occurs and the on-chip refresh address counter is internally incremented in preparation for the next $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

Hidden Refresh: A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the $\overline{CAS}$ active time and cycling $\overline{RAS}$. The 21044 hidden refresh cycle is actually a $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle within an extended read cycle. The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required in hidden refresh cycles by DRAMs that do not have $\overline{CAS}$-before-$\overline{RAS}$ refresh capability.

Other Refresh Methods: It is also possible to refresh the 21044 by using read, write or read-modify-write cycles. Whenever a row is accessed, all the cells in that row are automatically refreshed. There are certain applications in which it might be advantageous to perform refresh in this manner but in general $\overline{RAS}$-only or $\overline{CAS}$-before-$\overline{RAS}$ refresh is the preferred method.

Fast Page Mode

The 21044 has fast page mode capability. Fast page mode memory cycles provide faster access and lower power dissipation than normal memory cycles. In fast page mode, it is possible to perform read, write or read-modify-cycles. As long as the applicable timing requirements are observed, it is possible to mix these cycles in any order. A fast page mode cycle begins with a normal cycle. While $\overline{RAS}$ is kept low to maintain the row address, $\overline{CAS}$ is cycled to strobe in additional column addresses. This eliminates the time required to set up and strobe sequential row addresses for the same page.

$\overline{CAS}$-before-$\overline{RAS}$ Refresh Counter Test Cycle

A special timing sequence using the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle provides a convenient method of verifying the functionality of the $\overline{CAS}$-before-$\overline{RAS}$ refresh activated circuitry.

After the $\overline{CAS}$-before-$\overline{RAS}$ refresh operation, if $\overline{CAS}$ goes high and then low again while $\overline{RAS}$ is held low, the read and write operations are enabled.

This is shown in the $\overline{CAS}$-before-$\overline{RAS}$ counter test cycle timing diagram. A memory cell can be addressed with 10 row address bits and 10 column address bits defined as follows:

Row Address—Bits A0 through A9 are supplied by the on-chip refresh counter.

Column Address—Bits A0 through A9 are strobed-in by the falling edge of $\overline{CAS}$ as in a normal memory cycle.

Suggested $\overline{CAS}$-before-$\overline{RAS}$ Counter Test Procedure

The $\overline{CAS}$-before-$\overline{RAS}$ refresh counter test cycle timing is used in each of the following steps:

1. Initialize the internal refresh counter by performing 8 cycles.
2. Write a test pattern of "lows" into the memory cells at a single column address and 1024 row addresses. (The row addresses are supplied by the on-chip refresh counter.)
3. Using read-modify-write cycles, read the "lows" written during step 2 and write "highs" into the same memory locations. Perform this step 1024 times so that highs are written into the 1024 memory cells.
4. Read the "highs" written during step 3.
5. Complement the test pattern and repeat steps 2, 3 and 4.

Power-Up

If $\overline{RAS}$ = V_{SS} during power-up, the 21044 could begin an active cycle. This condition results in higher than necessary current demands from the power supply during power-up. It is recommended that $\overline{RAS}$ and $\overline{CAS}$ track with V_{CC} during power-up or be held at a valid V_{IH} in order to minimize the power-up current.

An initial pause of 200 μs is required after power-up followed by 8 initialization cycles before proper device operation is assured. 8 initialization cycles

are also required after any 16 ms period in which there are no $\overline{RAS}$ cycles. An initialization cycle is any cycle in which $\overline{RAS}$ is cycled.

Termination

The lines from the TTL driver circuits to the 21044 inputs act like unterminated transmission lines resulting in significant positive and negative overshoots at the inputs. To minimize overshoot it is advisable to terminate the input lines and to keep them as short as possible. Although either series or parallel termination may be used, series termination is generally recommended since it is simple and draws no additional power. It consists of a resistor in series with the input line placed close to the 21044 input pin. The optimum value depends on the board layout. It must be determined experimentally and is usually in the range of 20Ω to 40Ω.

Board Layout

It is important to lay out the power and ground lines on memory boards in such a way that switching transient effects are minimized. The recommended methods are gridded power and ground lines or separate power and ground planes. The power and ground lines act like transmission lines to the high frequency transients generated by DRAMs. The impedance is minimized if all the power supply traces to all DRAMs run both horizontally and vertically and are connected at each intersection or better yet if power and ground planes are used.

Address and control lines should be as short as possible to avoid skew. In boards with many DRAMs these lines should fan out from a central point like a fork or comb rather than being connected in a serpentine pattern. Also the control logic should be centrally located on large memory boards to facilitate the shortest possible address and control lines to all the DRAMs.

Decoupling

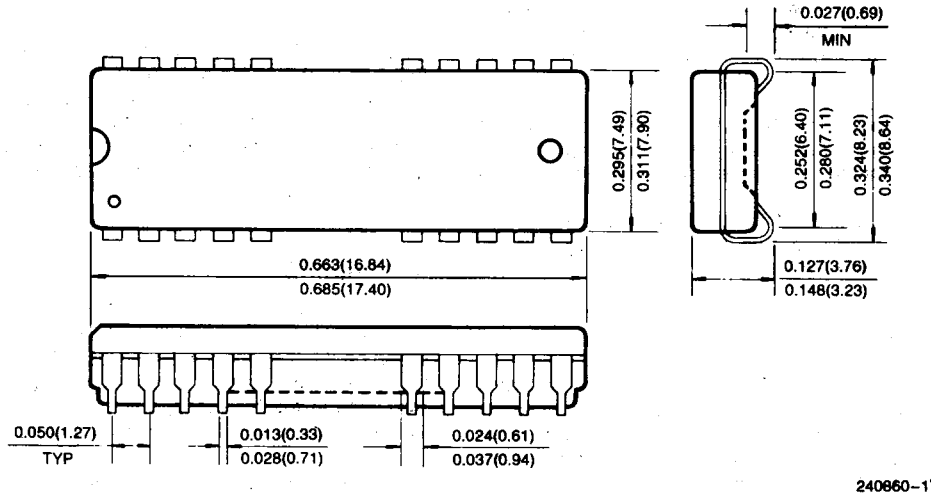
The importance of proper decoupling cannot be over emphasized. Excessive transient noise or voltage droop on the V_{CC} line can cause loss of data integrity (soft errors). The total combined voltage changes over time in the V_{CC} to V_{SS} voltage (measured at the device pins) should not exceed 500 mV.

A high frequency 0.3 μF ceramic decoupling capacitor should be connected between the V_{CC} and ground pins of each 21044 using the shortest possible traces. These capacitors act as a low impedance shunt for the high frequency switching transients generated by the 21044 and they supply much of the current used by the 21044 during cycling.

In addition, a large tantalum capacitor with a value of 47 μF to 100 μF should be used for bulk decoupling to recharge the 0.3 μF capacitors between cycles, thereby reducing power line droop. The bulk decoupling capacitor should be placed near the point where the power traces meet the power grid or power plane. Even better results may be achieved by distributing more than one tantalum capacitor throughout the memory array.

PACKAGE DIMENSIONS

20-LEAD PLASTIC SMALL OUTLINE J-LEAD (T)



REVISION SUMMARY

The following list represents the key differences between version -003 and -004 of the 21044 4M (1,048,576 x 4) bit Dynamic RAM with Fast Page Mode.

1. Updated AC characteristics