CMOS 32-BIT HIGH-SPEED MICROPROCESSOR SLICE

KEY FEATURES

- **Eight CMOS 2901 Type Devices in a Single Package**
- **32 x 32 Dual Port RAM**
- **Low CMOS Power**
  — 350 mW
- **High Speed Operation**
  — 23 MHz Read-Modify-Write Cycle
- **Fully Firmware Compatible with the 2901**
- **On Board Carry Look-Ahead**

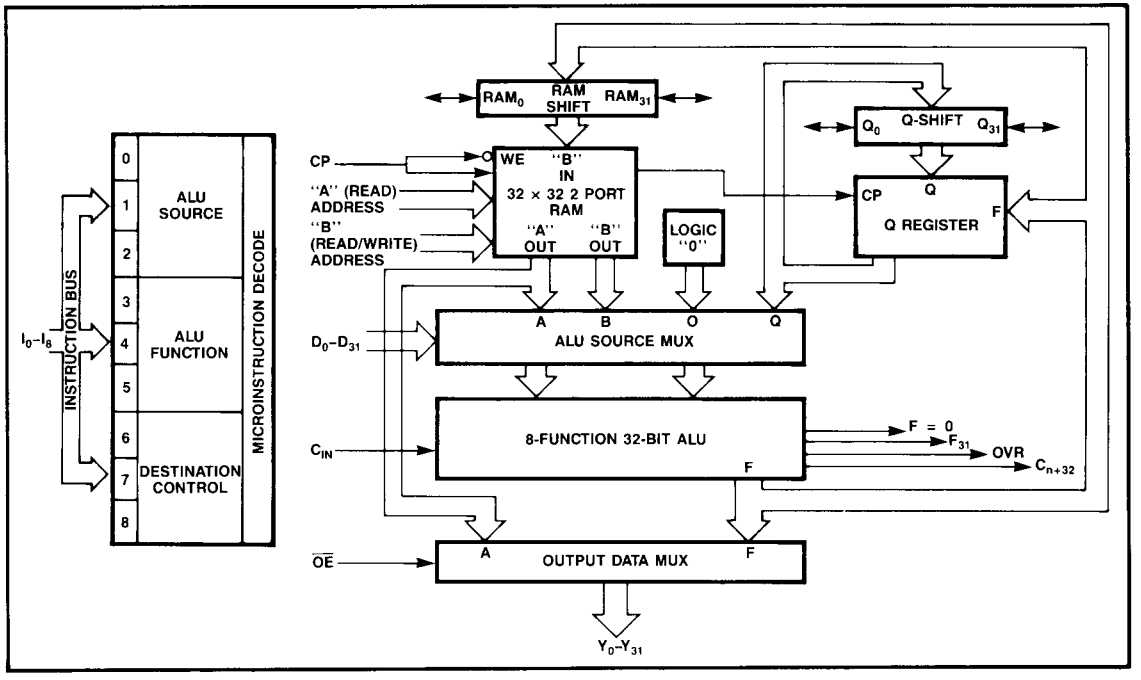
GENERAL DESCRIPTION

The WS59032 is a 32-bit High-Speed microprocessor which combines the functions of eight 2901 4-bit slice processors and distributed look-ahead carry generation on a single High Performance CMOS device. The WS59032 dual port RAM is 32-bits wide and 32 words deep. This architecture provides greater flexibility and eases the task of generating new microcode while maintaining 100% compatible with existing 2901 based microcode.

This microprogrammable circuit has the flexibility to efficiently emulate almost any digital computing machine. It is an ideal candidate for such applications as peripheral controllers, CPUs, programmable microprocessors, and Digital Signal Processors.

The advanced CMOS process, with which the WS59032 is manufactured, provides significant performance improvements over an equivalent Bipolar device configuration. While operating faster than a 2901C based system, the WS59032 requires less than 3% of the power consumed by an equivalent Bipolar system.

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Signal Name	I/O	Description
A0-4	I	Addresses which select the word of on board RAM which is to be displayed through the A port.
B0-4	I	Addresses which select the word of on board RAM which is to be displayed through the B port and into which data is written when the clock is low.
I0-8	I	Block of three instruction groups which are to select 1) which data sources will be applied to the ALU (I012), 2) what function the ALU will perform (I345), and 3) what data is to be written into the Q register or on board RAM(I678).
Q31, RAM31	I/O	Signal paths at the MSB of the on-board RAM and the Q-register which are used for shifting data. When the destination code on I678 indicates an up shift (Octal 6 or 7) the three state outputs are enabled and the MSB of the ALU output is available on the RAM 31 pin and the MSB of the Q-register is available on the Q 31 pin. Otherwise, the pins appear as inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of RAM (octal 4 and 5) and the Q register (octal 4).
Q0, RAM0	I/O	Shift lines similar to Q31 and RAM31, however the description is applied to the LSB of RAM and the Q-register.
D0-D31	I	These thirty two direct data inputs can be selected as a data source for the ALU. D0 is the LSB.
Y0-Y31	O	These thirty two three state outputs, when enabled, display either the data on the A-port of the register stack or the outputs of the ALU as determined by the destination code I678.
$\overline{OE}$	I	When high, the Y outputs are in the high impedance state. When low, either the contents of the A-register or the outputs of the ALU are displayed on Y0-Y31, as determined by I678.
OVR	O	This signal indicates that an overflow into the sign bit has occurred as a result of a two's complement operation.
F=0	O	This output, when high, indicates the result of an ALU operation is zero.
F31	O	The most significant ALU output bit.
Cn	I	The carry-in to the ALU.
Cn+32	O	The carry-out of the ALU.
CP	I	This clock signal is applied to the A and B-port latches, RAM, and Q-register. The clock low time is the write enable to the on-board dual port RAM, including set-up time for the A and B-port registers. The A and B-port outputs change while the clock is high. The Q-register is latched on the clock low-to-high transition.

PIN DESIGNATOR

PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #	PIN NAME	PGA GRID #
VCC	N1	B3	N2	D23	B1	Y7	K12
VCC	A1	B4	M3	D24	B2	Y8	K13
GND	N7	D0	N6	D25	B3	Y9	J12
GND	G13	D1	M6	D26	A2	Y10	J13
GND	A12	D2	L6	D27	A3	Y11	H11
GND	C6	D3	N5	D28	B4	Y12	H12
RAM0	M7	D4	M5	D29	A4	Y13	H13
RAM31	B6	D5	N4	D30	B5	Y14	G12
Q0	L7	D6	M4	D31	A5	Y15	G11
Q31	A6	D7	N3	I0	N8	Y16	F13
CLK	A7	D8	H3	I1	M8	Y17	F12
CIN	N13	D9	H2	I2	L8	Y18	F11
CN+32	A9	D10	H1	I3	N9	Y19	E13
OVR	C8	D11	G1	I4	M9	Y20	E12
F=0	C13	D12	G3	I5	N10	Y21	D13
F31	B8	D13	G2	I6	A8	Y22	D12
OEN	M12	D14	F1	I7	B7	Y23	B13
A0	J1	D15	F2	I8	C7	Y24	C12
A1	J2	D16	F3	Y0	M10	Y25	A13
A2	K1	D17	E1	Y1	N11	Y26	B12
A3	K2	D18	E2	Y2	N12	Y27	B11
A4	L1	D19	D1	Y3	M11	Y28	A11
B0	M1	D20	D2	Y4	M13	Y29	B10
B1	L2	D21	C1	Y5	L12	Y30	A10
B2	M2	D22	C2	Y6	L13	Y31	B9

ABSOLUTE MAXIMUM RATINGS*

Operating Temp (Comm'l) ..... 0°C to +70°C
(Mil) ..... −55°C to +125°C
Storage Temp. (No bias) ... −65°C to +150°C
Voltage on any pin with
respect to GND ..... −0.6V to +7V
Latch Up Protection ..... >200 mA
ESD Protection ..... > ±2000V

*Notice: Stresses above those listed here may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

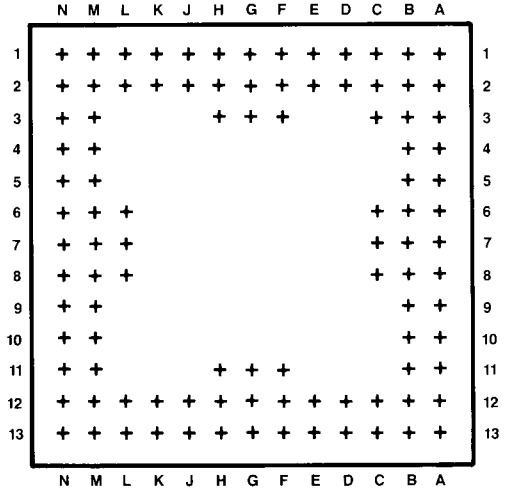
DC CHARACTERISTICS Over Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	TEST CONDITIONS			MIN	MAX	UNITS
V_{oh}	Output High Voltage	V_{CC} = Min. V_{in} = V_{ih} or V_{il}	All outputs	I_{oh} = −1.6mA	2.4		V
V_{ol}	Output Low Voltage	V_{CC} = Min V_{in} = V_{ih} or V_{il}	Y0-Y31	I_{ol} = 12mA Com'l		0.5	V
				I_{ol} = 9mA Mil			
			All others	I_{ol} = 8mA			
V_{ih}	Input High Voltage	Guaranteed Input High Voltage			2.0		
V_{il}	Input Low Voltage	Guaranteed Input Low Voltage				0.8	
I_{ix}	Input Load Current	V_{CC} = Max, V_{in} = Gnd or V_{CC}			−10	10	µA
I_{oz}	High Impedance Output Current	V_{CC} = Max, V_O = Gnd or V_{CC}			−50	50	µA
I_{CC}	Power Supply Current	V_{CC} = Max	Comm'l (0°C to +70°C)			70	mA
			Mil (−55°C to +125°C)			85	

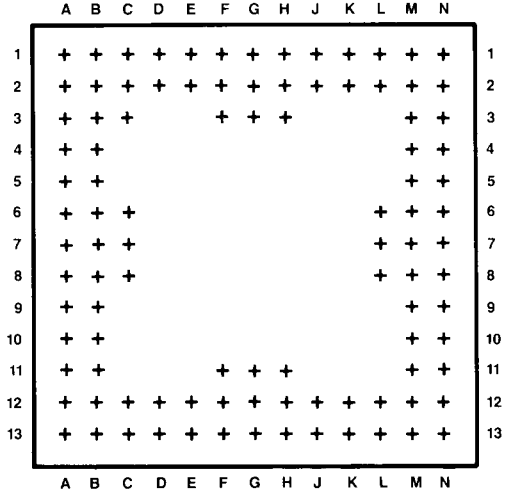
NOTES: 1) Commercial: V_{CC} = +5V ± 5%, T_A = 0°C to 70°C.
2) Military: V_{CC} = +5V ± 10%, T_A = −55°C to +125°C.

PACKAGE ORIENTATION

101 PIN PGA PACKAGE



TOP VIEW
(THROUGH PACKAGE VIEW)



BOTTOM VIEW

FUNCTIONAL TABLES

Mnemonic	MICRO CODE				ALU SOURCE OPERANDS	
	I_2	I_1	I_0	Octal Code	R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Table 1 : ALU Source Operand Control.

Mnemonic	MICRO CODE				ALU Function	SYMBOL
	I_5	I_4	I_3	Octal Code		
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	R ∨ S
AND	H	L	L	4	R AND S	R ∧ S
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EXOR S	$R \bar{\vee} S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \bar{\vee} S}$

Table 2. ALU Function Control.

Mnemonic	MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
	I_8	I_7	I_6	Octal Code	SHIFT	LOAD	SHIFT	LOAD		RAM_0	RAM_{15}	Q_0	Q_{15}
QREG	L	L	L	0	X	NONE	NONE	F→Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F→B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F→B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2→B	DOWN	Q/2→Q	F	F_0	IN_{15}	Q_0	IN_{15}
RAMD	H	L	H	5	DOWN	F/2→B	X	NONE	F	F_0	IN_{15}	Q_0	X
RAMQU	H	H	L	6	UP	2F→B	UP	2Q→Q	F	IN_0	F_{15}	IN_0	Q_{15}
RAMU	H	H	H	7	UP	2F→B	X	NONE	F	IN_0	F_{15}	X	Q_{15}

X = Don't care.
B = Register Addressed by B inputs.
DOWN is toward LSB. UP is toward MSB.

Table 3. ALU Destination Control.

		I_{210} (Octal Code)							
		0	1	2	3	4	5	6	7
I_{543} (Octal Code)	ALU Function	ALU Source (R, S)							
		A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0	C_n = L R Plus S C_n = H	A + Q A + Q + 1	A + B A + B + 1	Q Q + 1	B B + 1	A A + 1	D + A D + A + 1	D · Q D + Q + 1	D D + 1
1	C_n = L S Minus R C_n = H	Q − A − 1 Q − A	B − A − 1 B − A	Q − 1 Q	B − 1 B	A − 1 A	A − D − 1 A − D	Q − D − 1 Q − D	− D − 1 − D
2	C_n = L R Minus S C_n = H	A − Q − 1 A − Q	A − B − 1 A − B	− Q − 1 − Q	− B − 1 − B	− A − 1 − A	D − A − 1 D − A	D − Q − 1 D − Q	D − 1 D
3	R OR S	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
4	R AND S	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
5	$\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6	R EX-OR S	$A \bar{\vee} Q$	$A \bar{\vee} B$	Q	B	A	$D \bar{\vee} A$	$D \bar{\vee} Q$	D
7	R EX-NOR S	$\overline{A \bar{\vee} Q}$	$\overline{A \bar{\vee} B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \bar{\vee} A}$	$\overline{D \bar{\vee} Q}$	$\overline{D}$

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; $\bar{\vee}$ = EX-OR.

Table 4. Source Operand and ALU Function Matrix.

SOURCE OPERANDS AND ALU FUNCTIONS

Eight source operand pairs are available to the ALU as determined by the I0, I1, and I2 instruction inputs. The ALU performs eight functions; three arithmetic and five logic. This function selection is controlled by the I3, I4, and I5 instruction inputs. When in the arithmetic mode, the ALU results are also affected by the carry, Cn. In the logic mode, the Cn input has no effect.

The matrix of Table 4 results when Cn and I0 through I5 are viewed together. Table 5 defines the logic operations which the WS59032 can perform and Table 6 shows the arithmetic operations of the device. Both carry-in HIGH (Cn = 1) and carry-in LOW (Cn = 0) are defined in these operations.

Octal I_{543}, I_{210}	Group	Function
40	AND	$A \wedge Q$
41		$A \wedge B$
45		$D \wedge A$
46		$D \wedge Q$
30	OR	$A \vee Q$
31		$A \vee B$
35		$D \vee A$
36		$D \vee Q$
60	EX-OR	$A \triangledown Q$
61		$A \triangledown B$
65		$D \triangledown A$
66		$D \triangledown Q$
70	EX-NOR	$\overline{A \triangledown Q}$
71		$\overline{A \triangledown B}$
75		$\overline{D \triangledown A}$
76		$\overline{D \triangledown Q}$
72	INVERT	$\overline{Q}$
73		$\overline{B}$
74		$\overline{A}$
77		$\overline{D}$
62	PASS	Q
63		B
64		A
67		D
32	PASS	Q
33		B
34		A
37		D
42	"ZERO"	0
43		0
44		0
47		0
50	MASK	$\overline{A} \wedge Q$
51		$\overline{A} \wedge B$
55		$\overline{D} \wedge A$
56		$\overline{D} \wedge Q$

Table 5. ALU Logic Mode Functions.

Octal I_{543}, I_{210}	C_n = L		C_n = H	
	Group	Function	Group	Function
00	ADD	A + Q	ADD plus one	A + Q + 1
01		A + B		A + B + 1
05		D + A		D + A + 1
06		D + Q		D + Q + 1
02	PASS	Q	Increment	Q + 1
03		B		B + 1
04		A		A + 1
07		D		D + 1
12	Decrement	Q - 1	PASS	Q
13		B - 1		B
14		A - 1		A
27		D - 1		D
22	1's Comp.	-Q - 1	2's Comp. (Negate)	-Q
23		-B - 1		-B
24		-A - 1		-A
17		-D - 1		-D
10	Subtract (1's Comp.)	Q - A - 1	Subtract (2's Comp.)	Q - A
11		B - A - 1		B - A
15		A - D - 1		A - D
16		Q - D - 1		Q - D
20		A - Q - 1		A - Q
21		A - B - 1		A - B
25		D - A - 1		D - A
26		D - Q - 1		D - Q

Table 6. ALU Arithmetic Mode Functions.

WS59032D COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032D over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	51ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	26.4 MHz
Minimum Clock Low Time	22ns
Minimum Clock High	26ns
Minimum Clock Period	48ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	30ns
From $\overline{OE}$ High to output disable	25ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F = 0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	66	66	58	66	62	75	—	ns
D0-D31	45	45	35	45	35	48	—	
C_n	36	36	18	36	32	42	—	
I_{012}	46	46	35	46	41	58	—	
I_{345}	51	51	41	51	46	53	—	
I_{678}	22	—	—	—	—	22	20	
A BYPASS ALU (I = 2XX)	46	—	—	—	—	—	—	
CLOCK	51	51	42	51	46	59	22	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	20	1 (Note 3)	53 (Note 4)	0	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		0	
D0-D31	—	—	20	0	
C_n	—	—	22	0	
I_{012}	—	—	28	0	
I_{345}	—	—	30	0	
I_{678}	7	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	7	3	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032D MILITARY RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032D over the Military operating temperature range of −55°C to +125°C and a power supply range of 5V ± 10%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	60ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	23.6 MHz
Minimum Clock Low Time	28ns
Minimum Clock High	30ns
Minimum Clock Period	60ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	36ns
From $\overline{OE}$ High to output disable	30ns

2

COMBINATIONAL PROPAGATION DELAYS (C_L = 50PF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F = 0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	72	72	63	69	69	81	—	ns
D0-D31	51	51	40	52	42	52	—	
C_n	41	41	21	39	36	36	—	
I_{012}	48	48	40	48	44	63	—	
I_{345}	54	54	46	56	51	57	—	
I_{678}	27	—	—	—	—	21	20	
A BYPASS ALU (I = 2XX)	51	—	—	—	—	—	—	
CLOCK	58	58	50	58	53	66	29	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up before H L	Hold after H L	Set Up before L H	Hold after L H	UNITS
A, B Source Address	25	1 (Note 3)	63 (Note 4)	1	ns
B Destination Address	25	DO NOT CHANGE (Note 2)		1	
D0-D31	—	—	30	0	
C_n	—	—	30	0	
I_{012}	—	—	36	0	
I_{345}	—	—	42	0	
I_{678}	13	DO NOT CHANGE (Note 2)		0	
RAM0, 31 and Q0, 31	—	—	10	5	

NOTES:
1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H> L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H> L included here.

WS59032DA COMMERCIAL RANGE AC CHARACTERISTICS

The tables shown here specify the guaranteed performance of the WS59032DA over the Commercial operating temperature range of 0°C to +70°C and a power supply range of 5V ± 5%. Inputs are switching between 0 and 3V with rise and fall times of 1 V/ns and measurements made at 1.5V. All outputs have maximum DC load.

CYCLE TIME AND CLOCK CHARACTERISTICS

READ-MODIFY-WRITE (from select of A, B registers to end of cycle)	48ns
Maximum Clock Frequency to Shift Q (50% duty cycle, I = 432 or 632)	33MHz
Minimum Clock Low Time	18ns
Minimum Clock High	23ns
Minimum Clock Period	42ns

OUTPUT ENABLE/DISABLE TIME

Disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage.

From $\overline{OE}$ Low to Y output enable	27ns
From $\overline{OE}$ High to output disable	20ns

COMBINATIONAL PROPAGATION DELAYS (C_L = 50pF)

FROM INPUT \ TO OUTPUT	Y	F31	C_{n+32}	F = 0	OVR	RAM0, RAM31	Q0, Q31	UNITS
A, B ADDRESS	62	62	54	60	56	64	–	ns
D0-D31	39	39	31	39	31	42	–	
C_n	33	33	16	30	27	37	–	
I_{012}	38	38	30	39	35	49	–	
I_{345}	47	47	39	45	40	46	–	
I_{678}	22	–	–	–	–	22	16	
A BYPASS ALU (I = 2XX)	42	–	–	–	–	–	–	
CLOCK	47	46	38	46	43	49	18	

SET-UP AND HOLD TIMES RELATIVE TO CLOCK (CP) INPUT

INPUT \ CP	Set Up Before H L	Hold After H L	Set Up Before L H	Hold After L H	UNITS
A, B Source Address	20	0 (Note 3)	44 (Note 4)	0	ns
B Destination Address	10	DO NOT CHANGE (Note 2)		0	
D0-D31	–	–	22	0	
C_n	–	–	22	0	
I_{012}	–	–	28	0	
I_{345}	–	–	31	0	
I_{678}	5	DO NOT CHANGE (Note 2)		0	
RAM0 31 and Q0, 31	–	–	5	3	

NOTES:

1) Dashes indicate that a set-up time constraint or a propagation delay path does not exist.
2) The phrase "DO NOT CHANGE" indicates that certain signals must remain low for the duration of the clock Low time. Otherwise, erroneous operation may be the result.
3) Prior to clock H > L transition, source addresses must be stable to allow time for the source data to be set up before the latch closes. After this transition the A address may be changed. If it is not being used as a destination, the B address may also be changed. If it is being used as a destination, the B address must remain stable during the clock Low period.
4) Set-up time before H > L included here.

COMPETITIVE TIMING ANALYSIS

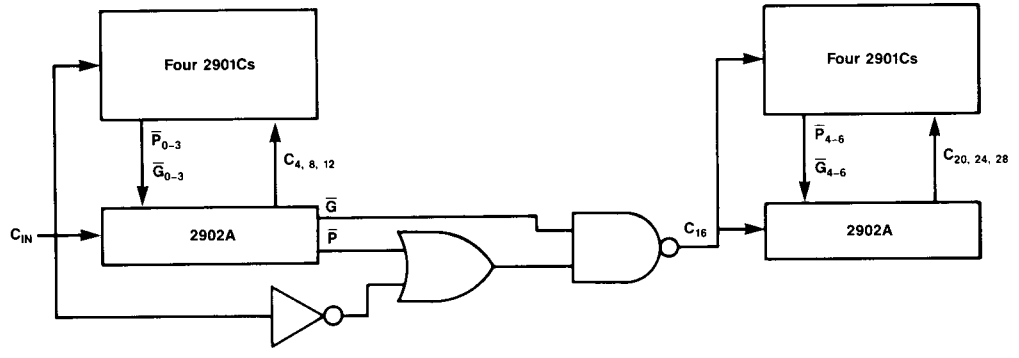
The following analysis compares the critical timing paths of a WS59032DA vs the equivalent Bipolar circuit implementation using eight 2901C's, two 2902A's and three high speed logic gates (See Figure).

As can be seen from the following comparison, the Data Path of the WS59032DA is 38% faster than the Data Path of the Bipolar/ECL functional equivalent circuit. Additionally, the Control Path of the WS59032DA is 60% faster than the Bipolar/ECL implementation. The actual values for the Bipolar/ECL circuit will be lengthened by the layout dependent interconnect delays between the individual devices. When these delays are taken into account, the WS59032DA speed advantage becomes even greater.

TIMING COMPARISON
WS59032DA vs Eight 2901C's, Two 2902A's Plus High Speed Logic

DATA PATH	CONTROL PATH
WS59032DA	**WS59032DA**
A,B Address → F = Ø = 60ns	I 012 → F = Ø = 39 ns
interconnect delay = Øns	interconnect delay = Ø ns
Total Delay ≤60ns	Total Delay ≤39 ns
DISCRETE IMPLEMENTATION (See Figure)	DISCRETE IMPLEMENTATION (See Figure)
A,B → $\overline{P}_3,\overline{G}_3$ = 37ns	I 012 → F = Ø = 37ns
$\overline{P}_3,\overline{G}_3$ → $\overline{P},\overline{G}$ = 11ns	$\overline{P}_3,\overline{G}_3$ → $\overline{P},\overline{G}$ = 11ns
$\overline{P},\overline{G}$ → C_{16} = 10ns	$\overline{P},\overline{G}$ → C_{16} = 10ns
C_{16} → C_{28} = 14ns	C_{16} → C_{28} = 14ns
C_{28} → F = Ø = 25ns	C_{28} → F = Ø = 25ns
interconnect delay = Xns	interconnect delay = Xns
Total Delay >97ns	Total Delay >97ns

Look-Ahead Carry Using Discrete Components



ORDERING INFORMATION

PART NUMBER	SPEED	PACKAGE TYPE	PACKAGE DRAWING	OPERATING TEMPERATURE RANGE	WSI MANUFACTURING PROCEDURE
WS59032DAG	D	101 Pin Ceramic PGA	G2	Comm'l	Standard
WS59032DG	D	101 Pin Ceramic PGA	G2	Comm'l	Standard
WS59032DGM	D	101 Pin Ceramic PGA	G2	Military	Standard
WS59032DGMB	D	101 Pin Ceramic PGA	G2	Military	MIL-STD-883C