

Universal Semiconductor

N-Channel Enhancement Mode Quad D-Mos FET Analog Switch Arrays

Ordering Information

Description	20V, 50Ω	10V, 50Ω	15V, 50Ω
16-Pin Plastic DIP	SD5000N	SD5001N	SD5002N
16-Pin Cerdip	SD5000J	SD5001J	SD5002J
Gold-Backed Chips in Waffle Pack	SD5000CHP	SD5001CHP	SD5002CHP

Features:

- Self-Aligning Silicon Gate Structure
- Low Transfer Capacitance — 0.2 pF typ.
- Low Input Capacitance — 2.4 pF typ.
- Low Output Capacitance — 1.3 pF typ.
- High Off Isolation
- Low Insertion Loss
- High-Speed Switching

Applications:

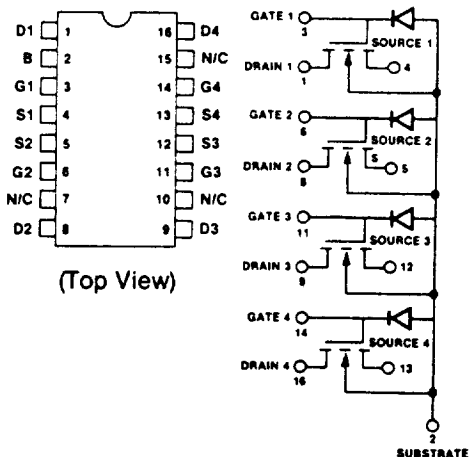
- ±10 V Analog Switches — SD5000
- ±5 V Analog Switches — SD5001
- ±7.5 V Analog Switches — SD5002
- Analog Multiplexers
- Analog Comparators
- Cross-Point Switches
- Sample and Hold

Absolute Maximum Ratings (T_A = +25°C unless otherwise noted)

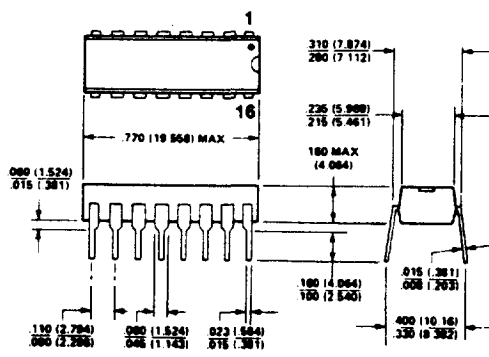
Parameter	SD5000	SD5001	SD5002	Units
V _{DS}	+20	+10	+15	Vdc
V _{SD}	+20	+10	+15	Vdc
V _{DB}	+25	+15	+22.5	Vdc
V _{SB}	+25	+15	+22.5	Vdc
V _{GS}	-25	-15	-22.5	Vdc
	+30	+25	+30	Vdc
V _{GB}	-0.3	-0.3	-0.3	Vdc
	+30	+25	+30	Vdc
V _{GD}	-25	-15	-22.5	Vdc
	+30	+25	+30	Vdc

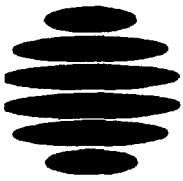
I _D	Continuous Drain Current	50mA
P _D	Total Package Power Dissipation (at or below T _A = +25°C)	640mW
	Linear Derating Factor	10.67mW/°C
P _D	Single Device Power Dissipation (at or below T _A = +25°C)	300mW
T _j	Operating Junction Temperature Range	
	'N' Package	-55 to +85°C
	'J' Package	-55 to +125°C
T _S	Storage Temperature Range	-55 to +150°C

Pin Configuration



Package Dimensions





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DC Electrical Characteristics (T_A = +25°C)

Parameter	SD5000			SD5001			SD5002			Unit	Test Conditions							
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max									
BV _{DS}	Drain-Source Breakdown Voltage			20	25		10	25		15	25	V	I _D = 10nA V _{GS} = V _{BS} = -5V					
BV _{SD}	Source-Drain Breakdown Voltage			20			10			15		V	I _S = 10nA V _{GD} = V _{BD} = -5V					
BV _{DB}	Drain-Substrate Breakdown Voltage			25	30		15	30		22.5	30	V	I _D = 10nA, V _{GB} = 0 Source Open					
BV _{SB}	Source-Substrate Breakdown Voltage			25	35		15	35		22.5	35	V	I _S = 10μA, V _{GB} = 0 Drain Open					
I _{D(off)}	Drain-Source Off Current						0.2	10				nA	V _{DS} = 10V	V _{GS} = V _{BS} = -5V				
										0.2	10				nA	V _{DS} = 15V		
										0.2	10				nA	V _{DS} = 20V		
I _{S(off)}	Source-Drain OFF Current						2.0	10				nA	V _{SD} = 10V	V _{GD} = V _{BD} = -5V				
										2.0	10				nA	V _{SD} = 15V		
										2.0	10				nA	V _{SD} = 20V		
I _{GBS}	Gate-Body Leakage Current						.01	1.0				μA	V _{GB} = 25V	V _{DB} = V _{SB} = 0				
										.01	1.0				μA	V _{GB} = 30V		
V _{GS(th)}	Gate Threshold Voltage			0.1	0.6	2.0	0.1	0.6	2.0	0.1	0.6	2.0	V	V _{DS} = V _{GS} , I _D = 1μA V _{SB} = 0				
r _{DS(on)}	Drain-Source ON Resistance			50			70			50			70			ohms	V _{GS} = 5V	I _D = 1mA V _{SB} = 0
				35			35			35			35			ohms	V _{GS} = 10V	
				28			28			28			28			ohms	V _{GS} = 15V	
				24			24			24			24			ohms	V _{GS} = 20V	
r _{DSM}	ON Resistance Match			1.0	5.0		1.0	5.0		1.0	5.0		ohms	V _{GS} = 5V				

AC Electrical Characteristics (T_A = +25°C)

Parameter	SD5000			SD5001			SD5002			Unit	Test Conditions			
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max					
g _{fs}	Common-Source Forward Transcond.			10	12		10	12		10	12	mrhos	V _{DS} = 10V, I _D = 20mA f = 1KHz, V _{SB} = 0	
C _(gs + gd + gb)	Gate Node Capacitance			2.4	3.5		2.4	3.5		2.4	3.5	pF	V _{DS} = 10V V _{GS} = V _{BS} = -15V f = 1MHz	
C _(gs + db)	Drain Node Capacitance			1.3	1.5		1.3	1.5		1.3	1.5	pF		
C _(gs + gd)	Source Node Capacitance			3.1	4.0		3.1	4.0		3.1	4.0	pF		
C _(dg)	Reverse Transfer Capacitance			0.2	0.5		0.2	0.5		0.2	0.5	pF		
C _T	Cross Talk			-107			-107			-107			dB	f = 3KHz, R _g = 600Ω