LOOK AHEAD CARRY LOGIC

The TC74HC182A is a high speed CMOS FUNCTION LOOK AHEAD CARRY GENERATOR fabricated with silicon gate C^2 MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

These circuits are capable of anticipating a carry across four binary adders or group of adders.They are cascadable to perform full look-ahead across n-bit adders. Carry, generate-carry, and propagate-carry functions are provided as shown in the pin designation table.

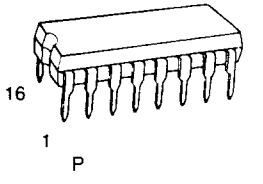
When used in conjunction with the HC181A aritimetic logic unit, these generators provide high-speed carry look-ahead capability for any word length. Each HC182A generates the look-ahead (anticipated carry)across a group of four ALU's and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. The method of cascading circuits to perform multi-level look-ahead is illustrated under typical application data.

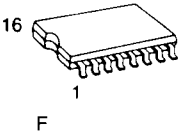
Carry input and output of the ALU's are in their true form, and the carry propagate(P) and carry generate(G) are in negated form; therefore, the carry functions(inputs, output, generate, and propagate) of the look-ahead generators are implemented in the compatible forms for direct connection to the ALU. Reinterpretation of carry functions as explained on the HC181A data sheet are also applicable to and compatible with the look-ahead generator.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

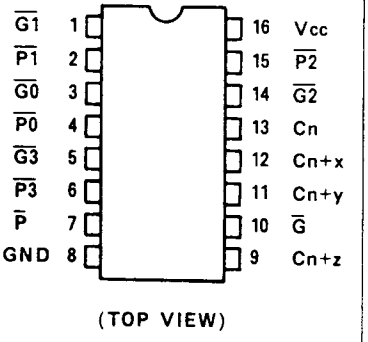
FEATURES:

- High Speed ····· t_{pd}=14ns(Typ.)at V_{CC}=5V
- Low Power Dissipation ····· I_{CC}=4μA(Max.)at Ta=25℃
- High Noise Immunity ····· $V_{NIH}=V_{NIL}$ 28% V_{CC} (Min.)
- Output Drive Capability ····· 10 LSTTL Loads
- Symmetrical Output Impedance ··· $|I_{OH}|=I_{OL}$=4mA(Min.)
- Balanced Propagation Delays ····· $t_{pLH} \simeq t_{pHL}$
- Wide Operating Voltage Range ··· V_{CC} (opr.)=2V~6V
- Pin and Function Compatible with 74LS182





PIN ASSIGNMENT



(TOP VIEW)

Pin Designation

Active"L"	Active"H"	Pin No.	Function
$\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$	G0, G1, G2, G3	3 , 1 , 14 , 5	Carry Generate Inputs
$\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$	P0, P1, P2, P3	4 , 2 , 15 , 6	Carry Propagate Inputs
Cn	$\overline{Cn}$	13	Carry Input
Cn+z, Cn+y Cn+z	$\overline{Cn+x}$, $\overline{Cn+y}$ $\overline{Cn+z}$	12 , 11 , 9	Carry Outputs
$\overline{G}$	Y	10	Carry Generate Output
$\overline{P}$	X	7	Carry Propagate Output
Vcc		16	Supply Voltage
GND		8	Ground

TRUTH TABLE

FOR $\overline{G}$ OUTPUT

INPUTS							OUTPUT
$\overline{G3}$	$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{G}$
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
All other combinations							H

FOR $\overline{P}$ OUTPUT

INPUTS				OUTPUT
$\overline{P3}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	$\overline{P}$
L	L	L	L	L
All other combinations				H

FOR Cn+z OUTPUT

INPUTS							OUTPUT
$\overline{G2}$	$\overline{G1}$	$\overline{G0}$	$\overline{P2}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+z
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

FOR Cn+x OUTPUT

INPUTS			OUTPUT
$\overline{G0}$	$\overline{P0}$	Cn	Cn+x
L	X	X	H
X	L	H	H
All other combinations			L

FOR Cn+y OUTPUT

INPUTS					OUTPUT
$\overline{G1}$	$\overline{G0}$	$\overline{P1}$	$\overline{P0}$	Cn	Cn+y
L	X	X	X	X	H
X	L	L	X	X	H
X	X	L	L	H	H
All other combinations					L

X:Don't care

$Cn+x=G0+P0Cn$

$Cn+y=G1+P1G0+P1P0Cn$

$Cn+z=G2+P2G1+P2P1G0+P2P1P0Cn$

$\overline{G}=\overline{G3+P3G2+P3P2G1+P3P2P1G0}$

$\overline{P}=\overline{P3P2P1P0}$

or

$\overline{Cn+x}=\overline{Y0(X0+Cn)}$

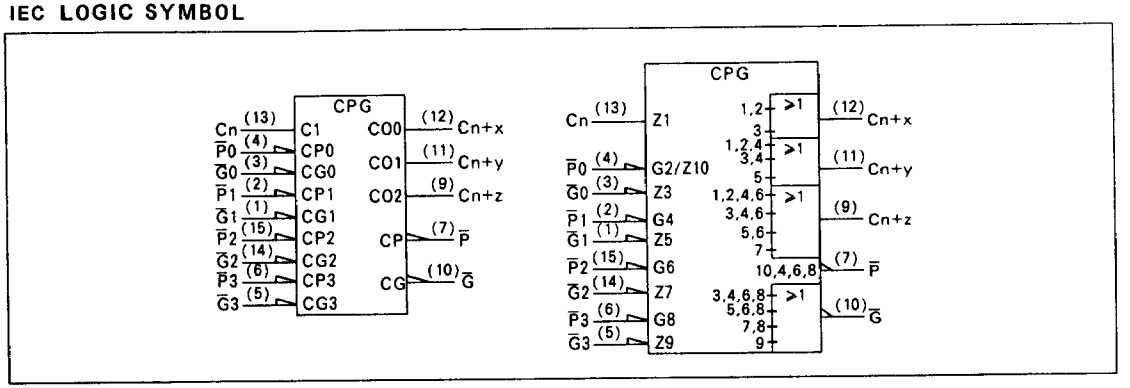
$\overline{Cn+y}=\overline{Y1[X1+Y0(X0+Cn)]}$

$\overline{Cn+z}=\overline{Y2[X2+Y1[X1+Y0(X0+Cn)]]}$

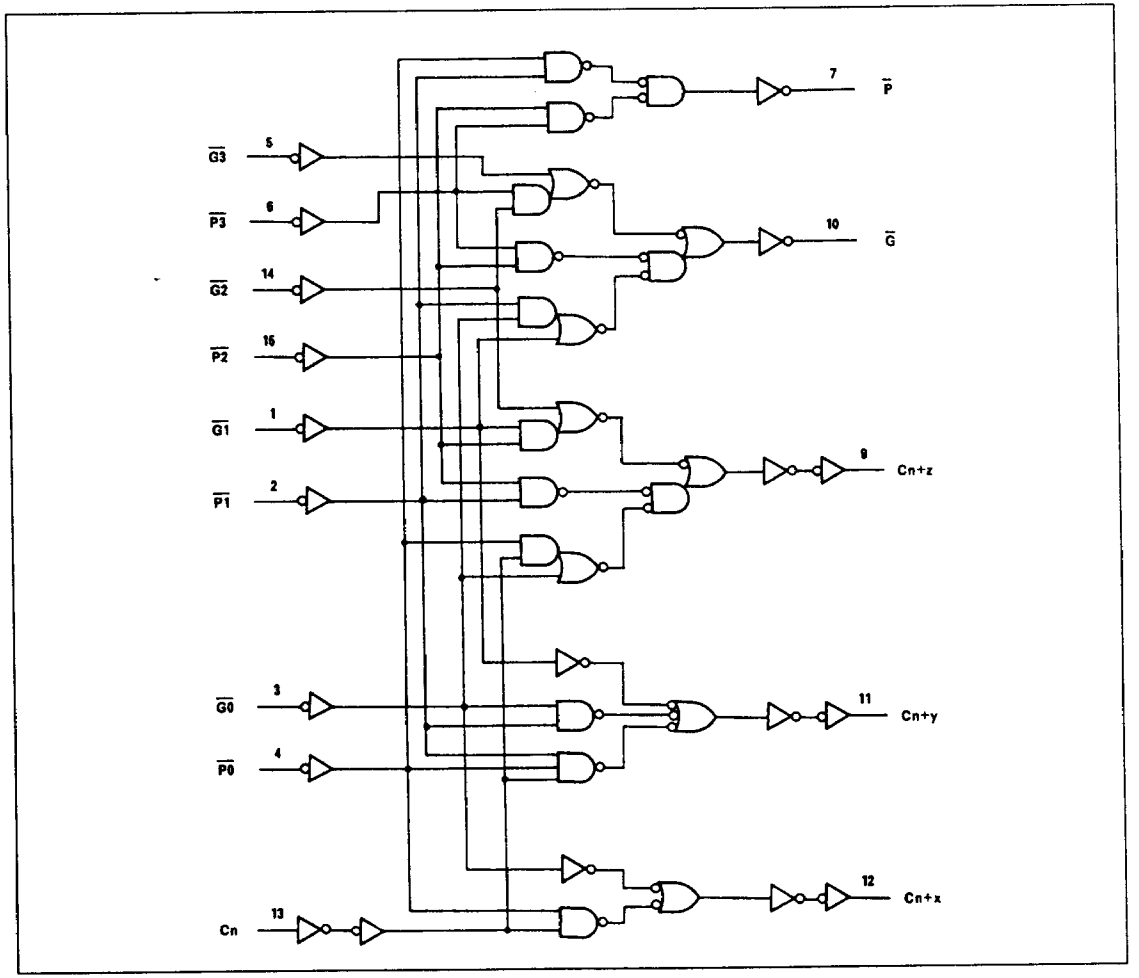
$Y=Y3(X3+Y2)(X3+X2+Y1)(X3+X2+X1+Y0)$

$X=X3+X2+X1+X0$

IEC LOGIC SYMBOL



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	−0.5 ~ 7	V
DC Input Voltage	V_{IN}	−0.5 ~ V_{CC} +0.5	V
DC Output Voltage	V_{OUT}	−0.5 ~ V_{CC} +0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(SOIC)	mW
Storage Temperature	T_{stg}	−65 ~ 150	℃
Lead Temperature 10sec	T_L	300	℃

*500mW in the range of Ta= −40℃~ 65℃. From Ta=65℃ to 85℃ a derating factor of −10mW/℃ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	−40 ~ 85	℃
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC}=2.0V) 0 ~ 500(V_{CC}=4.5V) 0 ~ 400(V_{CC}=6.0V)	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION		V_{CC}	Ta=25℃ MIN.	Ta=25℃ TYP.	Ta=25℃ MAX.	Ta=−40 ~85℃ MIN.	Ta=−40 ~85℃ MAX.	UNIT
High-Level Input Voltage	V_{IH}			2.0	1.5	−	−	1.5	−	V
				4.5	3.15	−	−	3.15	−	
				6.0	4.2	−	−	4.2	−	
Low-Level Input Voltage	V_{IL}			2.0	−	−	0.5	−	0.5	V
				4.5	−	−	1.35	−	1.35	
				6.0	−	−	1.8	−	1.8	
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} =−20 μA	2.0	1.9	2.0	−	1.9	−	V
				4.5	4.4	4.5	−	4.4	−	
				6.0	5.9	6.0	−	5.9	−	
			I_{OH} =−4 mA	4.5	4.18	4.31	−	4.13	−	
			I_{OH} =−5.2mA	6.0	5.68	5.80	−	5.63	−	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} =20 μA	2.0	−	0.0	0.1	−	0.1	V
				4.5	−	0.0	0.1	−	0.1	
				6.0	−	0.0	0.1	−	0.1	
			I_{OL} =4 mA	4.5	−	0.17	0.26	−	0.33	
			I_{OL} =5.2mA	6.0	−	0.18	0.26	−	0.33	
Input Leakage Current	I_{IN}	V_{IN} =V_{CC} or GND		6.0	−	−	±0.1	−	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} =V_{CC} or GND		6.0	−	−	4.0	−	40.0	

AC ELECTRICAL CHARACTERISTICS (C_L =15pF, V_{CC}=5V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		–	4	8	ns
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}$ / $\overline{P0}, \overline{P1}, \overline{P2}$ – Cn+x, Cn+y / Cn+z)	t_{pLH} t_{pHL}		–	14	24	
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}, G3$ / $\overline{P1}, \overline{P2}, \overline{P3}$ – $\overline{G}$)	t_{pLH} t_{pHL}		–	16	27	
Propagation Delay Time ($\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$ – $\overline{P}$)	t_{pLH} t_{pHL}		–	14	24	
Propagation Delay Time (Cn–Cn+x, Cn+y, Cn+z)	t_{pLH} t_{pHL}		–	14	24	

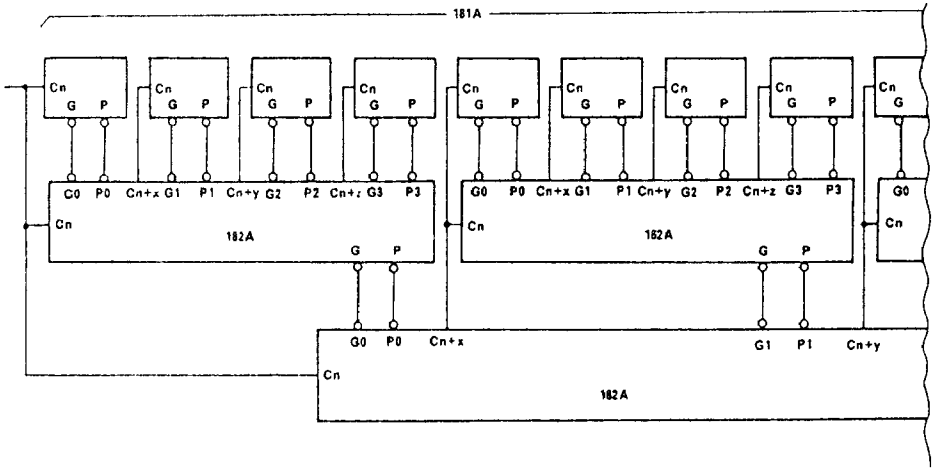
AC ELECTRICAL CHARACTERISTICS (C_L=50pF, Input t_r=t_f=6ns)

PARAMETER	SYMBOL	TEST CONDITION		Ta=25°C			Ta=–40 ~85°C		UNIT
			V_{CC}	MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		2.0	–	30	75	–	95	ns
			4.5	–	8	15	–	19	
			6.0	–	7	13	–	16	
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}$ / $\overline{P0}, \overline{P1}, \overline{P2}$ – Cn+x, Cn+y / Cn+z)	t_{pLH} t_{pHL}		2.0	–	62	135	–	170	
			4.5	–	17	27	–	34	
			6.0	–	13	23	–	29	
Propagation Delay Time ($\overline{G0}, \overline{G1}, \overline{G2}, \overline{G3}$ / $\overline{P1}, \overline{P2}, \overline{P3}$ – $\overline{G}$)	t_{pLH} t_{pHL}		2.0	–	72	150	–	190	
			4.5	–	19	30	–	38	
			6.0	–	14	26	–	33	
Propagation Delay Time ($\overline{P0}, \overline{P1}, \overline{P2}, \overline{P3}$ – $\overline{P}$)	t_{pLH} t_{pHL}		2.0	–	62	135	–	170	
			4.5	–	17	27	–	34	
			6.0	–	13	23	–	29	
Propagation Delay Time (Cn–Cn+x, Cn+y, Cn+z)	t_{pLH} t_{pHL}		2.0	–	62	135	–	170	
			4.5	–	17	27	–	34	
			6.0	–	13	23	–	29	
Input Capacitance	C_{IN}			–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD} (1)			–	61	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.
Average operating current can be obtained by the equation:

$$I_{CC(opr)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

TYPICAL APPLICATION



64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS