512Mbit GDDR4 SGRAM

2M x 32Bit x 8 Banks
Graphic Double Data Rate 4
Synchronous DRAM
with Uni-directional Data Strobe and DLL
(136Ball FBGA)

Revision 1.2

May 2007

Revision History

Revision	Month	Year	History
0.0	September	2005	-***Target Spec*** - Initial Draft.
0.1	December	2005	- correct typo
0.3	January	2006	- ***Preliminary Spec*** - correct typo - Adding the 2.8Gbps spec
1.0	June	2006	- Correct AC paramter(Cas Latency) - Adding the 2.2/2.4/2.8Gbps spec - Adding the IBIS - Adding the Current spec - define the CL of DBIdc below as CL of DBIdc = Normal CL + 2 tCK - Revision Multi-preamble
1.1	September	2006	- Adding the target spec of speed at 3.2Gbps (*K4U52324QE-BC06) - WL=7 only use less than 2.0Gbps. (page 11) - Remove note1. WL limitation of Rev1.0 (page67) - adding the AC parameter at 3.2Gbps (page67)
1.2	May	2007	- Added Revision ID on page 22. - Added power dissipation data on page 63.

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2M x 32Bit x 8 Banks Graphic Double Data Rate 4 Synchronous DRAM with Uni-directional Data Strobe

1.0 FEATURES

- 1.8V ± 0.09V power supply for device operation
- 1.8V ± 0.09V power supply for I/O interface
- On-Die Termination (ODT)
- Output Driver Strength adjustment by EMRS
- Calibrated output drive
- 1.8V Pseudo Open drain compatible inputs/outputs
- 8 internal banks for concurrent operation
- Differential clock inputs (CK and $\overline{CK}$)
- Commands entered on each positive CK edge
- Double pumping address
- CAS latency : 12, 13, 14, 15, 16, 17, 18, 19, 20, 21, 22 (clock)
- Burst length : 8 only
- Programmable Write latency : 1, 2, 3, 4, 5, 6 and 7 (clock)
- Single ended READ strobe (RDQS) per byte
- Single ended WRITE strobe (WDQS) per byte
- Auto Calibration mode by ZQ pin
- RDQS edge-aligned with data for READs
- WDQS center-aligned with data for WRITEs
- Data Mask(DM) for masking WRITE data
- Multi-preamble
- DBI(Data Bus Inversion) mode
- Auto & Self refresh modes
- Auto Precharge option
- 32ms, auto refresh (8K cycle)
- Lead Free 136 Ball FBGA(RoHS Compliant)
- Maximum clock frequency up to 1.4GHz
- Maximum data rate up to 2.8Gbps/pin
- DLL for edge aligned outputs
- Mirror function with MF pin
- Boundary scan function with SEN pin

2.0 ORDERING INFORMATION

Part Number	Max Freq.	Max Data Rate	Interface	Package
*K4U52324QE-BC06	1.6GHz	3.2Gbps/pin	Pseudo Open Drain_18	136 Ball FBGA
K4U52324QE-BC07	1.4GHz	2.8Gbps/pin		
K4U52324QE-BC08	1.2GHz	2.4Gbps/pin		
K4U52324QE-BC09	1.1GHz	2.2Gbps/pin		

Note: *K4U52324QE-BC06(3.2Gbps) is only tarage spec for AC parameter and Initial target voltage VDD/VDDQ = 1.95V ± 0.05V.

3.0 GENERAL DESCRIPTION

FOR 2M x 32Bit x 8 Bank GDDR4 SGRAM

The K4U52324QE is 536,870,912 bits of hyper synchronous data rate Dynamic RAM organized as 8 x 2,097,152 words by 32 bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 11.2GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

16MX32 GDDR4 SGRAM ADDRESSING

CONFIGURATION	16MX32 GDDR4 Addressing Scheme
	16Mx32
Row address	A0~A11
Column address	A0~A7,A9
Bank address	BA0~BA2
Autoprecharge	A8
Refresh	8K/32ms
Refresh period	3.9us

4.0 PIN CONFIGURATION

Normal Package (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12
A	VDDQ	VDD	VSS	ZQ					MF	VSS	VDD	VDDQ
B	VSSQ	DQ0	DQ1	VSSQ					VSSQ	DQ9	DQ8	VSSQ
C	VDDQ	DQ2	DQ3	VDDQ					VDDQ	DQ11	DQ10	VDDQ
D	VSSQ	WDQS0	RDQS0	VSSQ					VSSQ	RDQS1	WDQS1	VSSQ
E	VDDQ	DQ4	DM0	VDDQ					VDDQ	DM1	DQ12	VDDQ
F	VDD	DQ6	DQ5	VSSQ					VSSQ	DQ13	DQ14	VDD
G	VSS	VSSQ	DQ7	$\overline{CAS}$					$\overline{CS}$	DQ15	VSSQ	VSS
H	VDDQ	$\overline{RAS}$	$\overline{CKE}$	BA0/A1					BA1/A5	$\overline{WE}$	RFM	VDDQ
J	VSS	RFU	RFU	VREFC					VREFD	$\overline{CK}$	CK	VSS
K	VDD	A10/A0	A12/A2	VSS					VSS	BA2/A6	A8/A4	VDD
L	VSS	VSSQ	DQ25	A11/A3					A9/A7	DQ17	VSSQ	VSS
M	VDD	DQ24	DQ27	VSSQ					VSSQ	DQ19	DQ16	VDD
N	VDDQ	DQ26	DM3	VDDQ					VDDQ	DM2	DQ18	VDDQ
P	VSSQ	WDQS3	RDQS3	VSSQ					VSSQ	RDQS2	WDQS2	VSSQ
R	VDDQ	DQ28	DQ29	VDDQ					VDDQ	DQ21	DQ20	VDDQ
T	VSSQ	DQ30	DQ31	VSSQ					VSSQ	DQ23	DQ22	VSSQ
V	VDDQ	VDD	VSS	SEN					RESET	VSS	VDD	VDDQ

Note :

RFU is reserved for future use

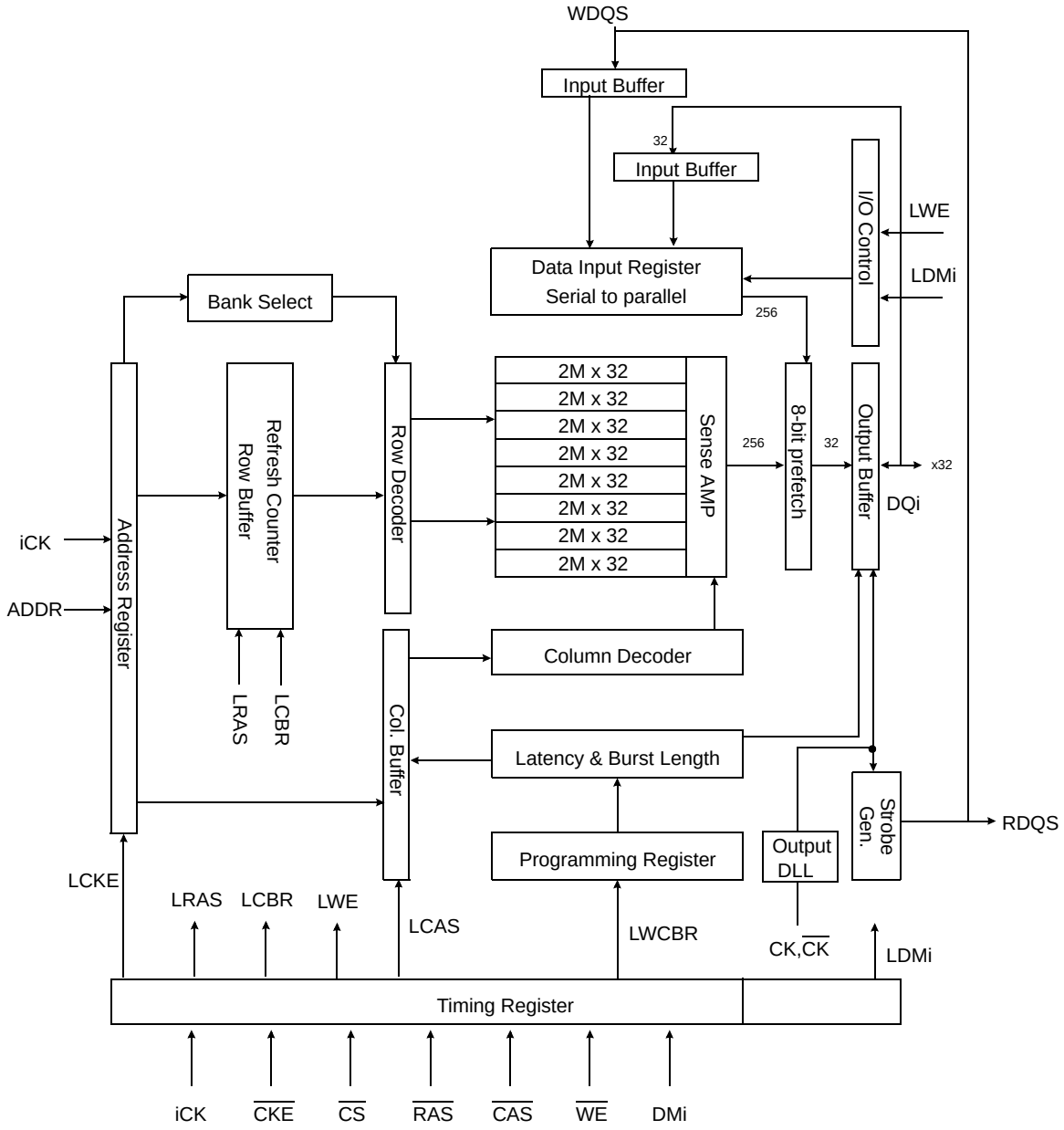
RFM : When the MF ball is tied LOW, RFM(H11) receiver is disabled and it recommended to be driven to a static LOW state, however, either static HIGH or floating state on this pin will not cause any problem for the DRAM. When the MF ball is tied HIGH, $\overline{RAS}$(H2) becomes RFM due to mirror function and the receiver is disabled. It is recommended to be driven to a static LOW state, however, either static HIGH or floating state on this pin will not cause any problem for the DRAM

Please refer to Mirror Function Signal Mapping table at page 6.

5.0 INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. CMD, ADD inputs are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Output (read) data is referenced to the crossings of CK and $\overline{CK}$ (both directions of crossing).
$\overline{CKE}$	Input	**Clock Enable:** $\overline{CKE}$ Low activates, and $\overline{CKE}$ High deactivates, internal clock signals and device input buffers and output drivers. Taking $\overline{CKE}$ High provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). $\overline{CKE}$ is synchronous for power down entry and exit, and for self refresh entry. $\overline{CKE}$ is asynchronous for self refresh exit. $\overline{CKE}$ must be maintained Low throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ and $\overline{CKE}$ are disabled during power-down. Input buffers, excluding $\overline{CKE}$, are disabled during self refresh.
$\overline{CS}$	Input	**Chip Select:** All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
DM0 ~DM3	Input/ Output(DBI)	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of clock. Although DM pins are input only, the DM loading matches the DQ and WDQS loading. If DBI is enabled during Read operation, DM is a flag signal for DBI.
BA0 ~ BA2	Input	**Bank Address Inputs:** BA0 ,BA1 and BA2 define to which bank an Active, Read, Write or Precharge command is being applied.
A0 ~ A11	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands to select one location out of the memory array in the respective bank. A8 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A8 LOW) or all banks (A8 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1,BA2. The address inputs also provide the op-code during Mode Register Set commands. Row addresses : RA0 ~ RA11, Column addresses : CA0 ~ CA7, CA9 . Column address CA8 is used for auto precharge.
DQ0 ~ DQ31	Input/ Output	**Data Input/ Output:** Bi-directional data bus.
RDQS0 ~ RDQS3	Input(DBI)/ Output	**READ Data Strobe:** Output with read data. RDQS is edge-aligned with read data. If DBI is enabled during Write operation, RDQS is a flag signal for DBI.
WDQS0 ~ WDQS3	Input	**WRITE Data Strobe:** Input with write data. WDQS is center-aligned to the inout data.
RFU		Reserved for future use pin
V_{DDQ}	Supply	DQ Power Supply
V_{SSQ}	Supply	DQ Ground
V_{DD}	Supply	Power Supply
V_{SS}	Supply	Ground
V_{REF}	Supply	**Reference voltage:** 0.7*VDDQ , **2 Pins :** (J,9) for Data input , (J,4) for CMD and ADDRESS
MF	Input	Mirror Function for clamshell mounting of DRAMs. VDDQ CMOS input.
ZQ	Reference	Resistor connection pin for On-die termination.
RESET	Input	Reset pin: RESET pin is a VDDQ CMOS input
SEN	Input	**Scan enable :** Must tie to the ground in case not in use. VDDQ CMOS input
RFM	Input	**Reserved for Mirror Function** : When the MF ball is tied low, $\overline{RFM}$(H11) is recommended to be driven to logic low state. When the MF ball is tied high, $\overline{RAS}$(H2) switch to RFM and is recommended to be driven to logic low state

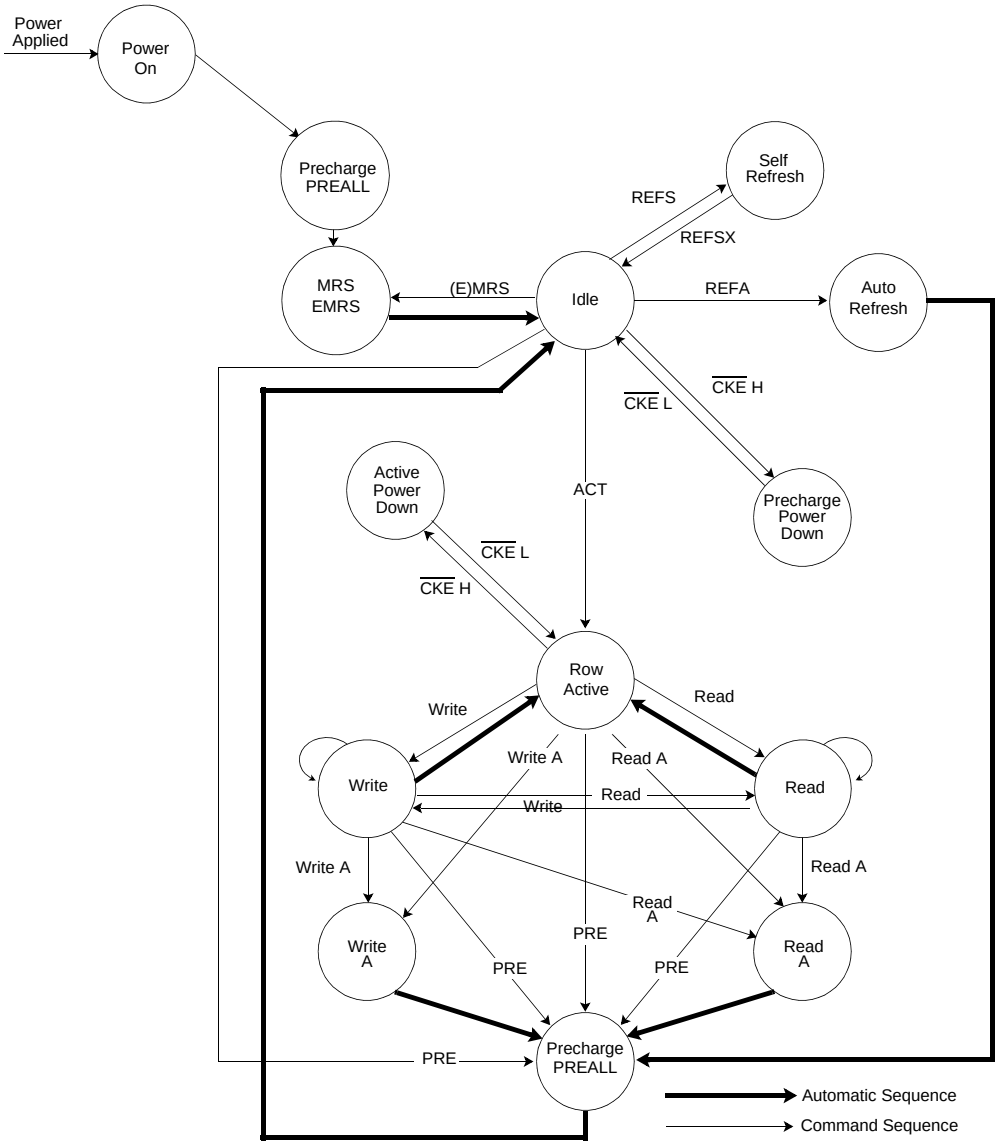
6.0 BLOCK DIAGRAM (2Mbit x 32I/O x 8 Bank)



* iCK : internal clock

7.0 FUNCTIONAL DESCRIPTION

7.1 SIMPLIFIED STATE DIAGRAM



PREALL = Precharge All Banks

MRS = Mode Register Set

EMRS = Extended Mode Register Set

REFS = Enter Self Refresh

REFSX = Exit Self Refresh

REFA = Auto Refresh

$\overline{CKE}$ H = Enter Power Down

$\overline{CKE}$ L = Exit Power Down

ACT = Active

Write A = Write with Autoprecharge

Read A = Read with Autoprecharge

PRE = Precharge

7.2 INITIALIZATION

GDDR4 SGRAM must be powered up and predefined manner below as sequence. Operational procedures other than those specified may result in undefined operation.

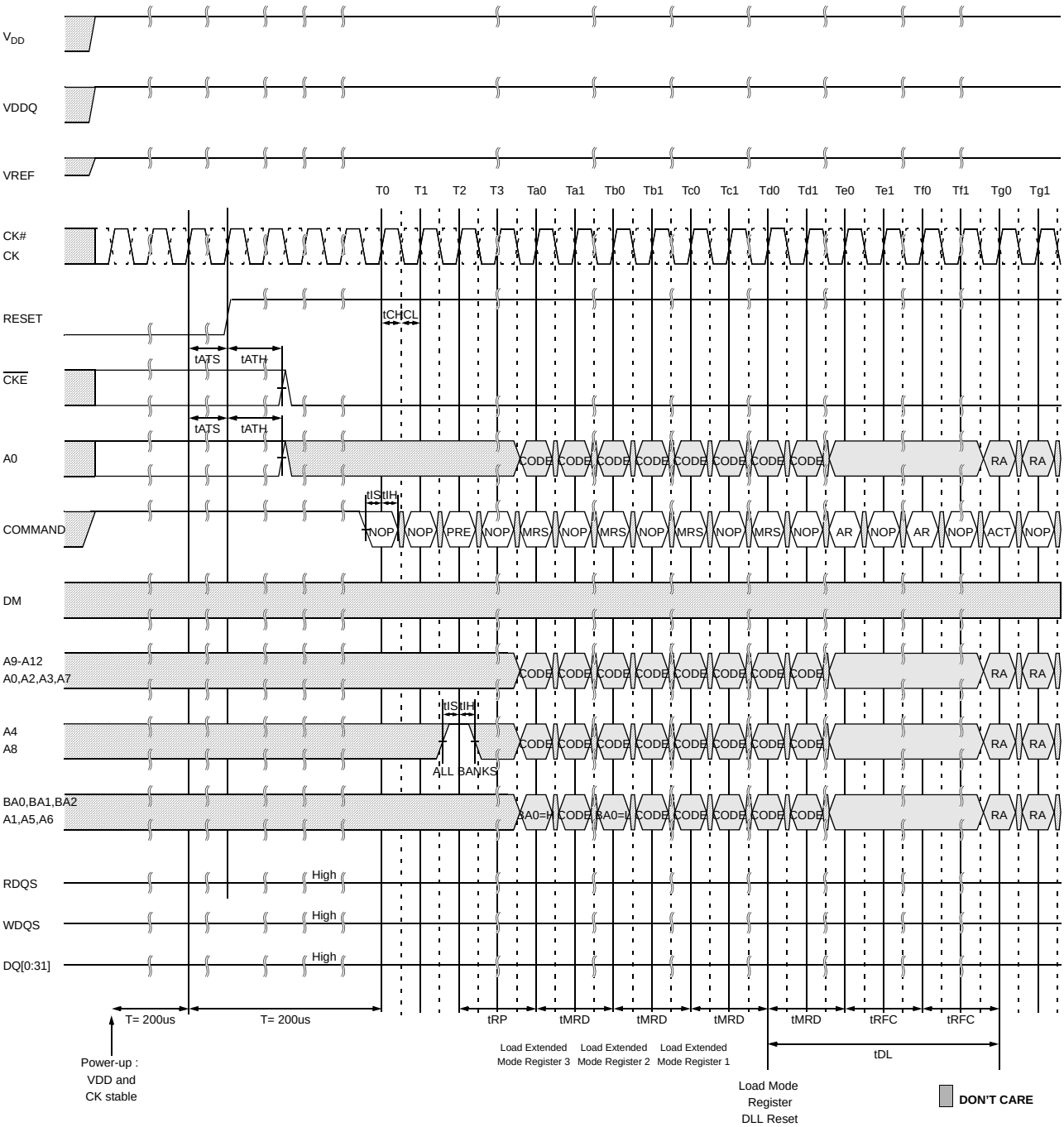
The Mode Register and Extended Mode Register do not have default values. If they are not programmed during the initialization sequence, it may lead to unspecified operation.

1. Apply power to VDD.
2. Apply power to VDDQ at same time or after power is applied to VDD.
3. Apply VREF at same time or after power is applied to VDDQ.(Inputs are not recognized as valid until after V_{REF} is applied)
4. Provide stable clock signals
5. Assert and hold RESET low
6. Wait 200 us
7. Bring RESET high latching the logic state of $\overline{CKE}$ and A0 to set the value of the address and command on die termination. See table 1 for the values and logic states for $\overline{CKE}$ and A0
8. $\overline{CKE}$ is then brought low after the on die termination is set.
9. Wait 200 us
10. Issue at least 2 NOP commands.
11. Issue a PRECHARGE ALL command followed by NOP commands to meet tRP
12. Issue MRS command to the mode register and the 3 extended mode registers in any order. The LMR command need to be spaced apart by tMRD.
13. Issue two AUTO REFRESH command
14. Once the two AUTO REFRESH commands are issued and tDL has been met the device is ready for operation.

TABLE 1. Address and Command On Die Termination

VALUE OHMS	$\overline{CKE}$	A0
ZQ/4	L	H
ZQ/2	H	H
ZQ	H	L

Note:
1. Before "Double Pumping address" is enabled, the Address and Command termination value is determined by the status of A10/A0 and $\overline{CKE}$.

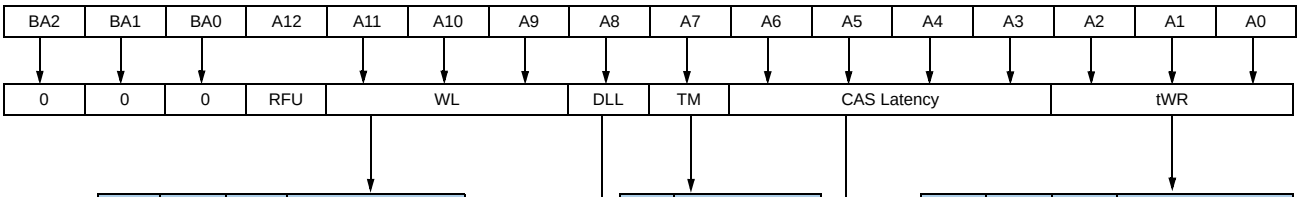


Note :

1. A DLL reset with A8 = H is required after enabling the DLL
2. 'MRD' is required before any command can be applied, and tDL is required before any command can be issued.
3. The two AUTO REFRESH command at Td0 and Te0 may be applied after the LOAD MODE REGISTER(LMR) command at Ta0.
4. PRE= PRECHARGE command, LMR = LOAD MODE REGISTER command, AR = AUTO REFRESH command, ACT = ACTIVE command, RA = Row Address, BA = Bank Address.

7.3 MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of GDDR4 SGRAM. It programs CAS latency, test mode and various vendor specific options to make GDDR4 SGRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for the proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (The GDDR4 SGRAM should be in active mode with $\overline{CKE}$ already Low prior to writing into the mode register). The state of address pins A_0 ~ A_{11} and BA_0, BA_1, BA_2 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the mode register. Minimum clock cycles specified as tMRD are required to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. CAS latency (read latency from column address) uses A_3, A_4, A_5, A_6, A_7 is used for test mode. A_8 is used for DLL reset. A_9 ~ A_{11} are used for Write latency. Refer to the table for specific codes for various addressing modes and CAS latencies.



A11	A10	A9	Write Latency
0	0	0	RFU
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

WL=1~6 use overal frequency

WL = 7 only use less than 2.0Gbps.

A7	Test Mode
0	Normal
1	Test Mode

A8	DLL Reset
0	No
1	Yes[1)]

A2	A1	A0	tWR
0	0	0	16
0	0	1	18
0	1	0	20
0	1	1	6
1	0	0	8
1	0	1	10
1	1	0	12
1	1	1	14

A6	A5	A4	A3	CAS Latency
0	0	0	0	16
0	0	0	1	17
0	0	1	0	18
0	0	1	1	19
0	1	0	0	20
0	1	0	1	21
0	1	1	0	22
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

Note : 1) DLL Reset is self-clearing.

BURST TYPE

Read and write accesses to the 16MX32 GDDR4 are burst-oriented, with the burst length fixed at 8 and thus not programmable in the MRS as with many other DRAMs. The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accessed for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A3 ~ Ai when the burst length is set to eight (where Ai is the most significant column address bit for a given configuration).

A2-A0 does not select the acess order whthin a burst and must be set zero.

Burst Definition

Burst Length	Starting Column Address			Order of Accesses Within a Burst
				Type= Sequential
8	A2	A1	A0	
	0	0	0	0 - 1 - 2 - 3 - 4 - 5 - 6 - 7

Note : 1. For a burst length of 8, A3-A7 select the block of 8 burst; A0-A2 select the starting column within the block and must be set to zero

WRITE Latency

The WRITE latency(WL) is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data. The latency can be set from 1 to 7 clocks depending on the operating frequency and desired current draw.

WRITE Recovery Time(tWR)

The value of tWR in the AC parametrics table of the GDDR4 SGRAM is loaded into register bits A0,A1,A2. The tWR register bits are not a required function and may be implemented at the discretion of the memory manufacturer.

CAS LATENCY (READ LATENCY)

The CAS latency is the delay, in clock cycles, between the registration of a READ command and the availability of the first bit of output data. The latency can be set to 7~22 clocks. If a READ command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n+m*. Below table indicates the operating frequencies at which each CAS latency setting can be used. Reserved states should not be used as unknown operation or incompatibility with future versions may result.

CAS Latency

SPEED	Allowable operating frequency (GHz)												
	CL=22	CL=21	CL=20	CL=19	CL=18	CL=17	CL=16	CL=15	CL=14	CL=13	CL=12	CL=11	CL=10
-07			≤ 1.4* (RDBI)		≤ 1.4								
-08					≤ 1.2* (RDBI)		≤ 1.2						
-09						≤ 1.1* (RDBI)		≤ 1.1					

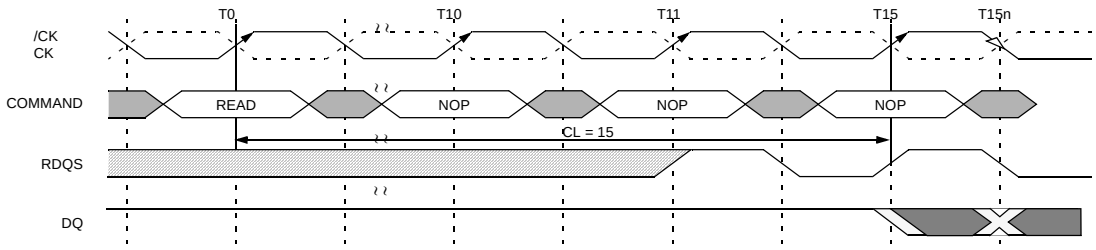
Note : * CL of RDBI(Read Data Bus Inversion) must be set by CL+2tCK, before 16MX32 GDDR4 is enable to DBIdc function.
CL of DBIdc = CL + 2tCK

Multi-preamble with CAS latency

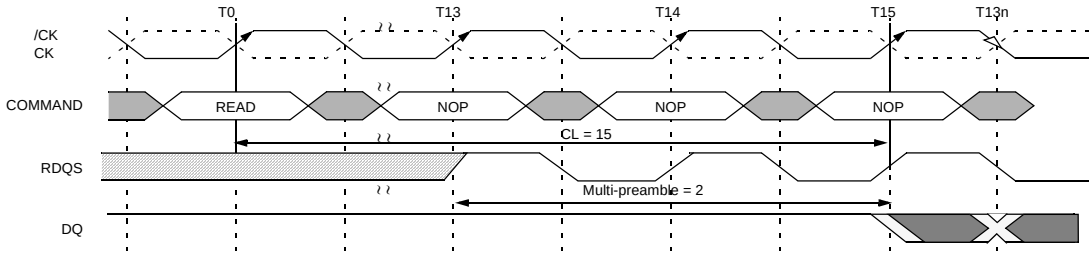
Operating CL	CL15 @ 1.1GHz	CL16 @ 1.2GHz	CL18 @ 1.4GHz
Multi-Preamble	1,2,3,		

Note: 1. 16MX32 GDDR4 can be enable to Multi-preamble more than CL15, and Multi-preamble is subject to restriction by 3tCK above the table.
2. If CL is added to 2tCK, Multi-preamble can use up to 5 tCK.
ex) CL17@1.1GHz, CL18@1.2GHz, CL20@1.4GHz
3. Multi-preamble is set by MRS. Refer to the MRS table of page 17
4. 16MX32 GDDR4 can't suppport for a Multi-preamble during DLL off mode.

Operation timing CL = 15



Operation timing CL = 15, Multi-preamble = 2

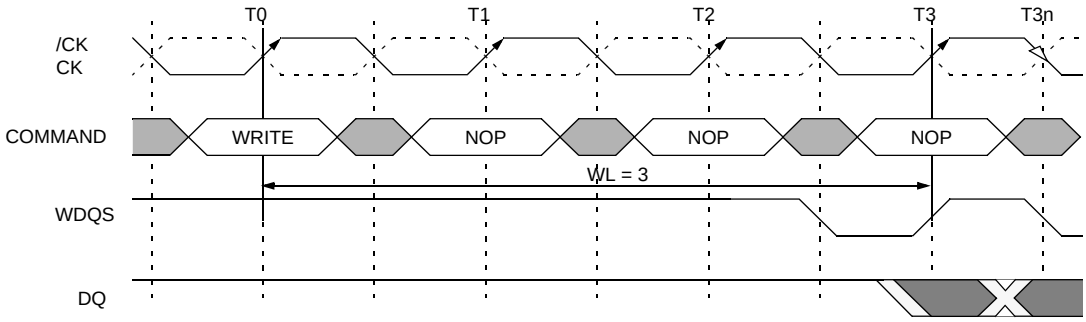


Burst Length = 8
Shown with nominal t_{AC} and nominal t_{DQSQ}

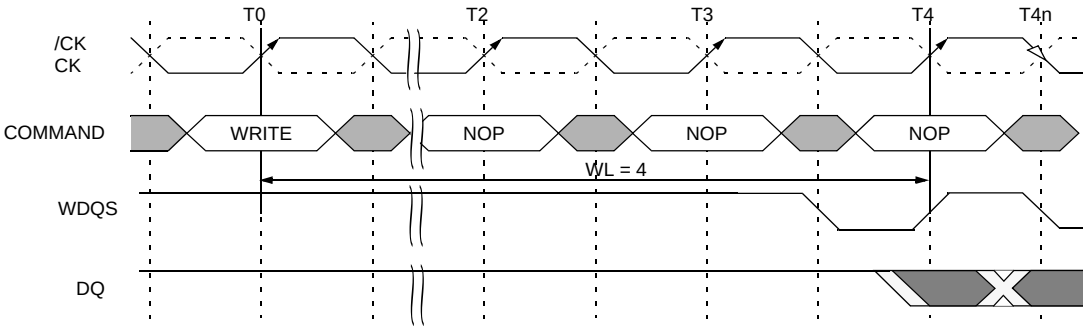
DON'T CARE TRANSITIONING DATA

WRITE LATENCY

The Write latency (WL) is the delay, in clock cycles, between the registration of a WRITE command and the availability of the first bit of input data. The latency can be set from 1 to 7 clocks depending in the operating frequency and desired current draw. When the write latencies are set to 1 or 2 or 3 clocks, the input receivers never turn off when the WRITE command is registered. If a WRITE command is registered at clock edge *n*, and the latency is *m* clocks, the data will be available nominally coincident with clock edge *n*+*m*. Reserved states should not be used as unknown operation or incompatibility with future versions may result.



Write latency = 3



Write latency = 4

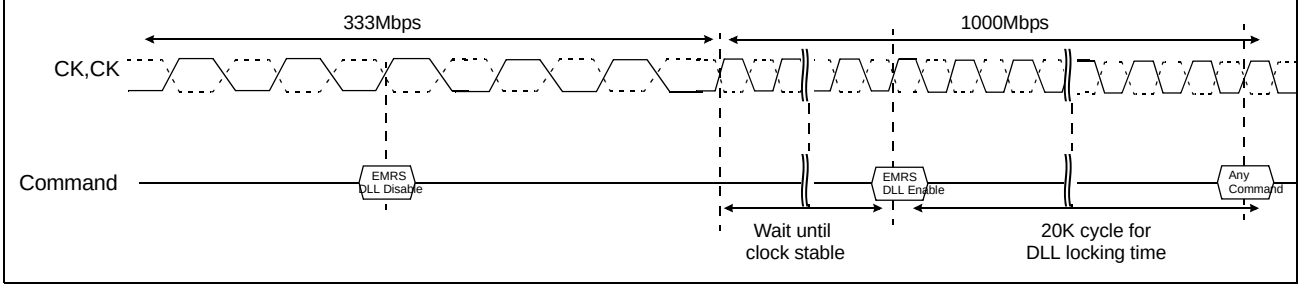
DON'T CARE **TRANSITIONING DATA**

DLL RESET

The normal operating mode is selected by issuing a MRS command with bit A8 set to zero, and bits A0 ~ A7 and A9 ~ A12 set to the desired values. DLL reset is initiated by issuing a MRS command with bit A8 set to one, and bits A0 ~ A7 and A9 ~ A12 set to the desired values. When a DLL reset is complete the GDDR4 SGRAM Reset bit, A8 of the mode register is self clearing(i.e. automatically set to a zero by the GDDR4 SGRAM)

In case the clock frequency need to be changed after the power-up GDDR4 doesn't require DLL reset. Instead, DLL should be disabled first before the frequency changed and then change the clock frequency as needed. After the clock frequency changed, there needed some time till clock become stable and then enable the DLL and then 20K cycle required to lock the DLL

Clock frequency change sequence after the power-up(example)



DLL ENABLE/DISABLE

The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after disabling the DLL for debugging or evaluation. (When the device exits self refresh mode, the DLL is enabled automatically.) Any time the DLL is enabled, 20K clock cycles must occur before an any command can be issued.

DLL AC Timings

Parameter	Symbol	Min	Typ	Max	Unit	Note
Clock Frequency (DLL on)	tCK			2.0	ns	1
Clock Frequency (DLL off)	tCK	6.0		20.0	ns	2

Note :
1. 16MX32 GDDR4 SGRAM support a minimum clock frequency of 500MHz for normal DLL-on operation, regardless of the speed bin of the device.
2. If users need operation below from 50MHz to 166MHz, they should use the DLL-off mode of the device.
3. 16MX32 GDDR4 SGRAM has a unknown operation period from 166MHz to 500MHz. We can't guarantee it during unknown period operation.

DLL INTRODUCTION

The GDDR4 uses a DLL to synchronize the byte lane to the clock. Although the DLL provides accurate clocking of data out, it requires a minimum operating frequency properly. The EXTENDED MODE REGISTER provides an avenue to turn the DLL off for running at lower frequencies.

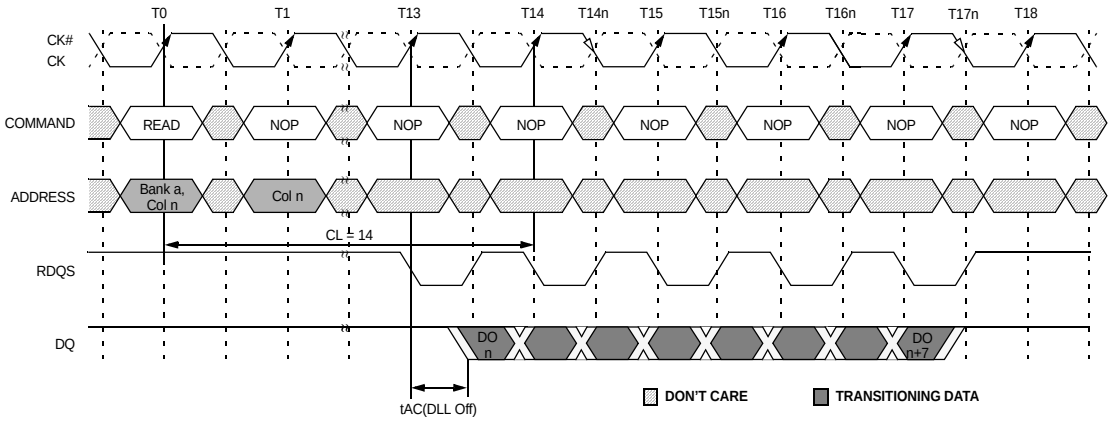
DLL OFF MODE

The GDDR4 devices default into the DLL off mode upon power-up. The device enters the DLL on mode of operation if and when the DLL is enabled, via a Load Mode Register Command to the Extended Mode Register. Once in the DLL on mode. the device remains in that mode until powered down or turned off via the EXTENDED MODE REGISTER.

With the DLL off mode the output, DQ and DQS transitions may or may not align with tCK and tCK# transitions, depending on clock fire-quency and CAS Latency settings.

The burst READ operation is a bit different from the standard DLL on mode. The frame from the READ command to first data out is defined by the CL-1tCK+tAC(DLL off). Data moves from the DRAM cell to the sense amp and is held in a buffer waiting for the appropri-ate clock cycle. The data will fire from the buffer tAC(DLL off) after the clock edge prior to the programmed CAS latency.

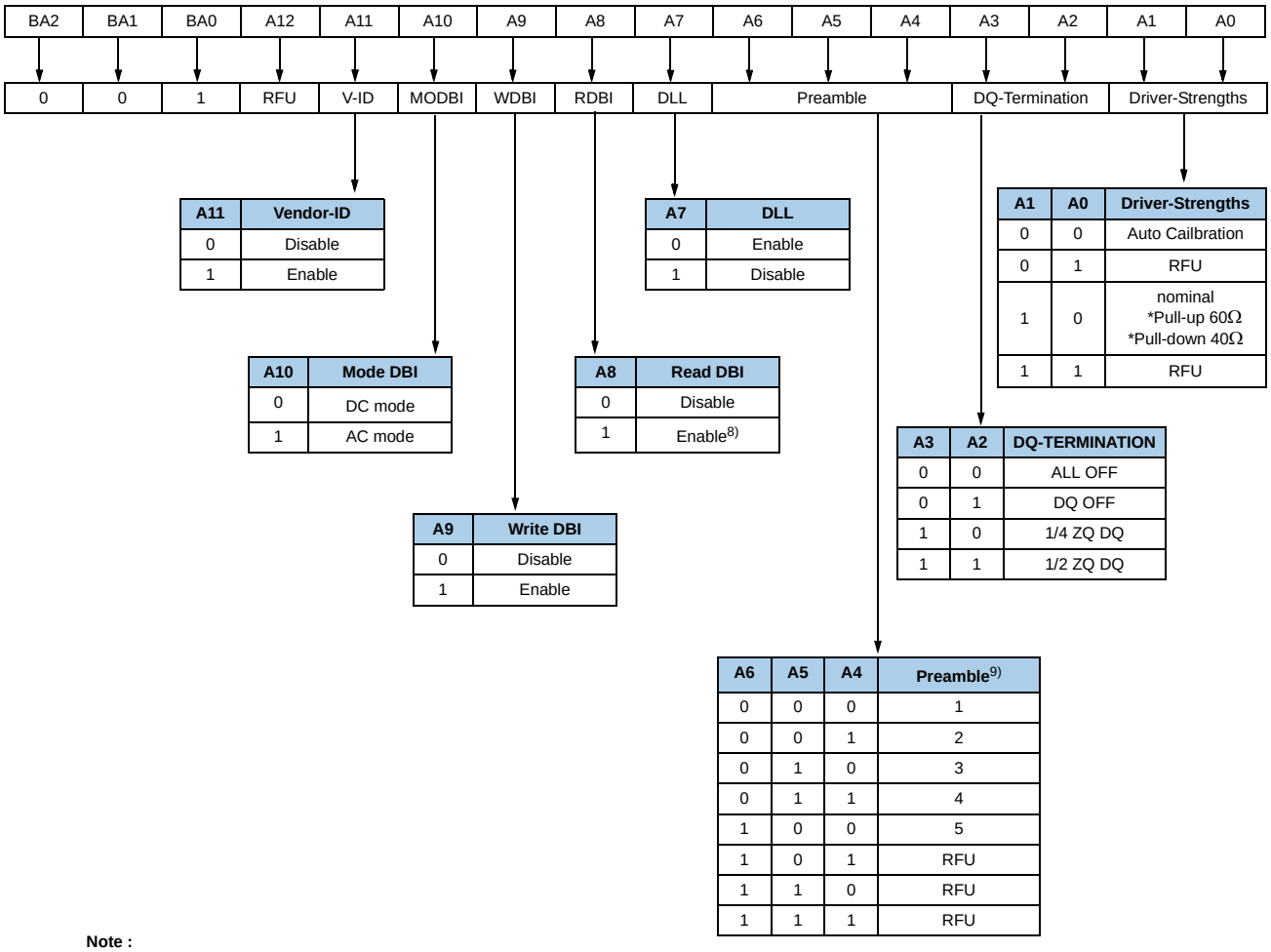
Data Termination Disable Timing



Note :

1. 16MX32 GDDR4 SGRAM doesn't support a Multi-preamble during DLL off Mode.

7.4 Extended Mode Register(EMRS1)



A11	Vendor-ID
0	Disable
1	Enable

A7	DLL
0	Enable
1	Disable

A1	A0	Driver-Strengths
0	0	Auto Cailbration
0	1	RFU
1	0	nominal *Pull-up 60Ω *Pull-down 40Ω
1	1	RFU

A10	Mode DBI
0	DC mode
1	AC mode

A8	Read DBI
0	Disable
1	Enable[8)]

A3	A2	DQ-TERMINATION
0	0	ALL OFF
0	1	DQ OFF
1	0	1/4 ZQ DQ
1	1	1/2 ZQ DQ

A9	Write DBI
0	Disable
1	Enable

A6	A5	A4	Preamble[9)]
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

Note :

1. The maximum number of preamble cycles over clock frequency which is supported by the GDDR4 SGRAM for Read commands .
2. The Auto Calibration option enables the Auto- Calibration functionality of the DRAM which controls the Pull-down, Pull-up Driver Strength and the Termination over process, temperature and voltage changes. The nominal option enables the factory setting for the Pull-down, Pull-up Driver-Strength and for the Termination. The design target for the factory setting is 40Ω Pulldown, 60Ω Pullup-Driver-Strength and 60Ω/120Ω for DQ-Termination, 60Ω/120Ω/240Ω for CMD/ADD-Termination with nominal process, voltage and temperature conditions. With the nominal option enabled Driver-Strength and Termination is expected to change with process, voltage and temperature variations.
3. If A3A2 is set 00 all DQ, DQS, DM, RDQS, WDQS and Command, Address terminators on the device are disabled. If A3A2 is set 01 all DQ, DQS,DM, RDQS, WDQS Terminations are switched off but Command, Address terminators are still enabled.
4. The LPTERM mode is only valid if A3A2 is either 10 or11.
5. Option ZQ/4 and ZQ/2 determine the target value of all DQ, DQS, DM. RDQS and WDQS terminations. If the Driver-Strengths/Termination settings.
6. From the low to high transition of the RESET signal A3A2 is set to either a 01, 10 or 11 and LPTERM mode disabled to assure address/command termination is enabled during initialization.
7. AC timings are only guaranteed with Auto Calibration.
8. 512M GDDR4 must be added 2clk to normal CL before using the Read of DBIdc.
   CL of DBIdc = Normal operation CL + 2.
9. Refer to the page 13.

DATA TERMINATION

The Data Termination is used to determine the value of the internal data termination resisters. The GDDR4 SGRAM supports 60Ω and 120Ω termination. The termination may also be disabled for testing and other purposes.

DATA DRIVER IMPEDANCE

The Data Driver impedance is used to determine the value of the data drivers impedance. When autocalibration is used the data driver impedance is set to pull-up 60Ω and pull-down 40Ωs and it's tolerance is determined by the calibration accuracy of the device. When any other value is selected the target impedance is set nominally to the desired impedance. However, the accuracy is now determined by the device's specific process corner, applied voltage and operating temperature.

PROGRAMMABLE IMPEDANCE OUTPUT BUFFER AND ACTIVE TERMINATOR

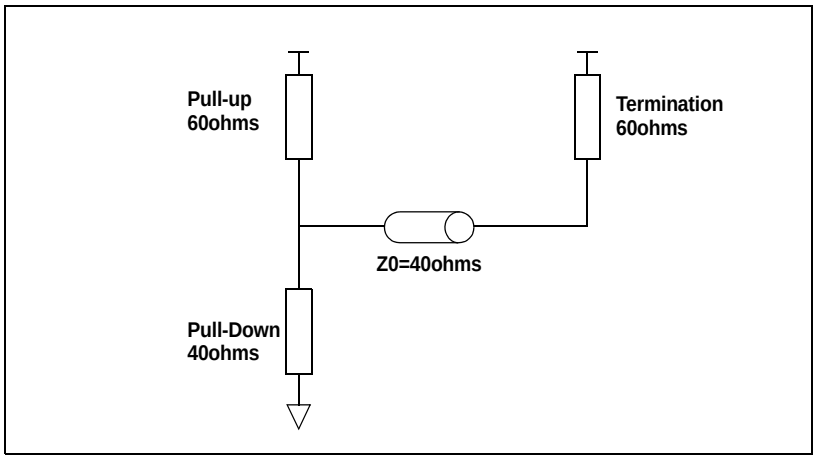
The GDDR4 SGRAM is equipped with programmable impedance output buffers and Active Terminators. This allows a user to match the driver impedance to the system. To adjust the impedance, an external precision resistor(RQ) is connected between the ZQ pin and Vss. The value of the resistor must be six times of the desired output impedance.
For example, a 240Ω resistor is required for an output impedance of 40 Ω. To ensure that output impedance is one sixth the value of RQ (within 10 %), the range of RQ is 120Ω to 360Ω (20Ω to 60Ω) output impedance.

MF,SEN, RESET, CK and $\overline{CK}$ are not internally terminated. CK and $\overline{CK}$ will be terminated on the system module using external 1% resisters. The output impedance is updated during all AUTO REFRESH commands and NOP commands when a READ is not in progress to compensate for variations in voltage supply and temperature. The output impedance updates are transparent to the system. Impedance updates do not affect device operation, and all data sheet timing and current specifications are met during update. To guarantee optimum output driver impedance after power-up, the GDDR4(x32) needs at least 20us after the clock is applied and stable to calibrate the impedance upon power-up. The user may operate the part with less than 20us, but the optimal output impedance is not guaranteed. The value of ZQ is also used to calibrated the internal address/command termination resisters. The two termination values that are selectable during power up are 1/2 of ZQ and ZQ. The value of ZQ is used to calibrate the internal DQ termination resisters. The two termination values that are selectable are 1/4 of ZQ and 1/2 of ZQ.

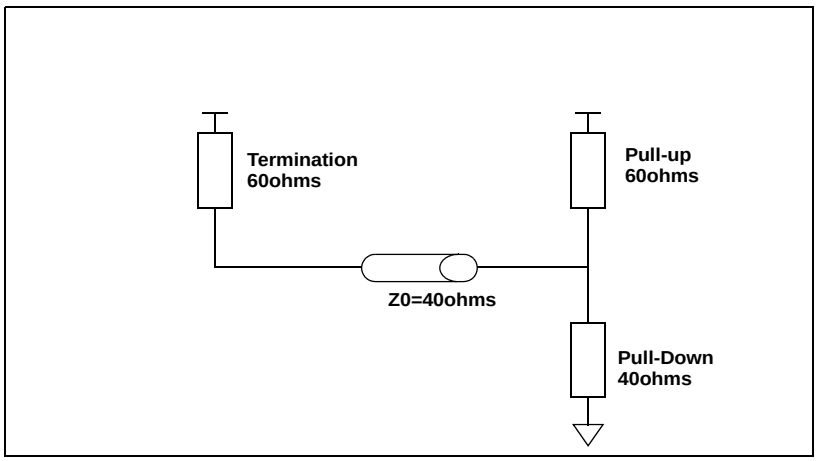
16MX32 GDDR4 SGRAM DRIVER TERMINATION

16MX32 GDDR4's driver and termination scheme.(IV-curve will be planced on the separately as an independant item)

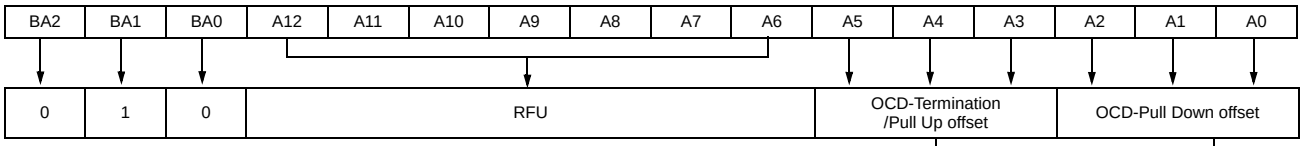
READ



WRITE



7.5 Extended Mode Register2(EMRS2)



A5	A4	A3	OCD Termination /Pull Up offset
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A5	A4	A3	OCD Pull down offset
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

Note : 1 . With negative offset steps the Driver Strength will be decreased and the Ron will be increased. With positive offset steps the Driver Strength will be increased and Ron will be decreased. With negative offset steps the Termination value will be increased. With positive offset steps the Termination value will be decreased.
2 . The Termination offset steps will be also applied to the Pull-up Driver Strength settings.
3 . IV curves and AC timings are only guaranteed with zero offset.
4 . Pull up offset controls both OCD and ODT.

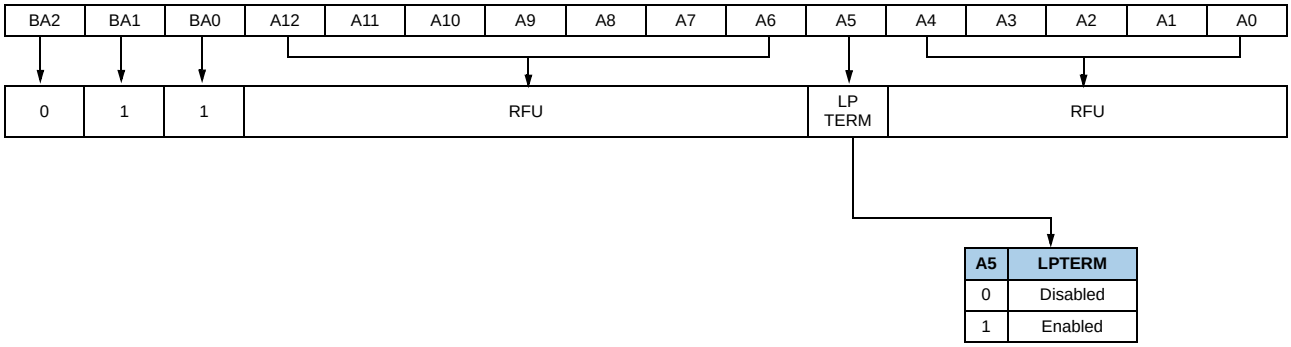
GDDR4 SGRAM Offset Control for driver and termination

GDDR4 SGRAM's DQ Ron Pull-down and DQ Ron Pull-up/Termination which makes it possible to adjust termination impedance and driver impedance within the range of Ron by 7 steps where + means increasing driver/termination strength, - means decreasing driver/ termination strength.

A5	A4	A3	OCD Termination /Pull up offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

A2	A1	A0	OCD Pull-down offset
0	0	0	0
0	0	1	+1
0	1	0	+2
0	1	1	+3
1	0	0	-4
1	0	1	-3
1	1	0	-2
1	1	1	-1

7.6 Extended Mode Register3(EMRS3)



A5	LPTERM
0	Disabled
1	Enabled

Note : 1 . For LPTERM mode the user has to make sure that the input timing is met. With LPTERM mode enabled the output timing is not guaranteed by comparison with nomal operation conditions.
2 . If the user activates bits in the extended mode register in an optional field, either the optional field is activated (if option is implemented in the device) or no action is taken by the device (if option is no implemented)

16MX32 GDDR4 SGRAM adds a low power mode to reduce power consumed for I/O termination by disabling the termination for a subset of the pins. This feature is available during normal operation but requires the memory controller meet the device specifications by operating at a reduced frequency. Absolute frequencies supported by the GDDR4 SGRAM are vendor specific.

Cortrol of the Low power mode is accomplished through the mode register field defined in Table 1. The Low Power Termination mode can only be enabled when DQ termination is enabled in the ZQ/2 or ZQ/4 mode.

Table 1: Low Power Termination Control

A5	**LPTERM**
0	Disabled
1	Enabled

Table 2 defines the termination states for the each signal group. The value EMRST[Termination] is meant to reference the value defined in the EMRS register for the state of ODT termination for actual termination impedance.

Table 2: Termination Support

Signal Group	LPTERM Disabled	LPTERM Enabled
CLK, $\overline{\text{CLK}}$	N/A	N/A
Address	Enabled	Disabled
$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{CS}}$	Enabled	Disabled
$\overline{\text{CKE}}$	Enabled	Disabled
RDQS[3:0]	EMRS[Termination]	Disabled
WDQS[3:0]	EMRS[Termination]	EMRS[Termination]
DQ[31:0], DM[3:0]	EMRS[Termination]	Disabled

7.7 Mirror Function

The GDDR4 SGRAM provides a mirror function (MF) ball to change the physical location of the control lines and all address lines which helps to route devices back to back. The MF ball will affect $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$ and $\overline{CKE}$ on balls H2, G4, H10, G9 and H3 respectively and A10/A0, BA0/A1, A12/A2, A11/A3, A8/A4, BA1/A5, BA2/A6, A9/A7 on balls K2, H4, K3, L4, K11, H9, K10, L9 respectively and only detects a DC input. The MF ball should be tied directly to VSS or VDD depending on the orientation of SGRAMcontrol line desired. When the MF ball is tied low, the orientaion of ball is as follows, $\overline{RAS}$ - H2, $\overline{CAS}$ - G4, $\overline{WE}$ - H10, $\overline{CS}$ - G9, $\overline{CKE}$ - H3, A10/A0 - K2, BA0/A1 - H4, A12/A2 - K3, A11/A3 - L4, A8/A4 - K11, BA1/A5 - H9, BA2/A6 - K10, A9/A7 - L9. The high state of the MF ball will change the location of the control balls as follows; $\overline{RAS}$ - H11, $\overline{CAS}$ - G9, $\overline{WE}$ - H3, $\overline{CS}$ - G4, $\overline{CKE}$ - H10, A10/A0 - K11, BA0/A1 - H9, A12/A2 - K10, A11/A3 - L9, A8/A4 - K2, BA1/A5 - H4, BA2/A6 - K3, A9/A7 - L4.

Mirror Function Signal Mapping

PIN	MF LOGIC STATE	
	HIGH	LOW
$\overline{RAS}$	H11	H2
$\overline{CAS}$	G9	G4
$\overline{WE}$	H3	H10
$\overline{CS}$	G4	G9
$\overline{CKE}$	H10	H3
A10/A0	K11	K2
BA0/A1	H9	H4
A12/A2	K10	K3
A11/A3	L9	L4
A8/A4	K2	K11
BA1/A5	H4	H9
BA2/A6	K3	K10
A9/A7	L4	L9

7.8 Manufacturers Vendor Code and Revision Identification

The Manufacturers Vendor Code, V, is selected by issuing a EXTENDED MODE REGISTER SET command with bits A11 set to one, and bits A0-A10 and A12 set to the desired values. When the V-ID function is enabled the GDDR4 SGRAM will provide its manufacturers vendor code on DQ[3:0] and revision identification on DQ[7:4]. The code will be driven onto the DQ bus after the EMRS that set A11 to 1. The DQ bus will be continously to driven until a EMRS write sets A11 back to 0. The DQ bus will be in a Hi-Z state after tWIDOFF max. The code can be sampled by the controller after waiting tWRIDON max and before tWRIDOFF min.

TABLE 1. AC Timing Parameters (Note : Table 1 is for reference only)

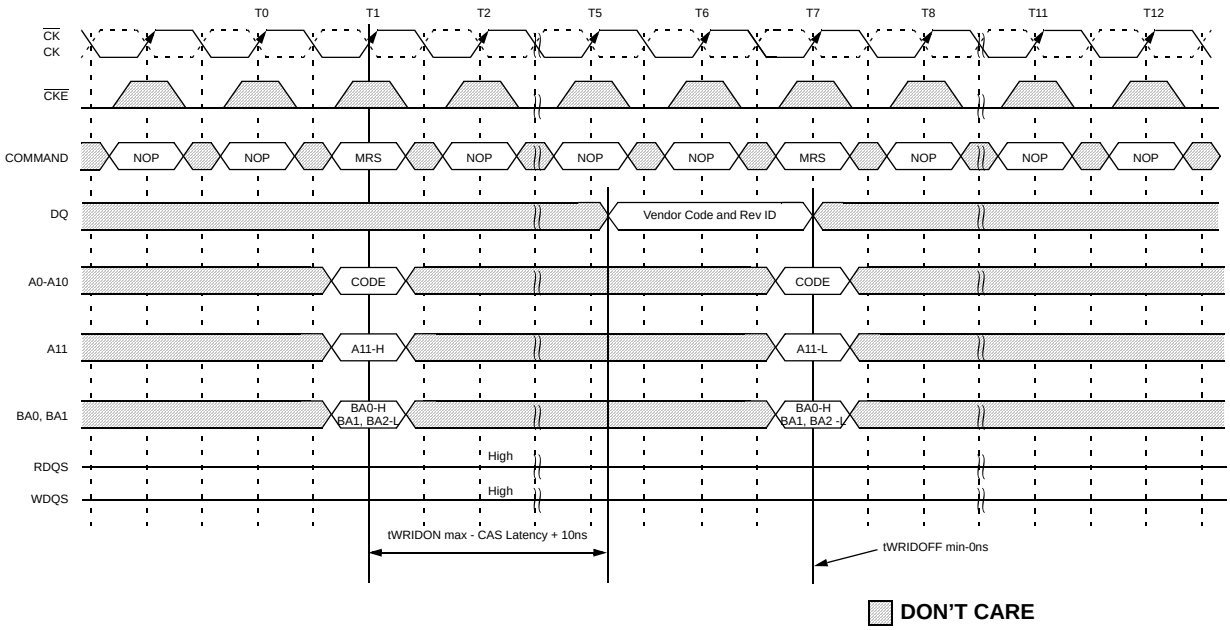
Parameter	Min	Max
tWRIDON	0ns	CL + 10ns
tWRIDOFF	0ns	CL + 10ns

Manufacturer	DQ[3:0]
Reserved	0
Samsung	1
Infineon	2
Elpida	3
Etron	4
Nanya	5

Manufacturer	DQ[3:0]
Hynix	6
Mosel	7
Winbond	8
ESMT	9
Reserved	A
Reserved	B

Manufacturer	DQ[3:0]
Reserved	C
Reserved	D
Reserved	E
Micron	F

Revision ID	DQ[7:4]
E-die	0000



7.9 multiplexed addresses

The address should be provided to the GDDR4 SGRAM in two parts that are latched into the memory with two consecutive clock edges. Command protocols incorporating such as CS, RAS, CAS and WE should be issued at the first rising edge of the clock and the half of addresses will be registered along with command inputs. Following this cycle, the remaining half of addresses will be registered at the rising edge of the clock.

The commands such as Row activation, READ, READ with auto-precharge, WRITE, WRITE with auto precharge, Precharge, Pre-charge all, Load mode register, Auto-refresh ans Self-refresh would require two consecutive clocks to fulfill single task. Only NOP command can be registered at single clock cycle. The clock reference for the AC timing is defined as the first rising edge of the clock.

It is prohibited to issue any other command at the second clock cycle which has been reserved for the second half of the addresses. Just only issue NOP at the second clock cycle for the preceding command.

Figure1. Command Sets with Multiplexed Addresses

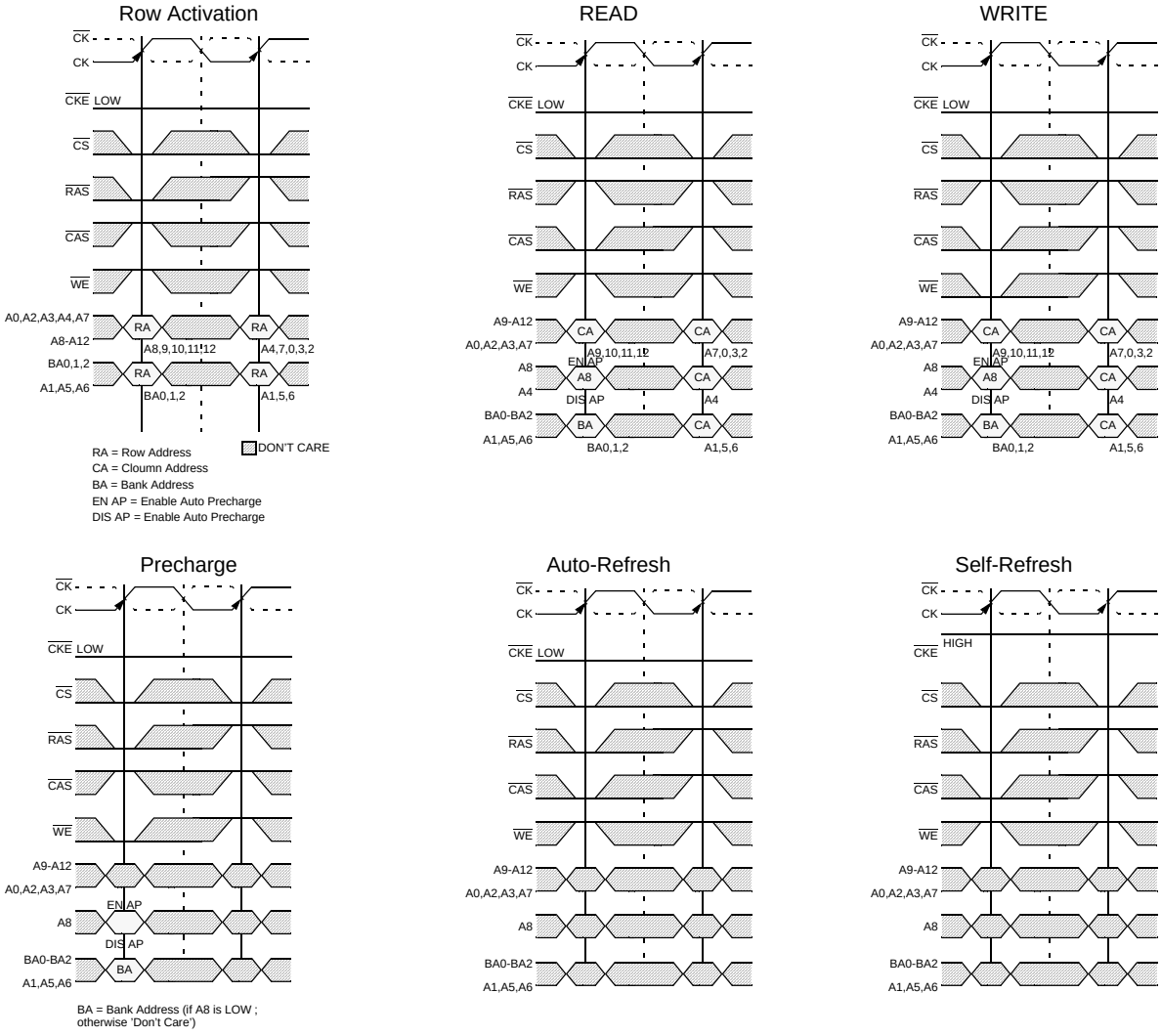


Table1. Address pair

CLOCK								
First	BA2	BA1	BA0	A12	A11	A10	A9	A8
Second	A6	A5	A1	A2	A3	A0	A7	A4

7.10 Clock frequency change sequence during device operation

1

Detail recommended sequence (100Mhz DLL off/ODT off -> 400Mhz DLL on/ODT on)

1) Issue EMRS with ODT on & DLL off at 100Mhz
2) Change frequency from 100Mhz to 400Mhz
3) Precharge all banks
4) Issue EMRS with ODT on & DLL on at 400Mhz
5) Issue MRS with valid mode and without DLL reset
6) Precharge all banks
7) Issue 2 times of auto-precharge
8) Wait 20tCK for the DLL locking

** Above sequence must follow spec. timing(ex, tRP, tMRD)

2

Detail recommended sequence (500Mhz DLL on -> 100Mhz DLL off and ODT off)

1) Issue EMRS with DLL off and ODT ON at 500Mhz
2) Change frequency from 500Mhz to 100Mhz
3) Precharge all banks
4) Issue EMRS with DLL off and ODT off at 100Mhz
5) Issue MRS with valid mode and without DLL reset
6) Precharge all banks
7) Issue 2 times of auto-precharge
8) Normal access to memory

** Above sequence must follow spec. timing(ex, tRP, tMRD)

3

Detail recommended sequence (100Mhz DLL off -> 125Mhz DLL off)

1) Change frequency from 100Mhz to 125Mhz
2) Precharge all banks
3) Issue EMRS with DLL off and ODT off at 200Mhz
4) Issue MRS with valid mode and without DLL reset
5) Precharge all banks
6) Issue 2 times of auto-precharge
7) Normal access to memory

** Above sequence must follow spec. timing (ex, tRP, tMRD)

Changing Clock Frequency

Clock Frequency Change Sequence-Auto Refresh(ARF) commands

1) Wait until all commands have finished, all banks are idle.
2) Only NOP or DESELECT or AREF commands may be issued (must meet setup/hold relative to clock while clock is changing) to GDDR4 SGRAM for the entire sequence unless stated to do otherwise. AREF commands must fulfill AREF burst requirements.
3) If new clock period is between the range of tCK (Max DLL Off) to tCK (Min DLL Off), then turn DLL off via EMRS register write.
4) Change the clock frequency and wait until clock is stabilized.
5) If the DLL is enabled, then complete steps 6a and 6b:
6a) Reset the DLL by writing to the MRS register.
6b) Wait tDL clock cycles before issuing any commands to the GDDR4 SGRAM.
7) GDDR4 SGRAM is ready for normal operation.

Clock Frequency Change Sequence- NOP/ DESELECT commands

1) Wait until all commands have finished, all banks are idle.
2) Send NOP or DESELECT (must meet setup/hold relative to clock while clock is changing) to GDDR4 SGRAM for the entire sequence unless stated to do otherwise. The user must take are AREF requirements.
3) If new clock period is between the range of tCK(Max DLL Off) to tck (Min DLL Off), then turn DLL off via EMRS register write.
4) Change the clock frequency and wait until clock is stabilized.
5) If new clock period is smaller than tCK (Max DLL On), then turn DLL on via EMRS register write.
6) If the DLL is enabled, then complete steps 6a and 6b:
6a) Reset the DLL by writing to the MRS register.
6b) Wait tDL clock cycles before issuing any commands to the GDDR4 SGRAM.
7) GDDR4 SGRAM is ready for normal operation.

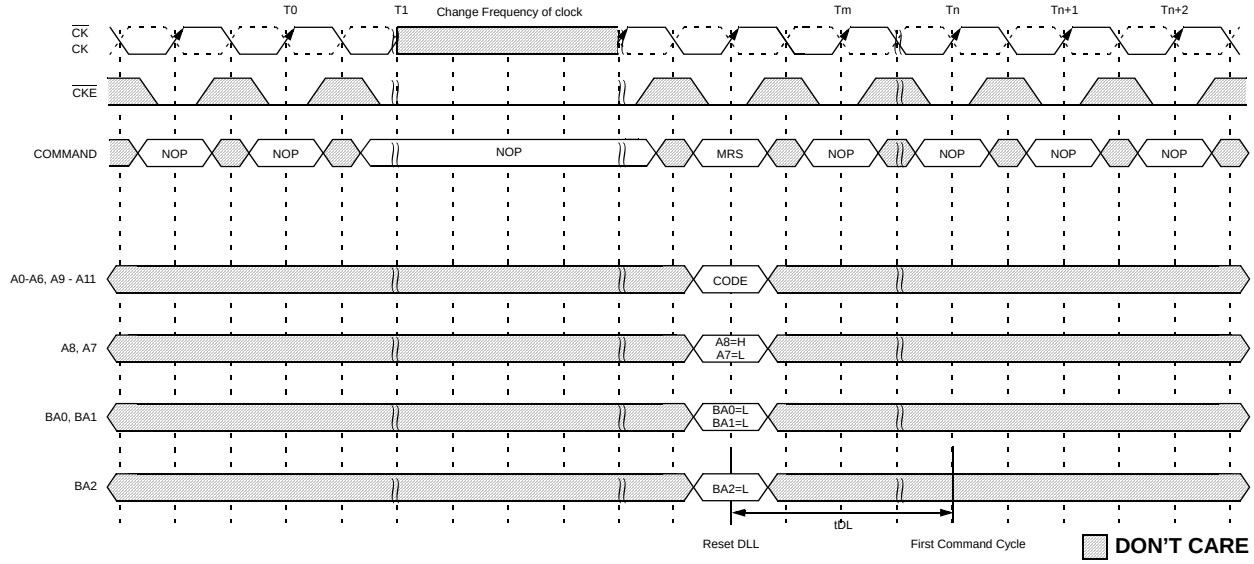


Figure : DLL is on and new frequency range DLL is on

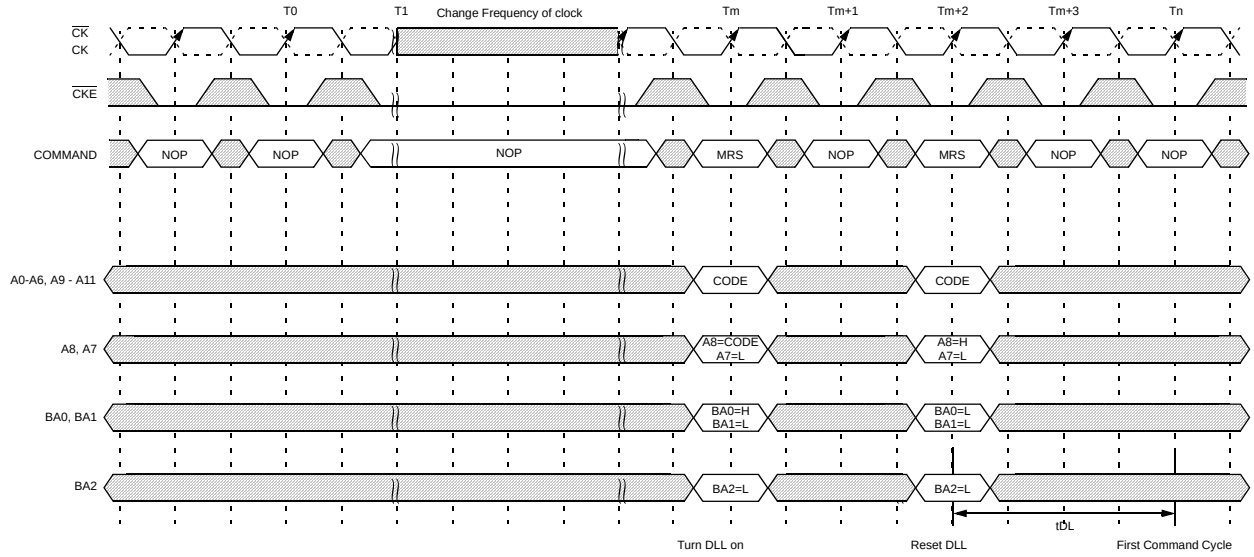


Figure : DLL is off and new frequency range DLL is on

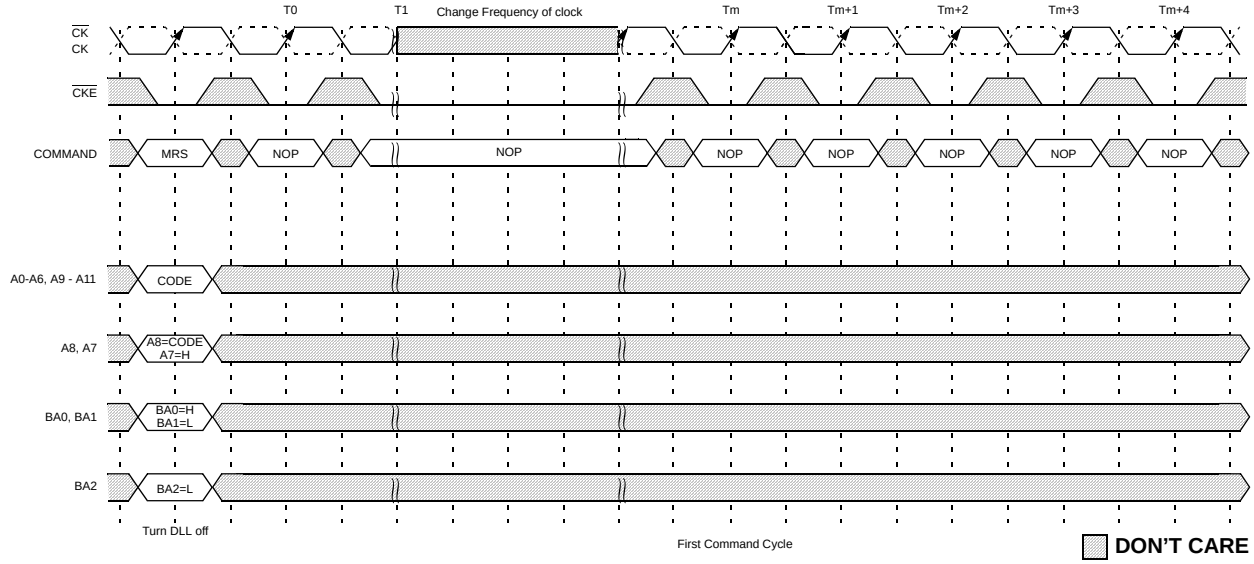


Figure : DLL is on and new frequency range DLL is off

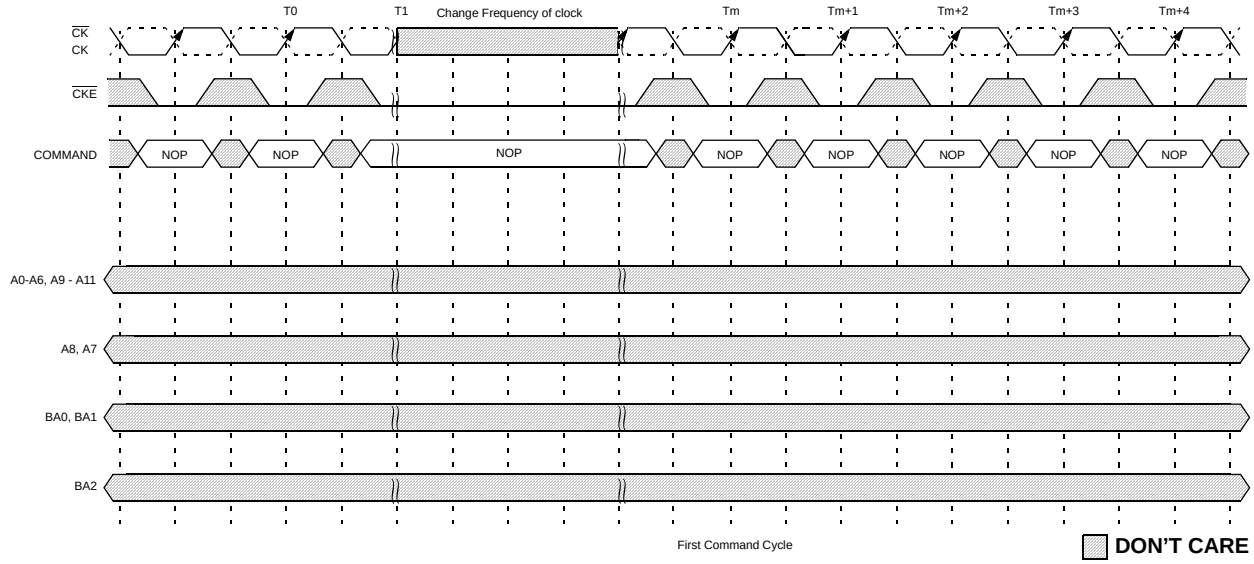


Figure : DLL is off and new frequency range DLL is off

7.11 BOUNDARY SCAN FUNCTION

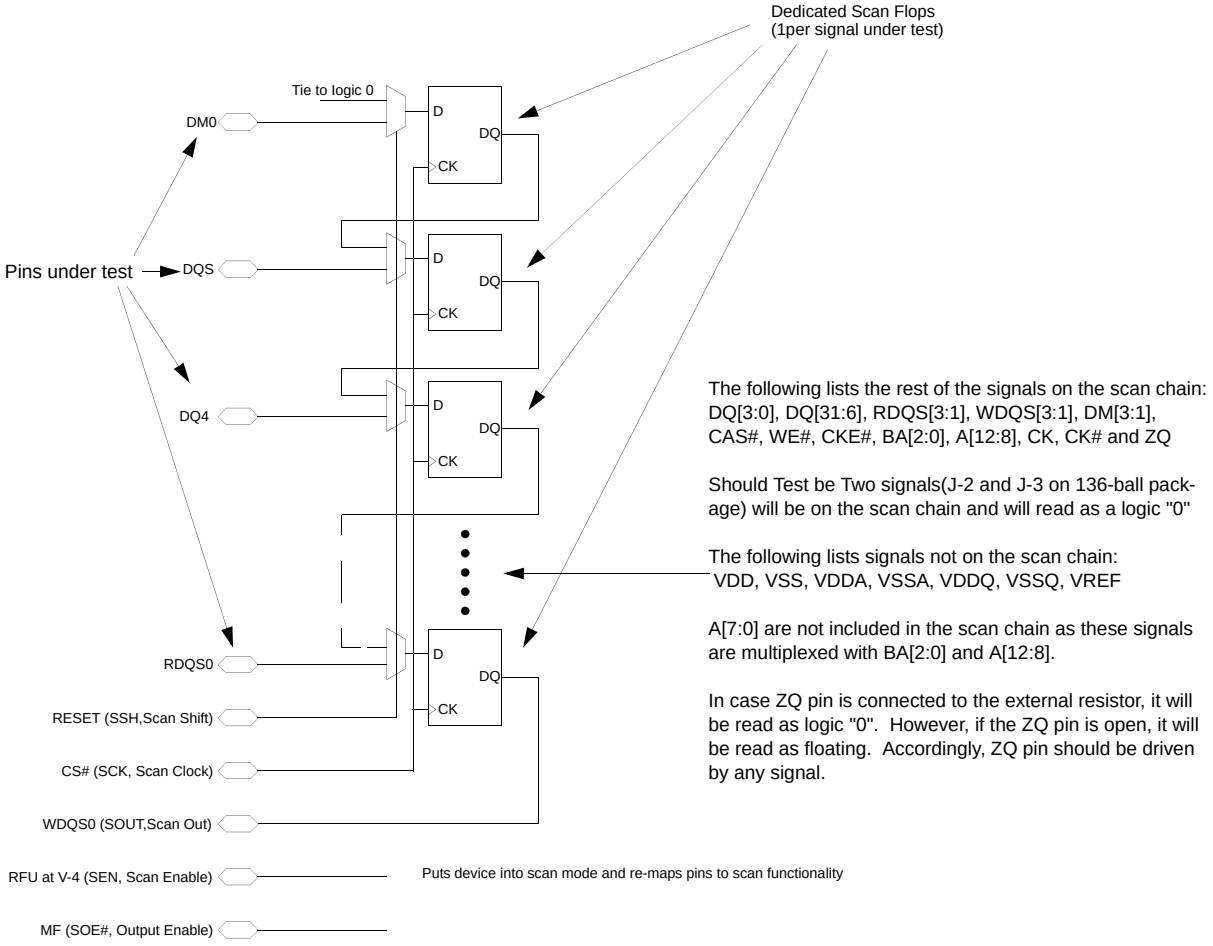
General Information

The GDDR4 incorporates a modified boundary scan test mode as an optional feature. This mode doesn't operate in accordance with IEEE Standard 1149.1 - 1990. To save the current GDDR4 ball-out, this mode will scan parallel data input and output and the scanned data through WDQS0 pin controlled by an add-on pin, SEN which is located at V-4 of 136 ball package.
For the normal device operation other than boundary scan, there required device re-initialization by device power-off and then power-on.

Disabling the Scan Feature

It is possible to operate the GDDR4 without using the boundary scan feature. SEN(at V-4 of 136 ball package) should be tied LOW(VSS) to prevent the device from entering the boundary scan mode. The other pins which are used for scan mode, RESET, MF, WDQS0 and CS# will be operating at normal GDDR4 functionalities when SEN is deasserted.

Figure 1. Internal Block Diagram (Reference Only)



BOUNDARY SCAN EXIT ORDER

BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL	BIT#	BALL
1	D-3	13	E-10	25	K-10	37	T-3	49	K-2	61	E-3
2	C-2	14	F-10	26	M-11	38	T-2	50	L-4		
3	C-3	15	E-11	27	L-10	39	R-3	51	J-3		
4	B-2	16	G-10	28	N-11	40	R-2	52	J-2		
5	B-3	17	F-11	29	M-10	41	P-3	53	H-2		
6	A-4	18	H-9	30	N-10	42	P-2	54	H-3		
7	B-10	19	H-10	31	P-11	43	N-3	55	H-4		
8	B-11	20	H-11	32	P-10	44	M-3	56	G-4		
9	C-10	21	J-11	33	R-11	45	N-2	57	F-2		
10	C-11	22	J-10	34	R-10	46	L-3	58	G-3		
11	D-10	23	L-9	35	T-11	47	M-2	59	E-2		
12	D-11	24	K-11	36	T-10	48	K-3	60	F-3		

Note :
1. When the device is in scan mode, the mirror function is disabled and none of the pins are remapped.
2. Since the other input of the MUX for DM0 is tied to GND, the device will continuously output zeros after scanning a bit #61, if the chip stays in scan shift mode.

SCAN PIN DESCRIPTION

Package Ball	Symbol	Normal Function	Type	Description
V-9	SSH	RESET	Input	Scan shift. Capture the data input from the pad at logic LOW and shift the data on the chain at logic HIGH.
G-9	SCK	CS#	Input	Scan Clock. Not a true clock, could be a single pulse or series of pulses. All scan inputs will be referenced to rising edge of the scan clock.
D-2	SOUT	WDQS0	Output	Scan Output.
V-4	SEN	RFU	Input	Scan Enable. Logic HIGH would enable the device into scan mode and will be disabled at logic LOW. Must be tied to GND when not in use.
A-9	SOE#	MF	Input	Scan Output Enable. Enables (registered LOW) and disables (registered HIGH) SOUT data. This pin will be tied to VDD or GND through a resistor (typically 1K Ω) for normal operation. Tester needs to overdrive this pin to gurarantee the required input logic level in scan mode.

Note :
1. When SEN is asserted, no commands are to be executed by the GDDR4. This applies to both user commands and manufacturing commands which may exist while RESET is deasserted.
2. All scan functionalities are valid only after the appropriate power-up and initialization sequesnce. (RESET,CKE#,A0 to set the ODT of the C/A)
3. In scan mode, the ODT for the address and control lines set to a nominal termination value of ZQ. The ODT for DQ's will be disabled. It is not necessary for the termination to be calibrated.
4. In a double-load clam-shell configuration, SEN will be asserted to both devices. Two Separate SOE#'s should be provided to top and bottem devices to access the scanned output. When either of the devices is in scan mode, SOE# for the device not being scanned will be disabled.

Scan DC Electrical Characteristics and Operating Conditions

PARAMETER/CONDITON	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF}+0.15	-	V	1,2
Input Low (Logic 0) Voltage	V_{IL}(DC)	-	V_{REF}-0.15	V	1,2

Note : 1. The parameter applies only when SEN is asserted.
2. All voltages referenced to GND.

Figure 1. Scan Capture Timing

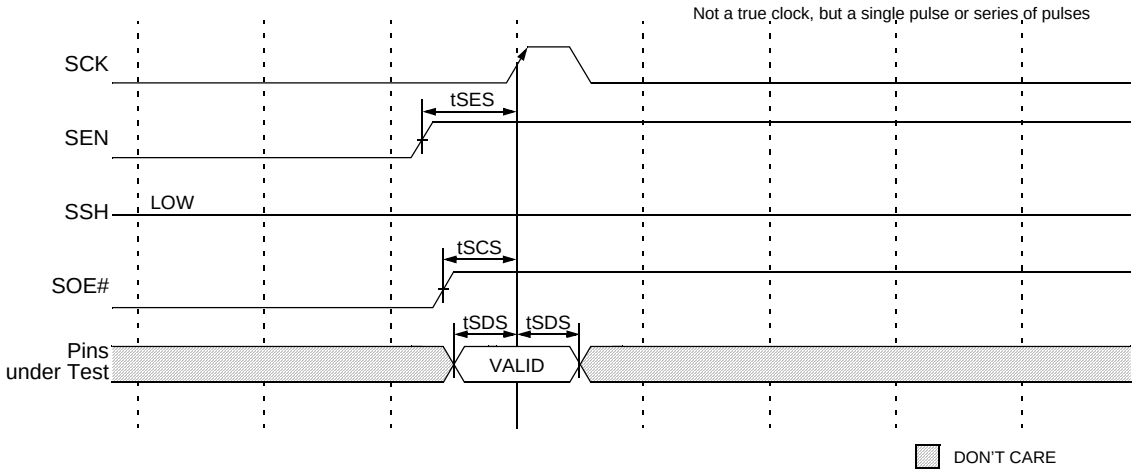


Figure 2.Scan Shift Timing

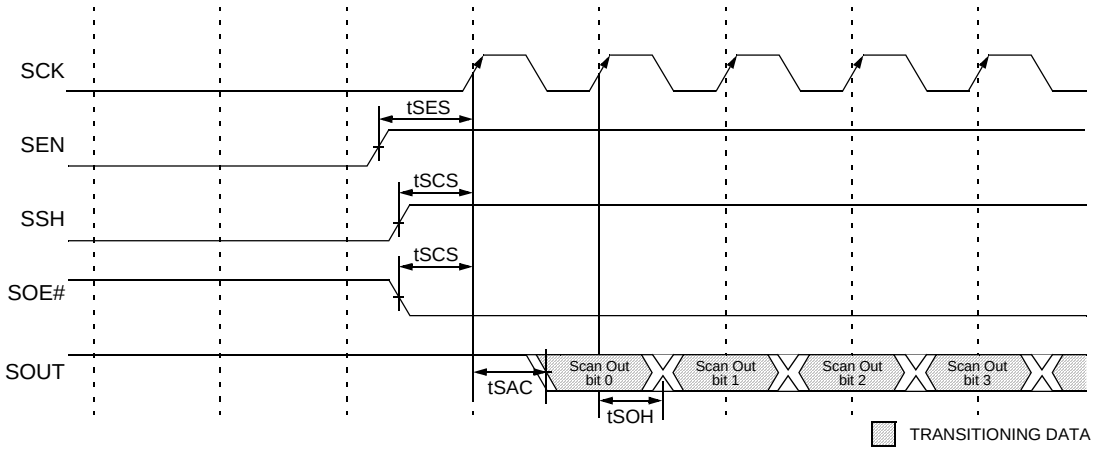
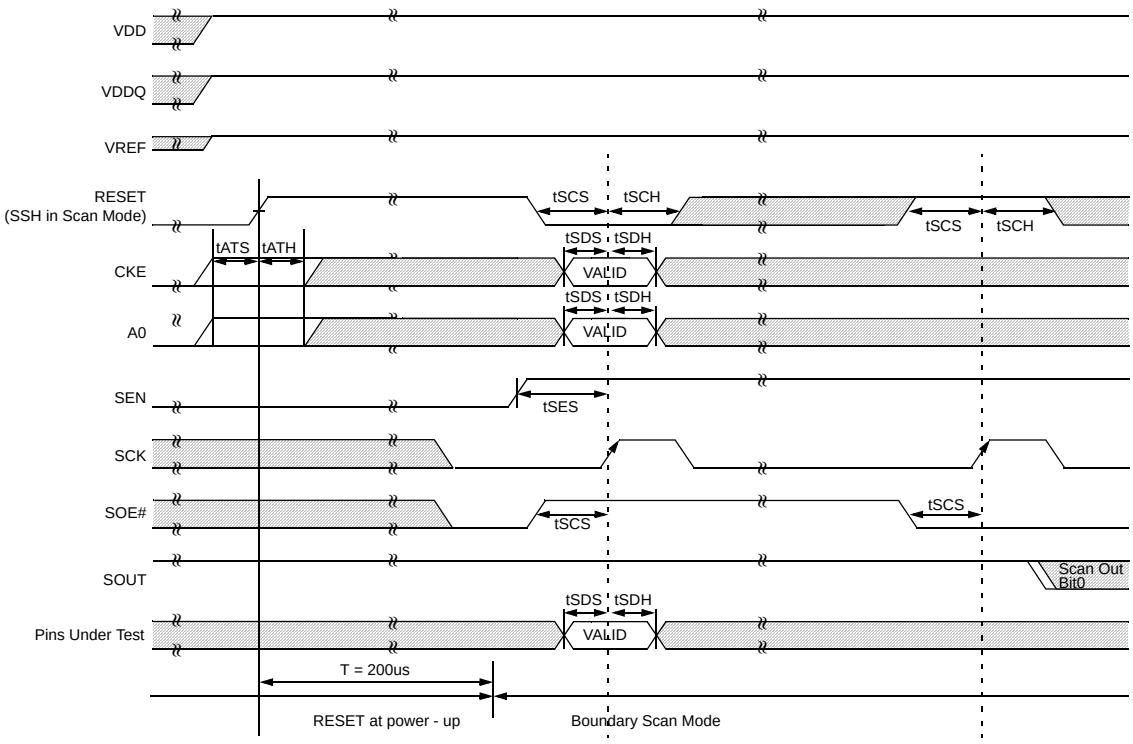


Table 4. Scan AC Electrical Characteristics

parameter/condition	symbol	min	max	units	notes
Clock					
Clock cycle time	tSCK	40	-	ns	1
Scan Command Time					
Scan enable setup time	tSES	20	-	ns	1, 2
Scan enable hold time	tSEH	20	-	ns	1
Scan command setup time for SSH, SOE# and SOUT	tSCS	14	-	ns	1
Scan command hold time for SSH, SOE# and SOUT	tSCH	14	-	ns	1
Scan Capture Time					
Scan capture setup time	tSDS	10	-	ns	1
Scan capture hold time	tSDH	10	-	ns	1
Scan Shift Time					
Scan clock to valid scan output	tSAC	-	6	ns	1
Scan clock to scan output hold	tSOH	1.5	-	ns	1

Note : 1. The parameter applies only when SEN is asserted.
2. Scan Enable should be issued earlier than other Scan Commands by 6ns.

Figure 1. Scan Initialization Sequence



Note : To set the pre-defined ODT for C/A, a boundary scan mode should be issued after an appropriate ODT initialization sequence with RESET and CKE# signals

7.12 Commands

Below Truth table-COMMANDs provides a quick reference of available commands. This is followed by a verbal description of each command. Two additional Truth Tables appear following the operation section : these tables provide current state/next state information.

Truth Table - Commands

NAME (FUNCTION)	CKE		$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	ADDR	NOTE
	Previous cycle	Current cycle						
DESELECT (NOP)	L	X	H	X	X	X	X	1, 7, 9
NO OPERATION (NOP)	L	X	L	H	H	H	X	1, 7
ACTIVE(Select bank & activate row)	L	L	L	L	H	H	Bank/Row	1, 3, 10
READ (Select bank and column, & start READ burst)	L	L	L	H	L	H	Bank/Col	1, 4, 10
WRITE (Select bank and column, & start WRITE burst)	L	L	L	H	L	L	Bank/Col	1, 4, 10
PRECHARGE (Deactivate row in bank or banks)	L	L	L	L	H	L	Code	1, 4, 5, 10
AUTO REFRESH	L	L	L	L	L	H	X	1, 6
SELF REFRESH ENTRY	L	H	L	L	L	H	X	1, 6
SELF REFRESH EXIT	H	L	H	X	X	X	X	1, 6
			L	H	H	H	X	1, 6
POWER DOWN ENTRY	L	H	H	X	X	X	X	1
			L	H	H	H	X	1
POWER DOWN EXIT	H	L	H	X	X	X	X	1
			L	H	H	H	X	1
LOAD MODE REGISTER(LMR)	L	L	L	L	L	L	Op-Code	1, 2, 10
DATA TERMINATOR DISABLE	L	L	H	H	L	H	X	1, 8

TRUTH TABLE - DM Operation

Name (Function)	DM	DQS	Note
Write Enable	L	Valid	
Write Inhibit	H	X	10

Note :

1. H=Logic High Level; L=Logic Low Level; X=Don't care.
2. BA0-BA2 select either the mode register or the extended mode register (BA0 = 0, BA1 = 0, BA2 = 0 select the mode register ; BA0 = 1, BA1 = 0, BA2 = 0 select extended mode register BA0 = 0, BA1 = 1, BA2 = 0 select extended mode register 2 ; BA0 = 1 , BA1 = 0, BA2 = 0 select extended mode register 3 ; other combinations of BA0 - BA2 are reserved). A0-A12 provide the op-code to be written to the selected mode register.
3. BA0-BA2 provide bank address and a0-a11 provide row address.
4. BA0-BA2 provide bank address; A0-A7 and A9-A10 provide column address; A8 HIGH enables the auto precharge feature (nonpersistent), and A8 LOW disables the auto precharge feature.
5. A8 LOW : BA0-BA2 determine which bank is precharged.
   A8 HIGH : all banks are precharged and BA0-BA2 are "Don't Care."
6. Internal refresh counter controls row addressing; all inputs and I/Os are "Don't Care' except for $\overline{CKE}$.
7. DESELECT and NOP are functionally interchangeable.
8. Used for bus snooping when the DQ termination is set to ZQ/2 in the EMRS and cannot be used during power-down or self refresh.
9. The decode of the DESELECT command excludes the Data Terminator Disable command.
10. Address is received on two consecutive rising edges of CK

DESELECT

The DESELECT function (/CS high) prevents new commands from being executed by the GDDR4(x32). The GDDR4(x32) SGRAM is effectively deselected. Operations already in progress are not affected.

NO OPERATION (NOP)

The NO OPERATION (NOP) command is used to instruct selected GDDR4(x32) to perform a NOP ($\overline{CS}$ LOW). This prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

LOAD MODE REGISTER

The mode registers are loaded via inputs A0-A11. See mode register descriptions in the Register Definition section. The Load Mode Register command can only be issued when all banks are idle, and a subsequent executable command cannot be issued until tMRD is met.

ACTIVE

The ACTIVE command is used to open (or activate) a row in a particular bank for a subsequent access. The value on the BA0, BA1 and BA2 inputs select the bank, and the address provided on inputsA0-A11 selects the row. This row remains active (or open) for accesses until a PRECHARGE command is issued to that bank. A PRECHARGE command must be issued before opening a different row in the same bank.

READ

The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 and BA2 inputs select the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on input A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the READ burst; if auto precharge is not selected, the row will remain open for subsequent accesses.

WRITE

The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 and BA2 inputs select the bank, and the address provided on inputs A0-A7, A9 selects the starting column location. The value on inputs A8 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be precharged at the end of the WRITE burst; if auto precharge is not selected, the row will remain open for subsequent accesses. Input data appearing on the DQs is written to the memory array subject to the DM input logic level appearing coincident with the data. If a given DM signal is registered LOW. the corresponding data will be written to memory; If the DM signal is registered HIGH, the corresponding data inputs will be ignored, and a WRITE will not be executed to that byte/column location.

PRECHARGE

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access a specified time (t_{RP}) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one banks are to be precharged, inputs BA0,BA1 and BA2 select the bank. Otherwise BA0, BA1 and BA2 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE command will be treated as a NOP if there is no open row is already in the process of precharging.

AUTO PRECHARGE

Auto precharge is a feature which performs the same individual-bank precharge function described above, but without requiring an explicit command. This is accomplished by using A8 to enable auto precharge in conjunction with a specific READ or WRITE command. A precharge of the bank/row that is addressed with the READ or WRITE command is automatically performed upon completion of the READ or WRITE burst. Auto precharge is nonpersistent in that it is either enable or disabled for each individual READ or WRITE command. Auto precharge ensures that the precharge is initiated at the earliest valid state within a burst. This "earliest valid stage" is determined as if an explicit PRECHARGE command was issued at the earliest possible time, without violating $t_{RAS(min)}$, as described for each burst type in the Operation section of this data sheet. The user must not issue another command to the same bank until the precharge time(t_{RP}) is completed.

AUTO REFRESH

Auto Refresh is used during normal operation of the GDDR4 SGRAM and is analogous to $\overline{CAS}$-BEFORE-$\overline{RAS}$ (CBR) REFRESH in FPM/EDO DRAMs. This command is nonpersistent, so it must be issued each time a refresh is required. The addressing is generated by the internal refresh controller. This makes the address bits a "Don't Care" during an Auto Refresh command. The 16Mx32 GDDR4 requires Auto Refresh cycles at an average interval of 3.9us (maximum).

A maximum Auto Refresh commands can be posted to any given GDDR4 SGRAM, meaning that the maximum absolute interval between any Auto Refresh command and the next Auto Refresh command is 9 x 3.9us(35.1us). This maximum absolute interval is to allow GDDR4 SGRAM output drivers and internal terminators to automatically recalibrate compensating for voltage and temperature changes.

SELF REFRESH

The SELF REFRESH command can be used to retain data in the GDDR4 SGRAM ,even if the rest of the system is powered down. When in the self refresh mode,the GDDR4 SGRAM retains data without external clocking. The SELF REFRESH command is initiated like an AUTO REFRESH command except $\overline{CKE}$ is disabled (HIGH). The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH. The active termination is also disabled upon entering Self Refresh and enabled upon exiting Self Refresh. (20K clock cycles must then occur before a READ command can be issued). Input signals except $\overline{CKE}$ are "Don't Care" during SELF REFRESH. The procedure for exiting self refresh requires a sequence of commands. First, CK and $\overline{CK}$ must be stable prior to $\overline{CKE}$ going back LOW. Once $\overline{CKE}$ is LOW,the GDDR4 must have NOP commands issued for tXSNR because tine is required for the completion of any internal refresh in progress. A simple algorithm for meeting both refresh, DLL requirements and out-put calibration is to apply NOPs for 20K clock cycles before applying any other command to allow the DLL to lock and the output drivers to recalibrate.

DATA TERMINATION DISABLE (BUS SNOOPING FOR READ COMMAND)

The DATA TERMINATOR DISABLE COMMAND is detected by the device by snooping the bus for READ commands excluding $\overline{CS}$. The GDDR4 SGRAM will disable its Data terminators when a READ command is detected. The terminators are disable CL Clocks after the READ command is detected. In a two rank system both dram devices will snoop the bus for READ commands to either device and both will disable their terminators if a READ command is detected. The command and address terminators and always enabled.

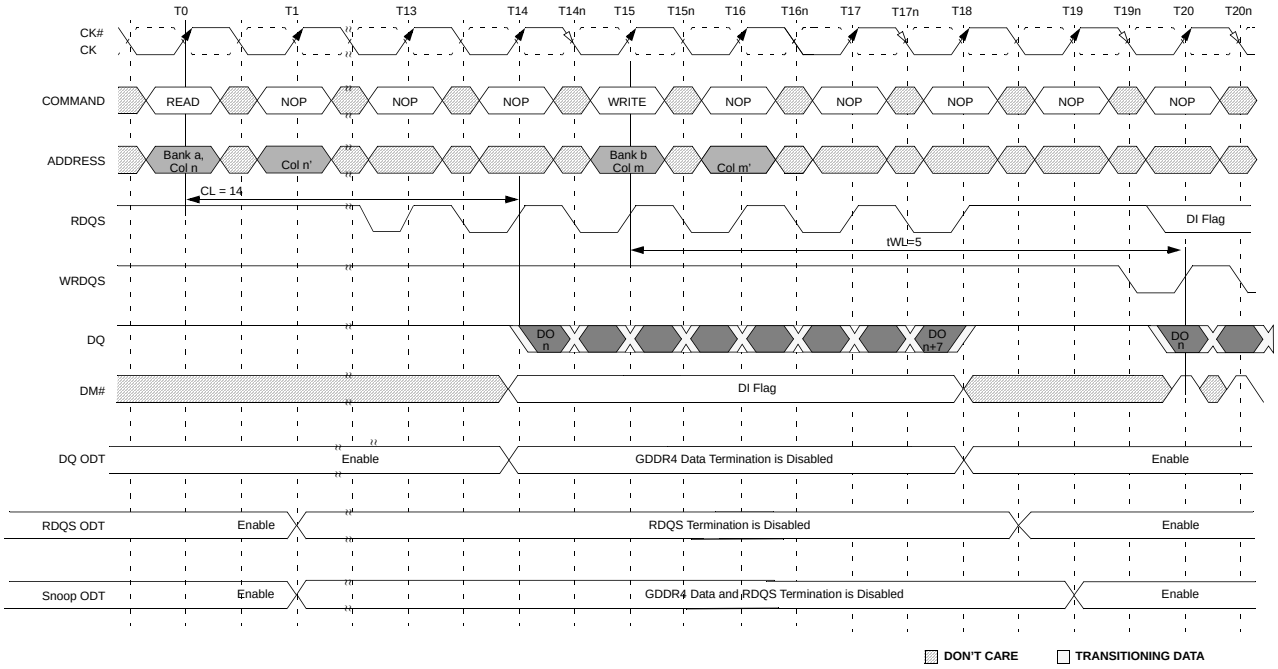
ON-DIE TERMINATION

In GDDR4 SGRAM there are two kinds of Termination control modes, READ and Bus snooping mode.
In READ mode the on-die termination for DQ pins are disabled CL clocks after the READ command and stays off for a duration of BL/2. The on-die termination for all other pins on the device are always on except RDQS pin. The on-die termination for RDQS pins are disabled CL-1 clocks after the READ command and stays off for a duration of BL/2+1.5(tCK).

In Bus snooping mode the on-die termination for DQ and RDQS pins are disabled CL-1 clocks after the Bus Snooping command and stays off for a duration of BL/2+2(tCK). The on-die termination for all other pins on the device are always on.

The on-die termination value on address and control pins is determined during power-up in relation to the state of $\overline{CKE}$ and A0 on the first transition of RESET. On the rising edge of RESET, if $\overline{CKE}$ and A0 are sampled LOW and LOW respectively, then the termination value is determined to be ZQ/4 for the address and command pins. On the rising edge of RESET, if $\overline{CKE}$ and A0 are sampled LOW and HIGH respectively, then the termination value is determined to be ZQ/2 for the address and command pins.
On the rising edge of RESET, if $\overline{CKE}$ and A0 are sampled HIGH and LOW respectively, then the termination value is determined to be ZQ for the address and command pins.

Data Termination Disable Timing



Note : RPRE=2 case is shown for an example. Actual supported RPRE numbers will be found in EMRS standard.

7.13 OPERATIONS

7.13.1 Bank/Row Activation

Before any READ or WRITE commands can be issued to a banks within the GDDR4 SGRAM, a row in that bank must be "opened." This is accomplished via the ACTIVE command, which selects both the bank and the row to be activated.

After a row is opened with an ACTIVE command, a READ or WRITE command may be issued to that row, subject to the t_{RCD} specification. $t_{RCD(min)}$ should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVE command in which a READ or WRITE command can be entered. For example, a t_{RCD} specification of 16ns with a 800MHz clock (1.25ns period) results in 12.8 clocks rounded to 13. This is reflected in below figure, which covers any case where $12<t_{RCD(min)}/t_{CK}\leq 13$.

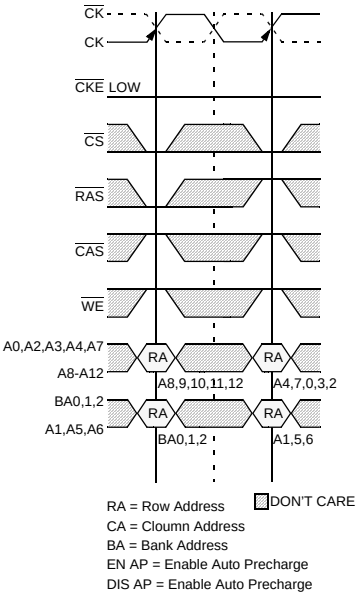
The same procedure is used to convert other specification limits from tome units to clock cycles).

A subsequent ACTIVE command to a different row in the same bank can only be issued after the previous active row has been "closed"(precharged). The minimum time interval between successive ACTIVE commads to the same bank is defined by t_{RC}.

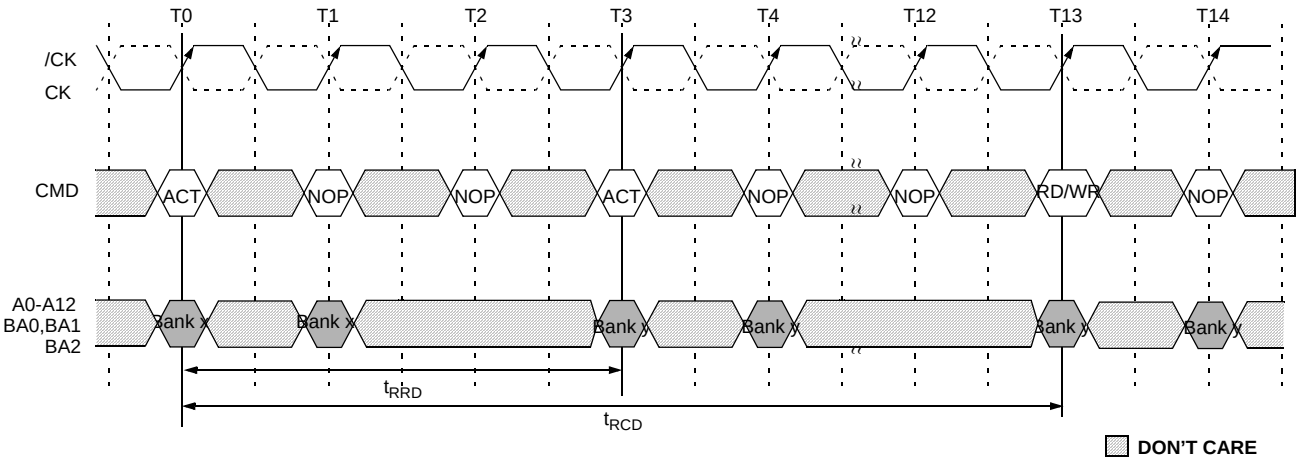
A subsequent ACTIVE command to another bank can be issued while the first bank is being accessed, which results in a reduction of total row access overhead. The minimum time interval between successive ACTIVE commands to different banks is defined by t_{RRD}.

* Any system or application incorporating random access memory products should be properly designed, tested and qualified to ensure proper use or access of such memory products. Disproportionate, excessive and/or repeated access to a particular address or addresses may result in reduction of product life.

Row Activation



Example : Meeting t_{RCD}



7.13.2 READs

READ bursts are initiated with a READ command, as below figure. The starting column and bank addresses are provided with the READ command and auto precharge is either enabled or disabled for that burst access. If auto precharge is enabled, the row being accessed is prechrged at the completion of the burst after $t_{RAS(min)}$ has been met. For the generic READ commands used in the following illustrations, auto precharge is disabled.

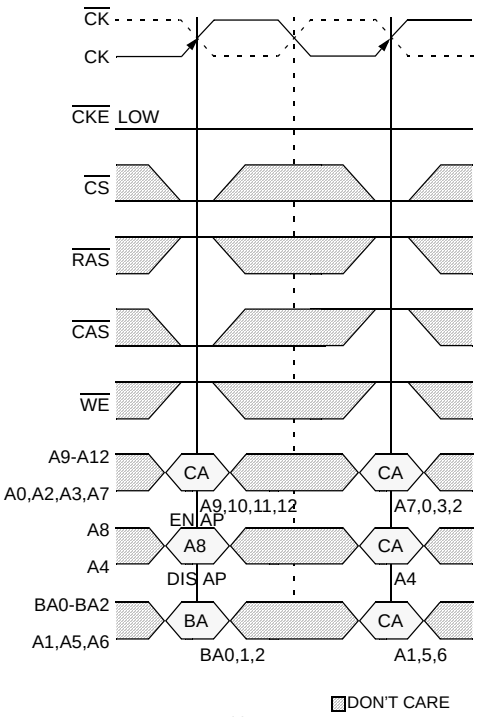
During READ bursts, the valid data-out element from the starting column address will be available following the CAS Latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive or negative strobe edge. READ burst figure shows general timing for 2 of the possible CAS latency settings. The GDDR4(x32) drives the output data edge aligned to the crossing of CK and /CK and to RDQS. The initial HIGH transitioning LOW of RDQS is known as the read preamble ; the half cycle coincident with the last data-out element is known as the read postamble.

Upon completion of a burst, assuming no other commands have been initiated, the DQs will go High-Z. A detailed explanation of t_{DQSQ} (valid data-out skew), t_{DV} (data-out window hold), the valid data window are depicted in Data Output Timing (1) figure. A detailed explanation of t_{AC} (DQS and DQ transition skew to CK) is shown in Data Output Timing (2) figure.

Data from any READ burst may be concatenated with data from a subsequent READ command. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued x cycles after the first READ command, where x equals the number of data element nibbles (nibbles are required by the 8*n*-prefetch architecture) depending on the burst length. This is shown in consecutive READ bursts figure. Nonconsecutive read data is shown for illustration in nonconsecutive READ bursts figure. Full-speed random read accesses within a page (or pages) can be performed as shown in Random READ accesses figure. Data from a READ burst cannot be terminated or truncated.

During READ commands the GDDR4 Dram disables its data terminators.

READ Commnad



GDDR4 SGRAM READ DATA TIMING

READ burst is initiated with a READ command.

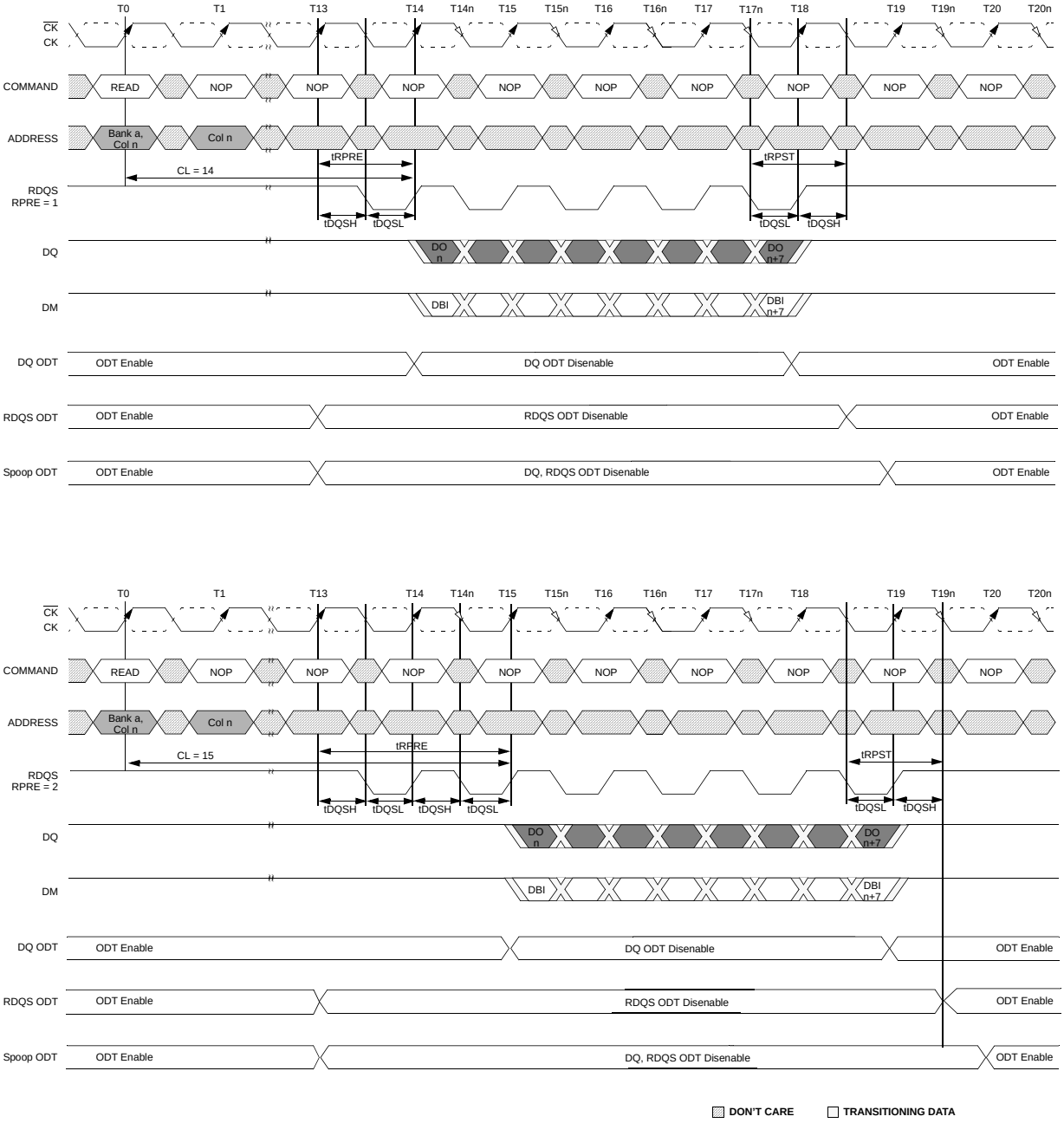
The starting colume and bank addresses are provided at the READ command and the following clock cycle, and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after tRAS min has been met.

During READ bursts, the first valid data-out element from the staring column address will be available following the CAS latency after the READ command. Each subsequent data-out element will be valid nominally at the next positive RDQS edge. The GDDR4 SGRAM drives the output data edge aligned to RDQS. And all outputs, i.e. DQs and RDQS, are also edge aligned to the clock. Prior to the first valid RDQS rising edge, a cycle is driven and specified as the READ preamble. The single preamble consists of half cycle High followed by a half cycle of Low driven by the GDDR4 SGRAM. For the multi-cycle preamble it should be set in extended mode register. The cycle on RDQS consisting of a half cycle Low coincident with the last data-out element followed by a half cycle High is known as the read postamble, and it will be driven by the SGRAM. The SGRAM toggles RDQS only when it is driving valid data on the bus. Upon completion of a burst, assuming no other command has been initiated; the DQs and RDQS will be in a Hi-Z state.

Data from any READ burst may be concatenated with data from a subsequent READ commmand. A continuous flow of data can be maintained. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued at least 4 cycles after the first READ command. A PRECHARGE can also be issued to the SGRAM with the same timing restriction as the new READ command if tRAS is met. A WRITE can be issued any time after a READ command as long as the bus turn around time is met. READ data cannot be truncated.

The data inversion flag is driven on the DM signal to identify whether the data is true or inverted data. If DM is HIGH, the data will be inverted and not inverted when it recognizes DM is LOW. READ Data Inversion can be programmed as a Disable(E8=0) or Enable (E8=1) in the extended mode. register 1.

Figure 1. READ Command



Note : RPRE=2 case is shown for an example. Actual supported RPRE numbers will be found in EMRS standard.

Figure 2. Byte Lane READ Timing

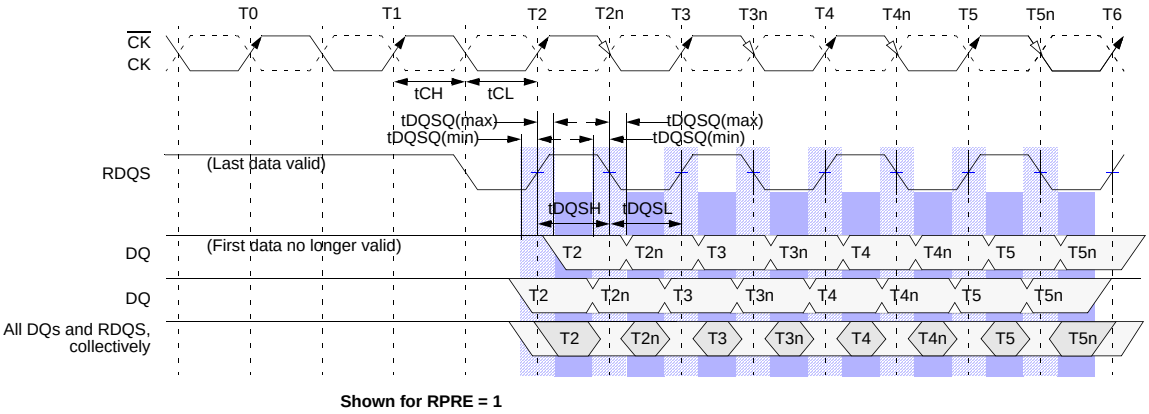
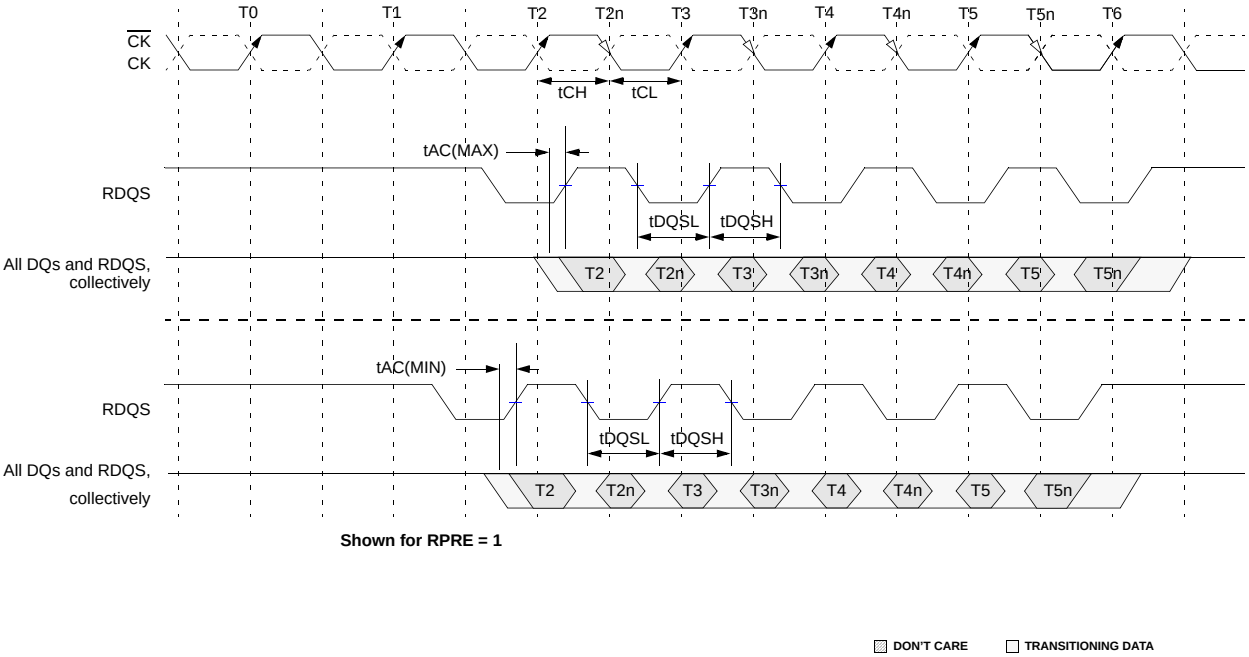
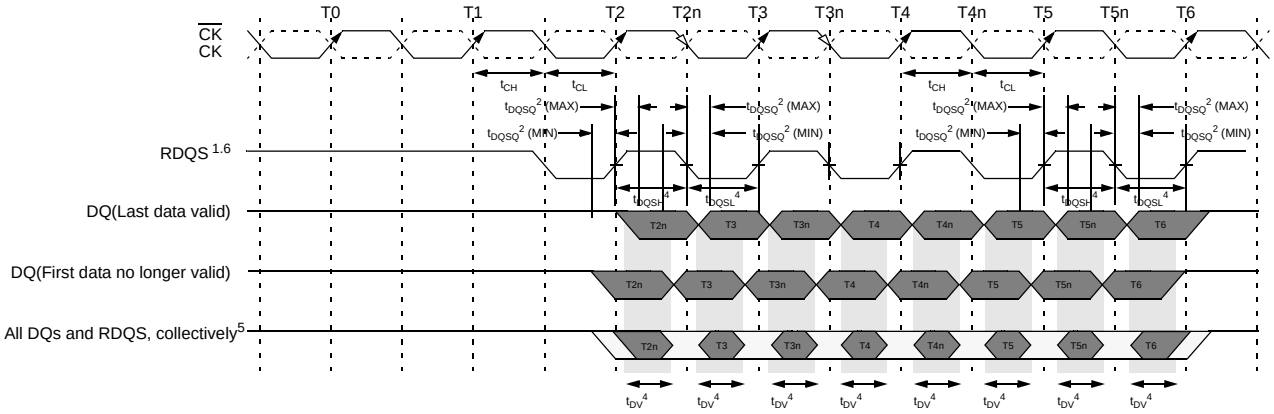


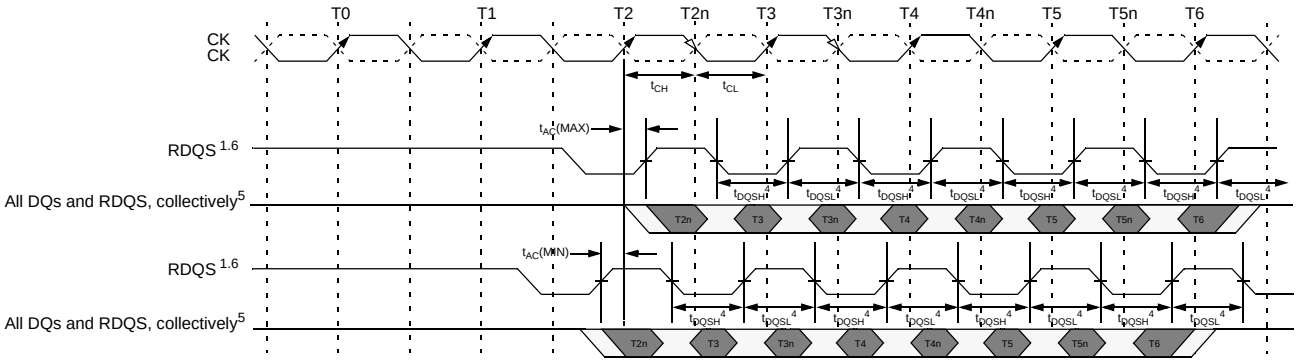
Figure 3. Byte Lane to CK/$\overline{CK}$



Data Output Timing (1) - t_{DQSQ}, t_{QH} and Data Valid Window

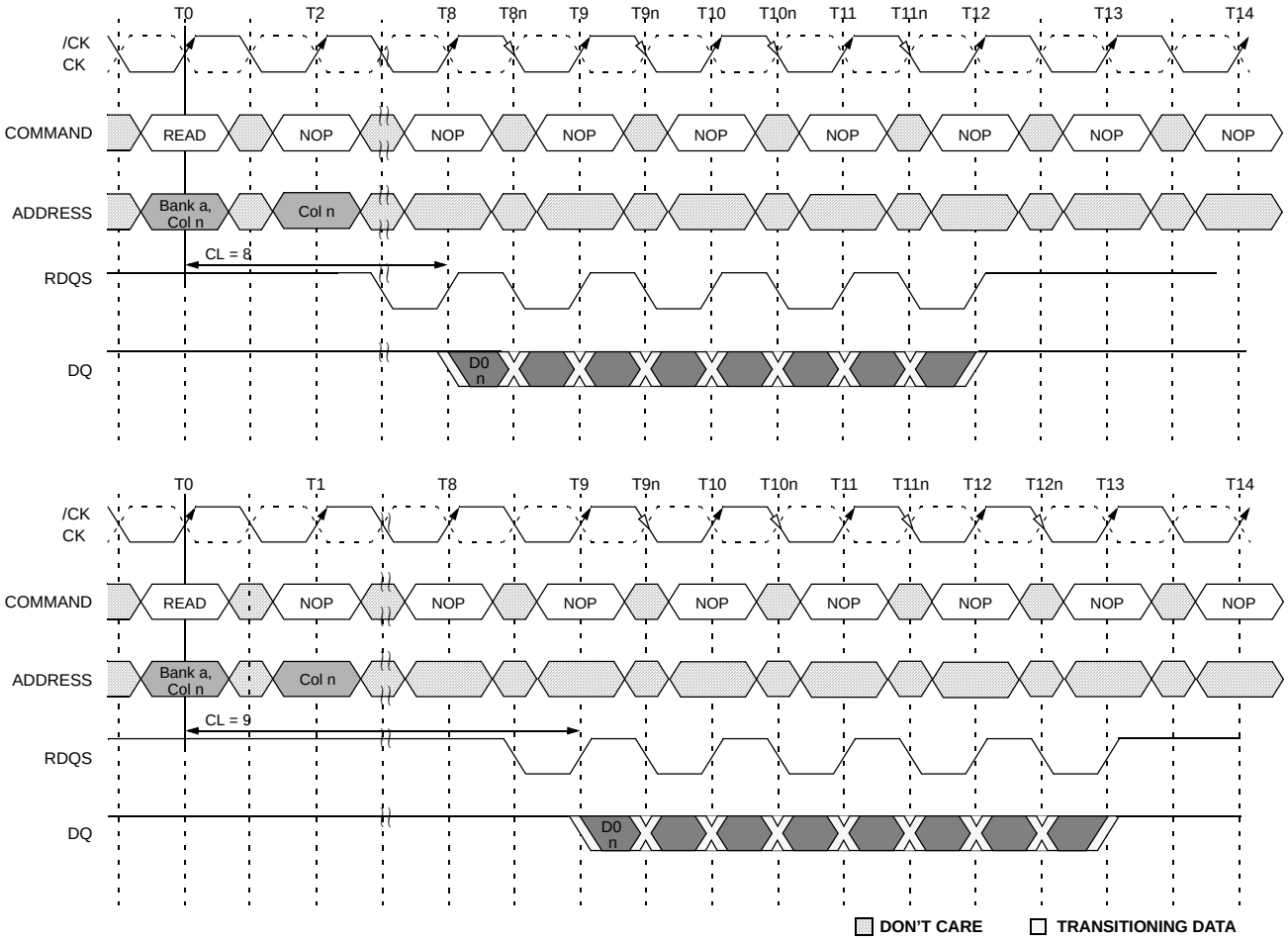


Data Output Timing (2) - t_{DQSQ}, t_{QH} and Data Valid Window



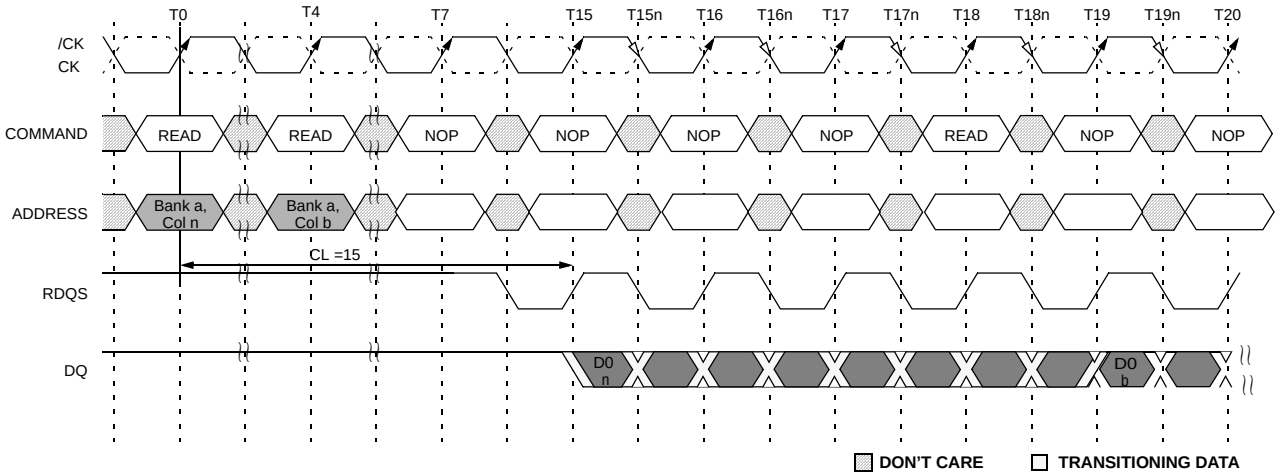
Note : 1. t_{DQSQ} represents the skew between the 8 DQ lines and the respective RDQS pin.
2. t_{DQSQ} is derived at each RDQS clock edge and is not cumulative over time and begins with first DQ transition and ends with the last valid transition of DQs.
3. t_{AC} is show in the nominal case
4. t_{DQHP} is the lesser of tDQSL or tDQSH strobe transition collectively when a bank is active.
5. The data valid window is derived for each RDQS transitions and is defined by t_{DV}.
6. There are 4 RDQS pins for this device with RDQS0 in relation to DQ0-DQ7, RDQS1 in relation DQ8-DQ15, RDQS2 in relation to DQ16-24 and RDQS3 in relation to DQ25-DQ31.
7. This diagram only represents one of the four byte lanes.
8. t_{AC} represents the relationship between DQ, RDQS to the crossing of CK and /CK.

READ Burst



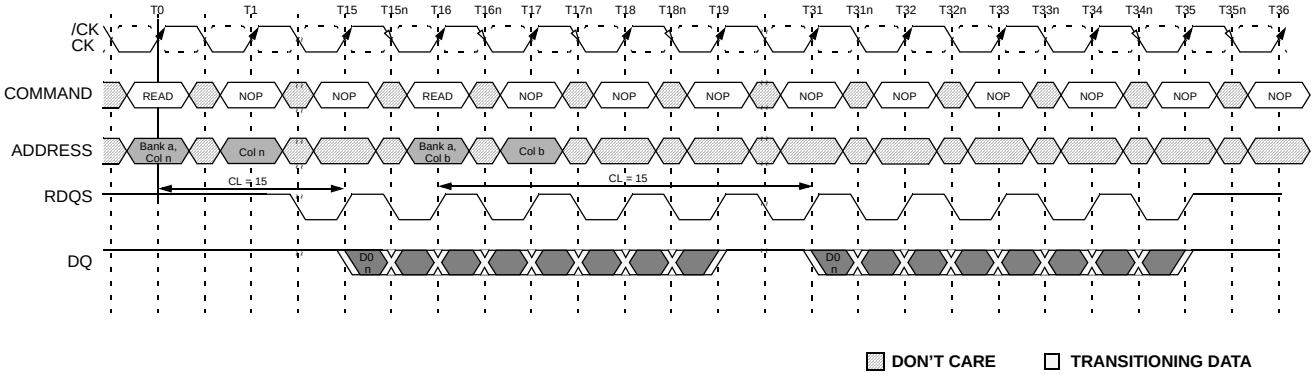
Note : 1. DO *n*=data-out from column *n*.
2. Burst length = 8
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Shown with nominal t_{AC} and t_{DQSQ}.
5. RDQS will start driving high 1/2 clock cycle prior to the first falling edge.

Consecutive READ Bursts



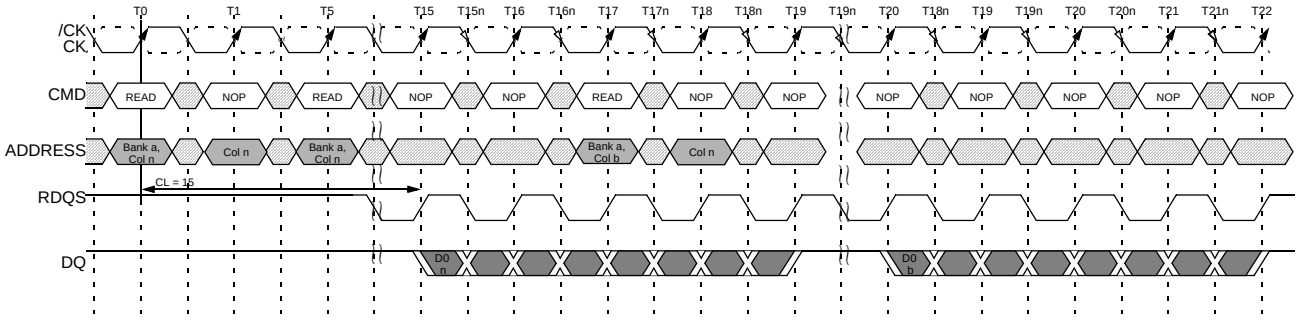
Note : 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 8
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Three subsequent elements of data-out appear in the programmed order following DQ *b*.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

Nonconsecutive READ Bursts



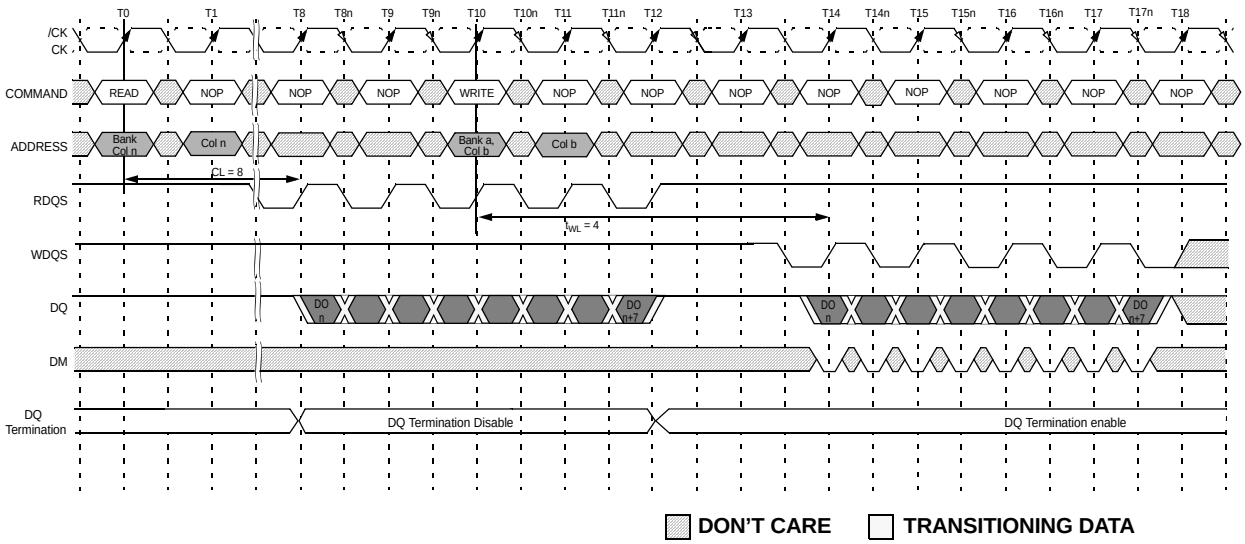
Note : 1. DO *n*=data-out from column *n*.
2. Burst length = 8
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Shown with nominal t_{AC} and t_{DQSQ}.
5. RDQS will start driving high 1/2 clock cycle prior to the first falling edge.

Random READ Accesses



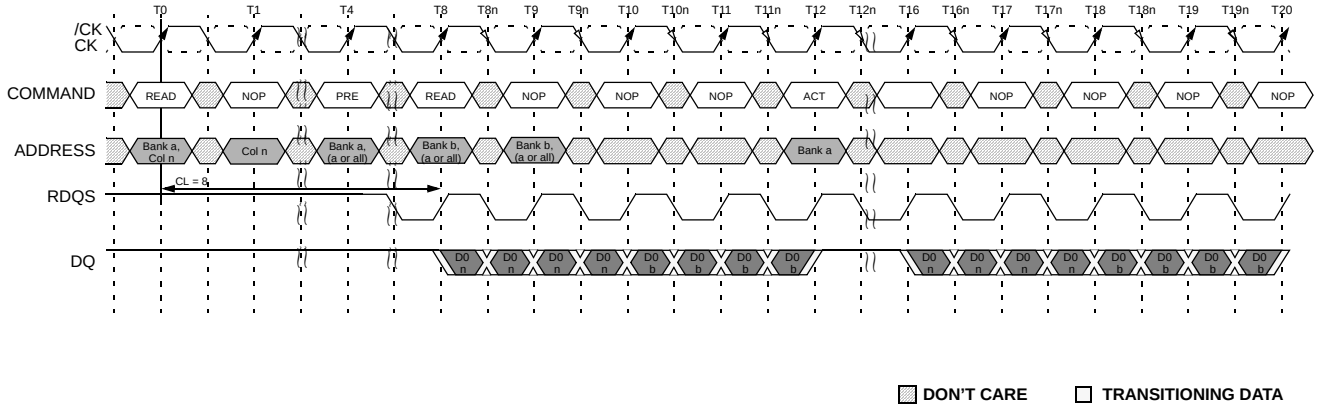
Note : 1. DO *n* (or *x* or *b* or *g*) = data-out from column *n* (or column *x* or column *x* or column *b* or column *g*).
2. Burst length = 8
3. *n*' or x or *b*' or *g*' indicates the next data-out following DO *n* or DO *x* or DO *b* OR DO *g*, respectively
4. READs are to an active row in any bank.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

READ to WRITE



Note : 1. DO *n* = data-out from column *n*.
2. DI *b* = data-in from column *b*.
3. Burst length = 8
4. One subsequent element of data-out appears in the programmed order following DO *n*.
5. Data-in elements are applied following DI *b* in the programmed order.
6. Shown with nominal t_{AC} and t_{DQSQ}.
7. t_{DQSS} in nominal case.
8. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.
9. The gap between data termination enable to the first data-in should be greater than 1tCK

READ to PRECHARGE



Note : 1. DO *n* (or *b*) = data-out from column *n* (or column *b*).
2. Burst length = 8
3. Three subsequent elements of data-out appear in the programmed order following DQ *n*.
4. Three subsequent elements of data-out appear in the programmed order following DQ *b*.
5. Shown with nominal t_{AC} and t_{DQSQ}.
6. Example applies when READ commands are issued to different devices or nonconsecutive READs.
7. RDQS will start driving high one half-clock cycle prior to the first falling edge of RDQS.

7.13.3 WRITEs

WRITE bursts are initiated with a WRITE command, as shown in Figure. The starting column and bank addresses are provided with the WRITE command, and auto precharge is either enabled or disabled for that access. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst. For the generic WRITE commands used in the following illustrations, auto precharge is disabled.

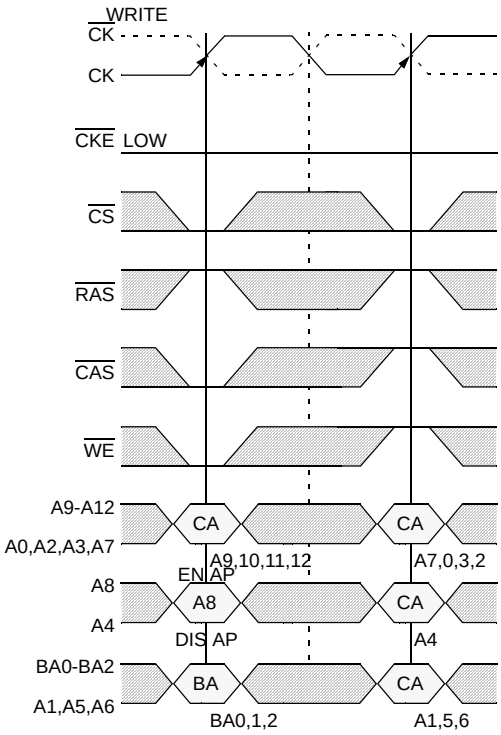
During WRITE bursts, the first valid data-in element will be registered in a rising edge of WDQS following the WRITE latency set in the mode register and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS edge a half cycle is needed and specified as the WRITE Preamble; the half cycle in WDQS following the last data-in element is known as the write postamble.

The time between the WRITE command and the first valid falling edge of WDQS (t_{DQSS}) is specified with a relative to the write latency. All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., $t_{DQSS(min)}$ and $t_{DQSS(max)}$) might not be intuitive, they have also been included. Write Burst figure shows the nominal case and the extremes of tDQSS for a burst of 4. Upon completion of a burst, assuming no other commands have been initiated, the DQs will remain High-Z and any additional input data will be ignored. Data for any WRITE burst may not be truncated with a subsequent WRITE command. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command after the burst has completed. The new WRITE command should be issued *x* cycles after the first WRITE command should be equals the number of desired nibbles (nibbles are required by 8n-prefetch architecture).

An example of nonconsecutive WRITEs is shown in Nonconsecutive WRITE to READ figure. Full-speed random write accesses within a page or pages can be performed as shown in Random WRITE cycles figure. Data for any WRITE burst may be followed by a subsequent READ command.

Data for any WRITE burst may be followed by a subsequent PRECHARGE command. To follow a WRITE the WRITE burst, t_{WR} should be met as shown in WRITE to PRECHARGE figure.

Data for any WRITE burst can not be truncated by a subsequent PRECHARGE command.



CA = Column Address
BA = Bank Address
EN AP = Enable Auto Precharge
DIS AP = Disable Auto Precharge

DON'T CARE

WRITE Command

GDDR4 SGRAM WRITE DATA TIMING

WRITE burst is initiated with a WRITE command.

The starting colume and bank addresses are provided at the WRITE command and the following clock cycle, and auto precharge is either enabled or disabled for that access with the A8 pin. If auto precharge is enabled, the row being accessed is precharged at the completion of the burst after tRAS min has been met.

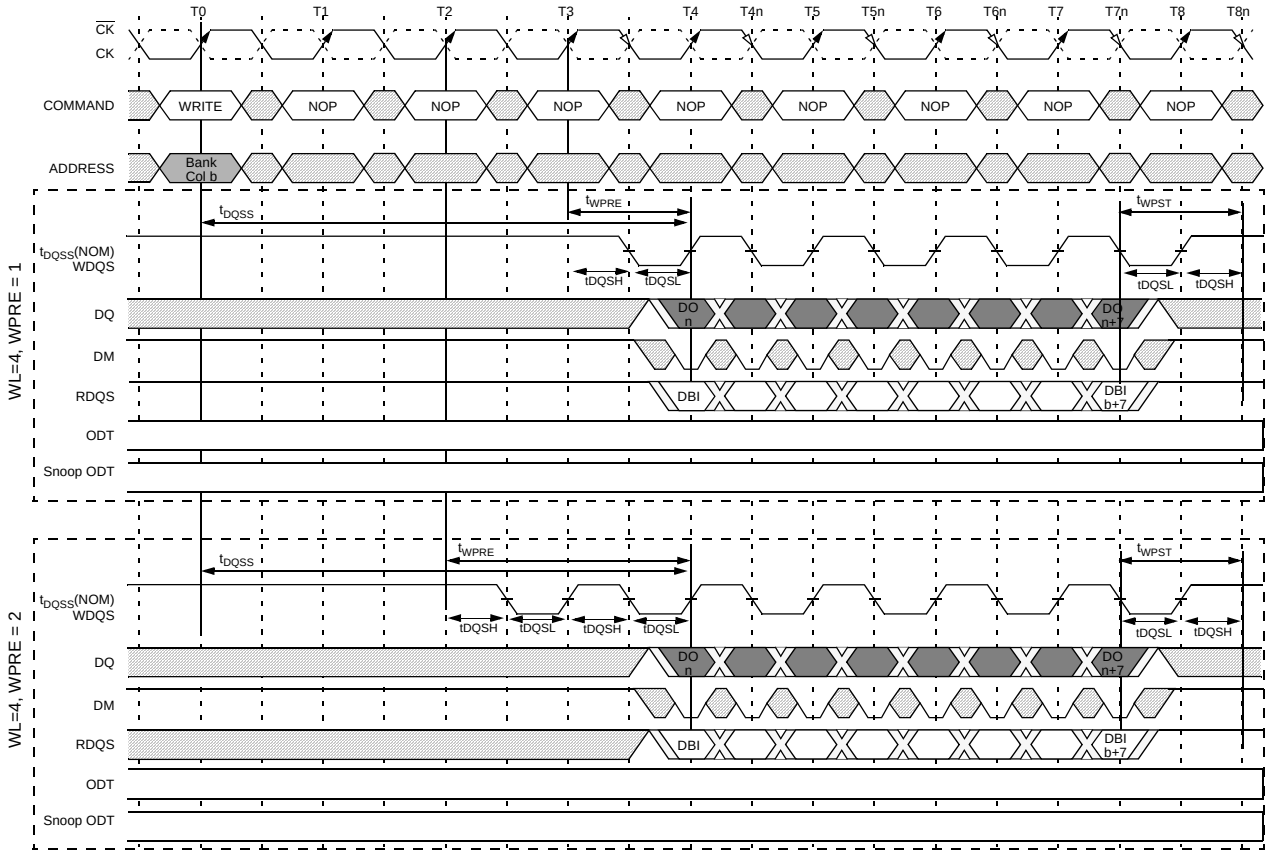
During WRITE bursts, the first valid data-out element will be registered on a rising of WDQS following the write latency plus the number preamble set in the mode (and extended mode) register and subsequent data elements will be registered on successive edges of WDQS. Prior to the first valid WDQS edge a cycle or cycles is/are needed and specified as the WRITE Preamble. The cycle on WDQS following the last data-in element is known as the write postamble and must be driven high by the controller it can not be left to float high using the on die termination.

The time between the WRITE command and the first valid edge of WDQS (tDQSS) is specified relative to the write latency and the number of write preamble (WL - 0.25CK and WL + 0.25CK), where WPRE is the number of write preamble set in the extended mode register. All of the WRITE diagrams show the nominal case, and where the two extreme cases (i.e., tDQSS[MIN] and tDQSS[MAX]) might not be intuitive, they have also been included. Upon completion of a burst, assuming no other commands have been initiated, the DQs wil remain High and any additional input data will be ignored.

Data for any WRITE burst may not be truncated with a subsequent WRITE command. The new WRITE command can be issued on any positive edge of clock following the previous WRITE command assuming the previous burst has completed. The new WRITE command should be issued at least 4 cycles after the first WRITE command. Data for any WRITE burst cannot be truncated by a subsequent PRECHARGE command. After the PRECHARGE command, a subsequent command to the same bank cannot be issued until tRP is met.

The data inversion flag receives the RDQS signal to identify whether to store the true or inverted data. If RDQS is HIGH, the data will be stored after inversion inside the DRAM and not inverted when it recognizes RDQS is LOW. WRITE Data Inversion can be programmed as a Disable(E9=0) or Enable(E9=1) in the extended mode register 1.

Figure 1. WRITE Command



DON'T CARE TRANSITIONING DATA

Note : WPRE = 2 case is shown for an example. Actual supported WPRE numbers will be found in EMRS standard.

Figure 2. WRITE Capture

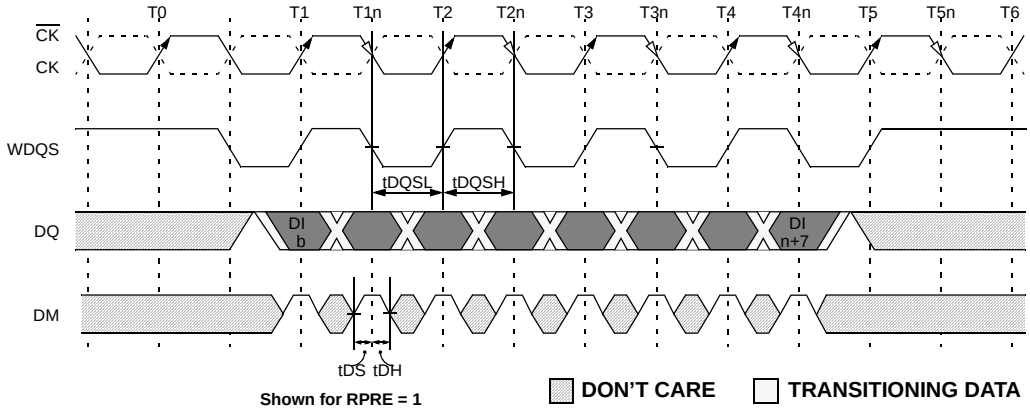
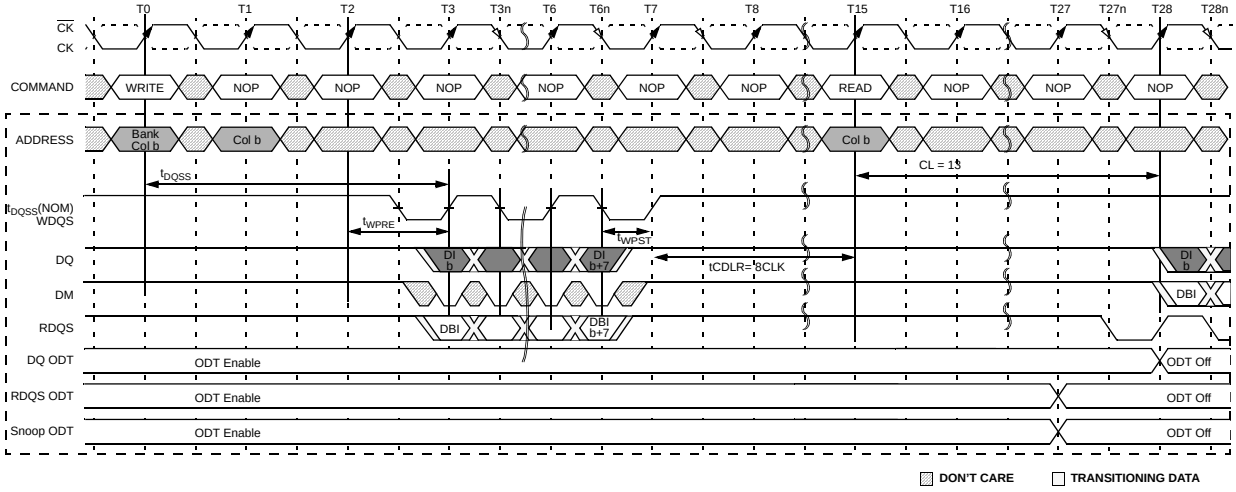
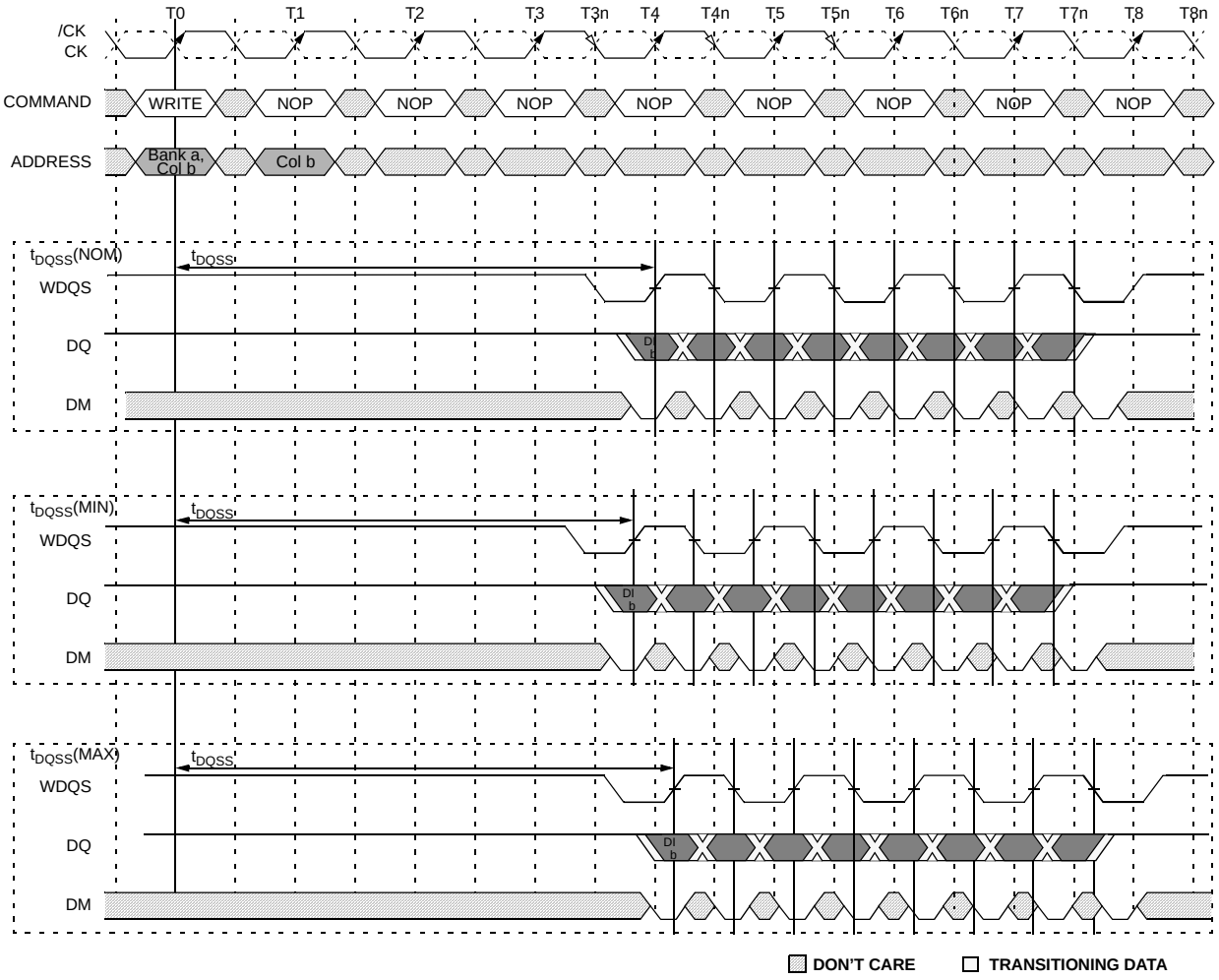


Figure 3. WRITE to READ



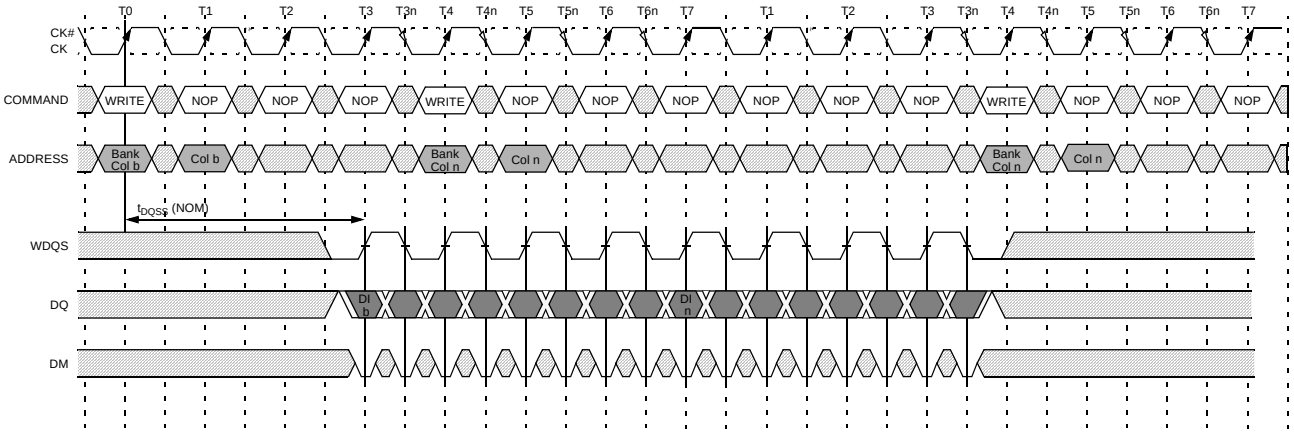
NOTE : 1. DI *b* = data-in for column *b*.
2. Seven subsequent elements of data-in are applied in the specified order following DI *b*.
3. A burst of 8 is shown.
4. t_{WTR} is referenced from the first positive CK edge after the last written data.
5. The READ and WRITE commands are to the same device. However, the READ and WRITE commands may be to different devices, in which case t_{WTR} is not required and the READ command could be applied earlier.
6. A8 is LOW with the WRITE command (auto precharge is disabled).
7. WRITE latency is set to 3.
8. The 8n prefetch architecture requires a 8-clock last data in to read data turnaround time (t_{CDLR}).

WRITE Burst



Note : 1. DI b = data-in for column b.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. A burst of 8 is shown.
4. A8 is LOW with the WRITE command (auto precharge is disabled).
5. Write latency is set to 4

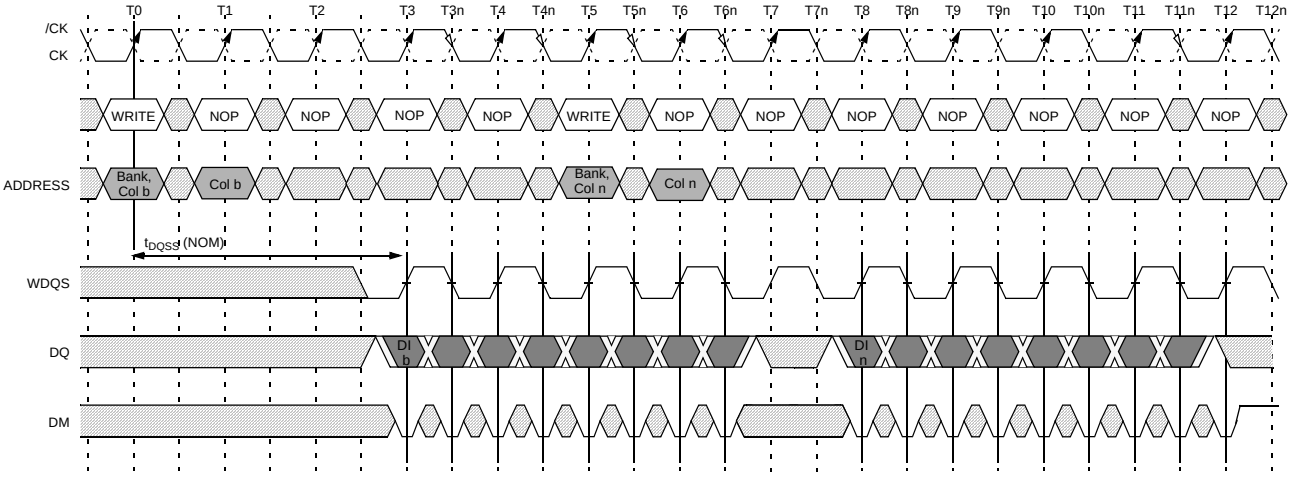
Consecutive WRITE to WRITE



DON'T CARE TRANSITIONING DATA

Note : 1. DI *b*, etc. = data-in for column *b*, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI *b*.
3. Three subsequent elements of data-in are applied in the programmed order following DI *n*.
4. Burst of 8 is shown.
5. Each WRITE command may be to any bank of the same device.
6. Write latency is set to 3

Nonconsecutive WRITE to WRITE

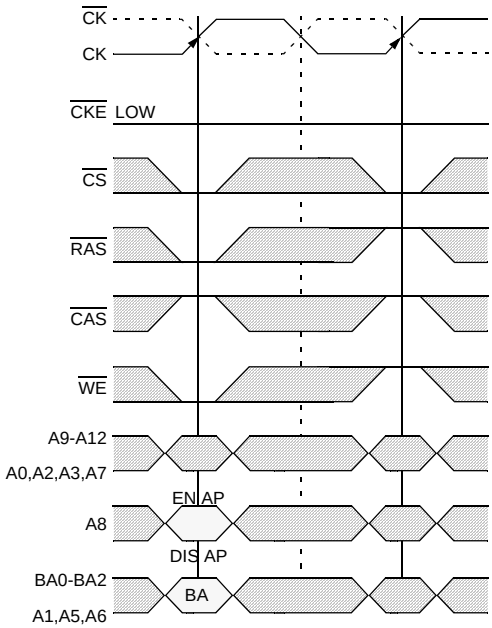


DON'T CARE TRANSITIONING DATA

Note : 1. DI b, etc. = data-in for column b, etc.
2. Three subsequent elements of data-in are applied in the programmed order following DI b.
3. Three subsequent elements of data-in are applied in the programmed order following DI n.
4. burst of 8 is shown.
5. Each WRITE command may be to any bank.
6. Write latency is set to 3

7.13.4 Precharge

The PRECHARGE command is used to deactivate the open row in a particular bank or the open row in all banks. The bank(s) will be available for a subsequent row access some specified time (t_{RP}) after the PRECHARGE command is issued. Input A8 determines whether one or all banks are to be precharged, and in the case where only one bank is to be precharged, inputs BA0, BA1 and BA2 select the bank. When all banks are to be precharged, inputs BA0, BA1, BA2 are treated as "Don't Care." Once a bank has been precharged, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to the bank.



BA = Bank Address (if A8 is LOW ; otherwise 'Don't Care')

DON'T CARE

BA=Bank Address
(if A8 is LOW; otherwise "Don't Care")

PRECHARGE Command

7.13.5 Power-down (CKE not Active)

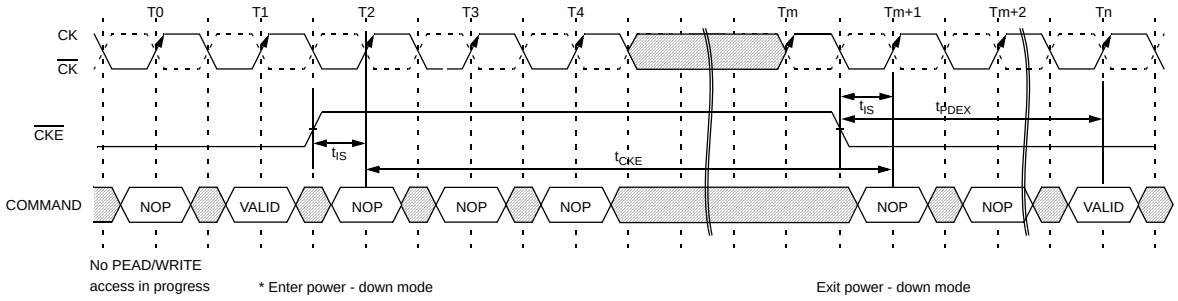
Unlike SDR SGRAMs,GDDR4(x32) SGRAM requires $\overline{CKE}$ to be active at all times an access is in progress; from the issuing of a READ or WRITE command until completion of the burst. For READs, a burst completion is defined when the Read Postamble is satisfied; For WRITEs, a burst completion is defined BL/2 cycles after the Write Postamble is satisfied.

Power-down is entered when $\overline{CKE}$ is registered High. If power-down occurs when there is a row active in any bank, this mode is referred to as active power-down. Entering power-down deactivates the input and output buffers, excluding CK,/CK and $\overline{CKE}$. For maximum power savings, the user has the option of disabling the DLL prior to entering power-down. However, power-down duration is limited by the refresh requirements of the device, so in most applications,the self-refresh mode is preferred over the DLL-disabled power-down mode.

When in power-down, $\overline{CKE}$ High and a stable clock signal must be maintained at the inputs of the GDDR4 SGRAM, while all other input signals are "Don't Care" except data terminator disable command.

The power-down state is synchronously exited when $\overline{CKE}$ is registered LOW (in conjunction with a NOP or DESELECT command). A valid executable command may be applied tPDEX later.

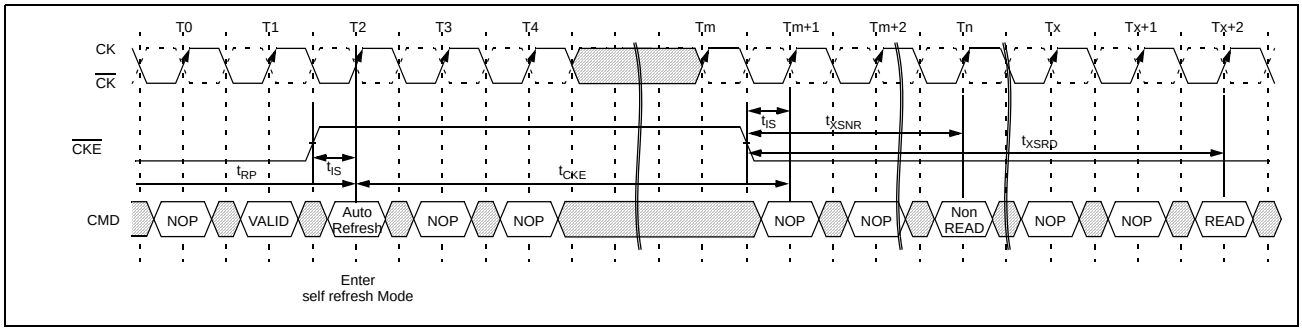
Power-Down



* Once the device enters the power down mode, it should be in NOP state more than 10ns.

7.13.6 Self Refresh

A self refresh command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ held low with $\overline{WE}$ and $\overline{CKE}$ high at the rising edge of the clock(CK). Once the self refresh command is initiated, $\overline{CKE}$ must be held High to keep the device in self refresh mode. During the self refresh operation, all inputs except $\overline{CKE}$ are ignored. The clock is internally disabled during self refresh operation to reduce power consumption. The self refresh is exited by supplying stable clock input before returning $\overline{CKE}$ Low, asserting deselect or NOP command and then asserting $\overline{CKE}$ Low for longer than tXSR for locking of DLL.



7.14 GDDR4 Read and Write DBI

The GDDR4 Data Bus Inversion (DBI) logic reduces the AC power (DBIac)as shown in the flow chart in figure 3 for reads.
The mapping of the DBI fiag for reads and writes are as follows:

TABLE 1. DBI Flag mapping for Reads

Data	DBI Flag
DQ[7:0]	DM[0]
DQ[15:8]	DM[1]
DQ[23:16]	DM[2]
DQ[31:24]	DM[3]

TABLE 2. DBI Flag mapping for Writes

Data	DBI Flag
DQ[7:0]	RDQS[0]
DQ[15:8]	RDQS[1]
DQ[23:16]	RDQS[2]
DQ[31:24]	RDQS[3]

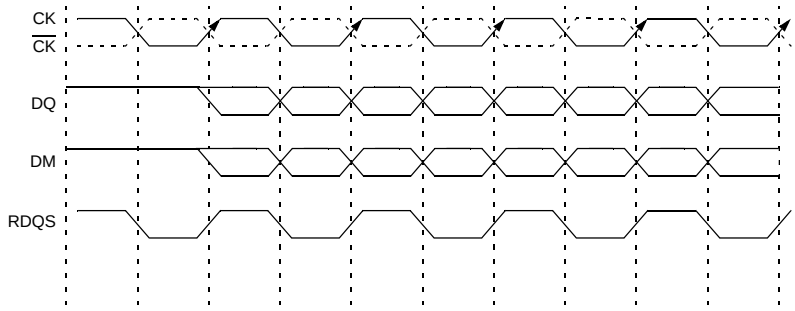
Note : When the DBI Flag equals 1 the Data is inverted

The timing diagram in figure 3 shows the read timing of the DM and the read Data DQ. The timing diagram in figure 4 shows the write timing of the RDQ and the write data DQ.

GDDR4 DBI logic reduces the DC power (DBIdc) as shown in the flow chart in figure 1 for Reads.

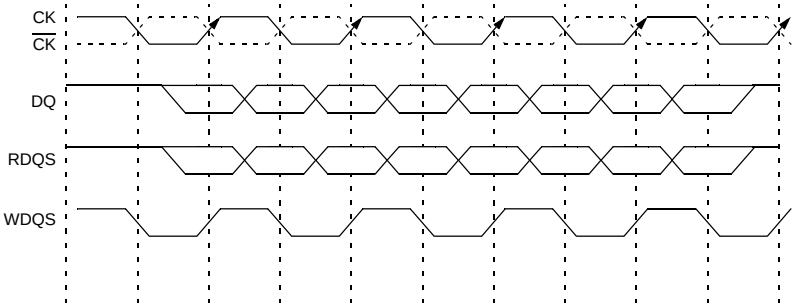
DBI Read Timing

The timing diagram shows the read timing of the DM and the read Data DQ.



DBI Write Timing

The timing diagram shows the write timing of the RDQ and the write data DQ.



Note 1 : For more detailed Read and Write timing diagrams please refer to the Read and Write descriptions in the specification.

Figure 1
Flow Chart Read DBIdc

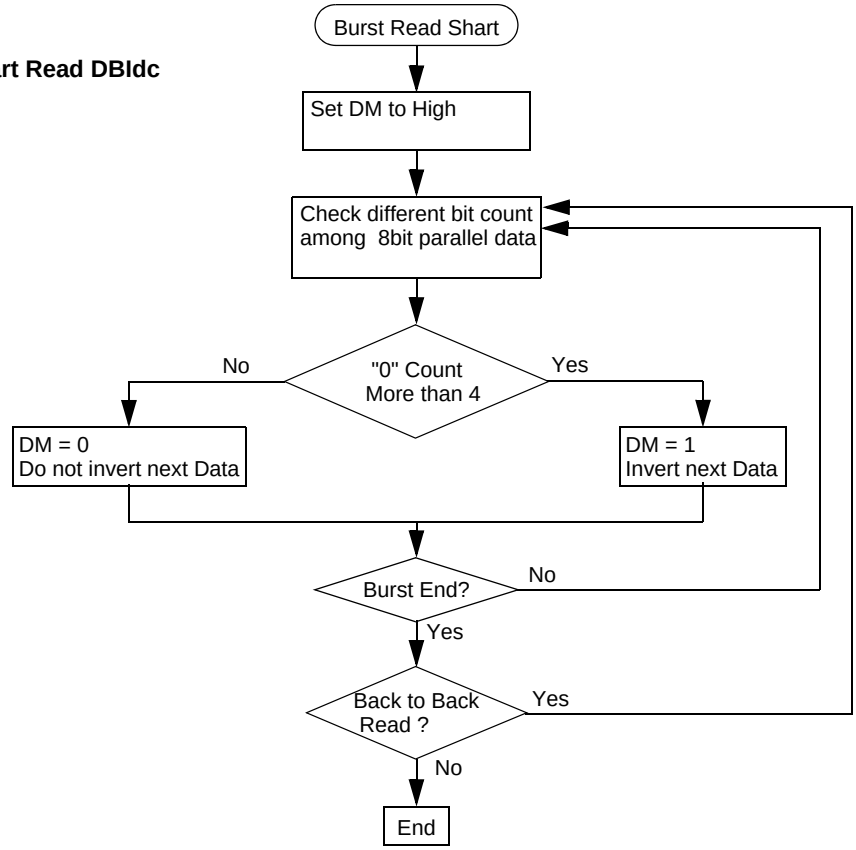


Figure 2

Flow Chart Write DBIdc

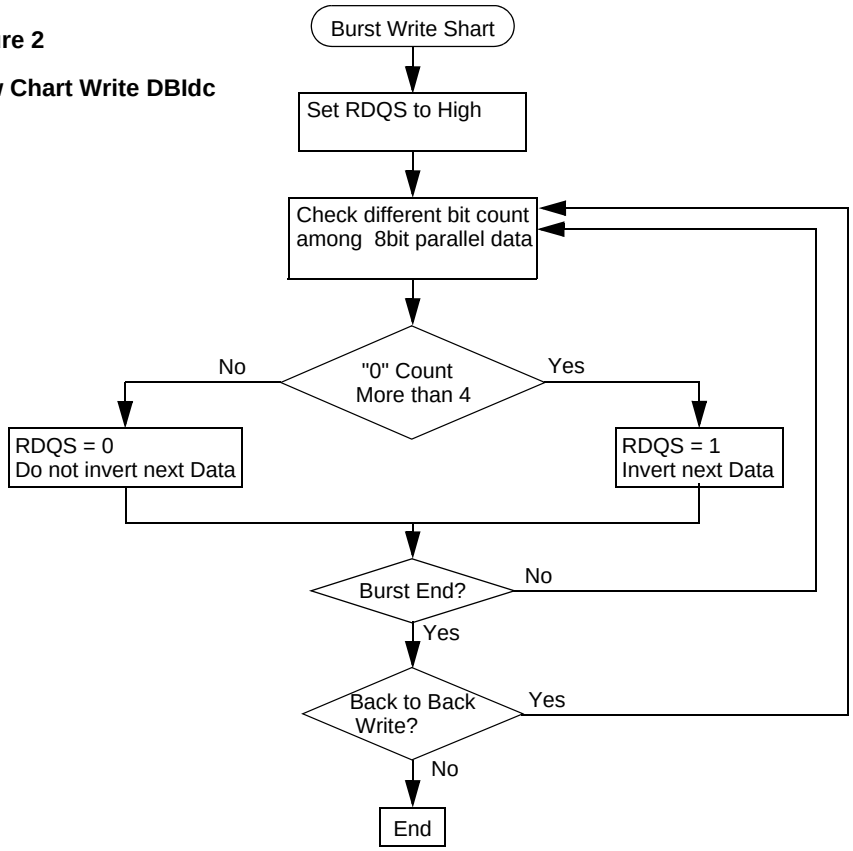


Figure 3
Flow Chart Read DBIac

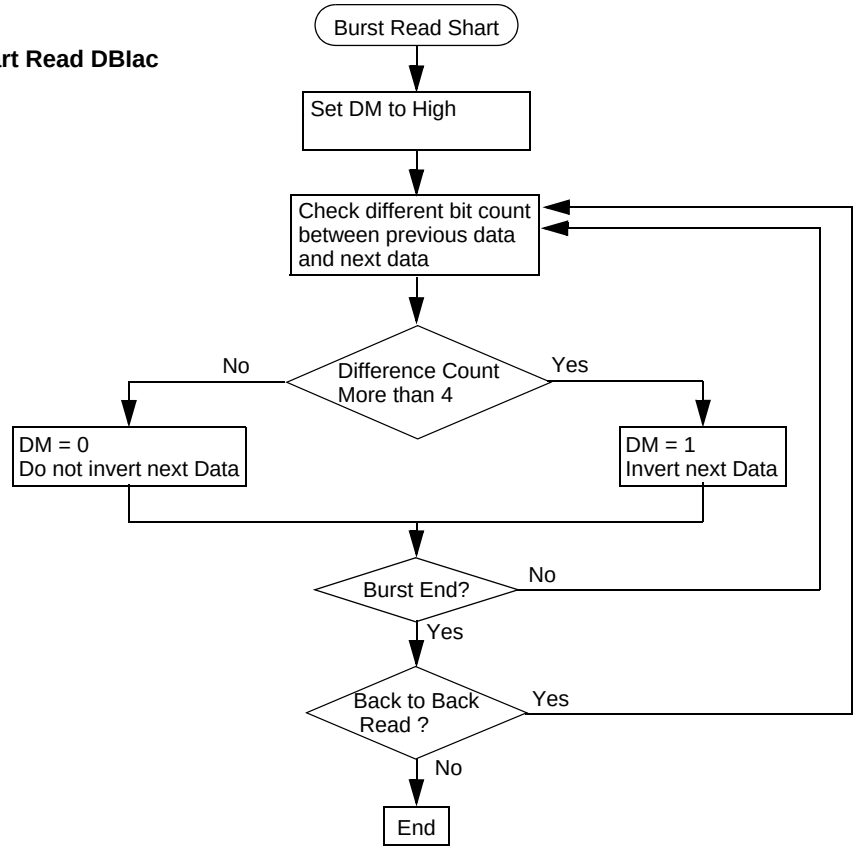
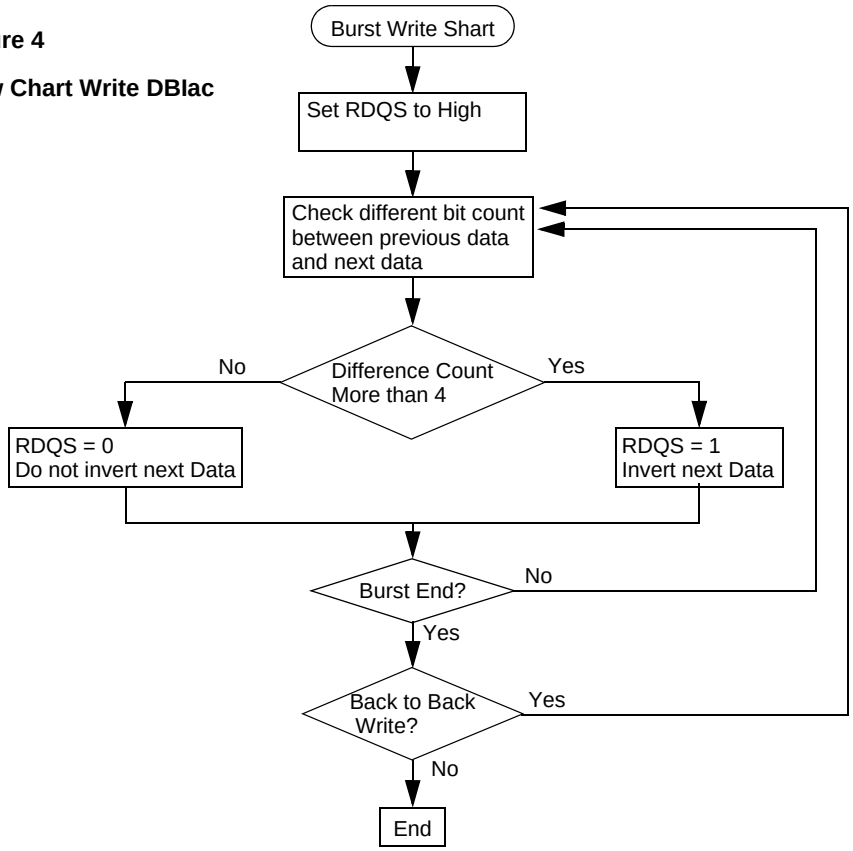


Figure 4

Flow Chart Write DBIac



7.15 GDDR4 SGRAM Data Training

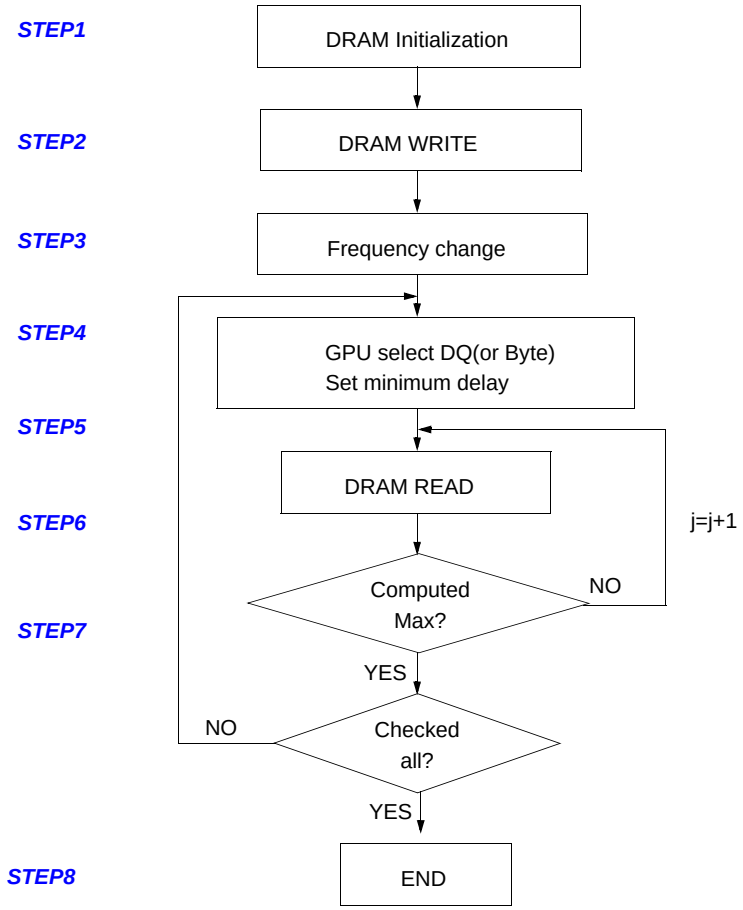
GDDR4 SGRAM can use normal DRAM write and read operation for data training. Before starting data training, the DRAM must be powered up and initialized in a predefined manner to prevent undefined operations. Then start read data training by going through step 1~ step 8 sequentially. After the read data training, the write data training can be started or vice versa. The preferred manner is read data training first and then write data training.

GDDR4 Read Data Training Sequence

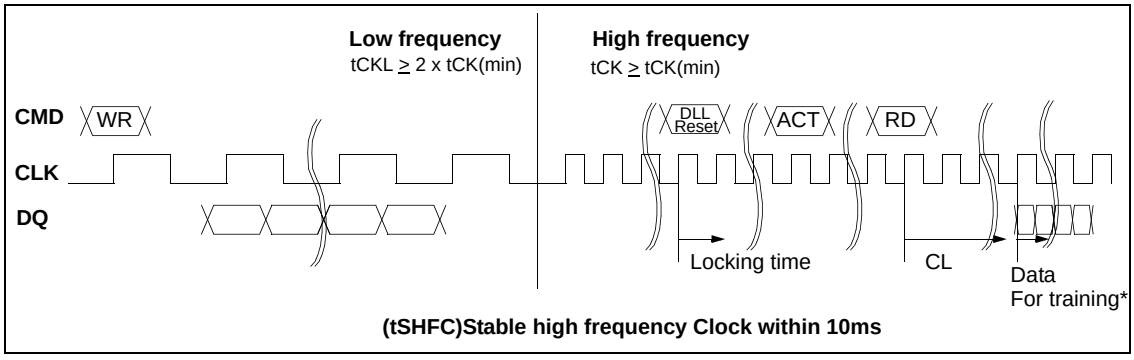
Step:

1. DRAM initialization should be done properly first and provide low clock frequency.
2. Issue DRAM write command to load data pattern at tCKL(clock frequency low) which defined more than 2 times of tCK(min). GPU can define the data pattern for the training. During the DRAM write, Refresh command can be used if required.
3. After completing DRAM write at tCKL, then change the clock frequency to target high frequency for the DRAM read within 10ms to prevent DRAM data loss just in case there is no refresh command. DLL reset is required after changing the frequency.
4. The controller needs to select a DQ(or Byte) to be trained and set a minimum delay
5. Issue normal DRAM read command. During normal DRAM read operation, Refresh command can be issued if required.
6. After the read command issued, if the step is not Max. then go to step5. Repeat Step5 to step6 until scan all the delay steps.
7. If all DQs(or Byte) are not checked, then go to step4. Repeat step4 ~step7 until scan all the delay steps.
8. If all completed, then END of DRAM READ data training

Read Data Training Flow Chart



Read Data Training Timing Diagram



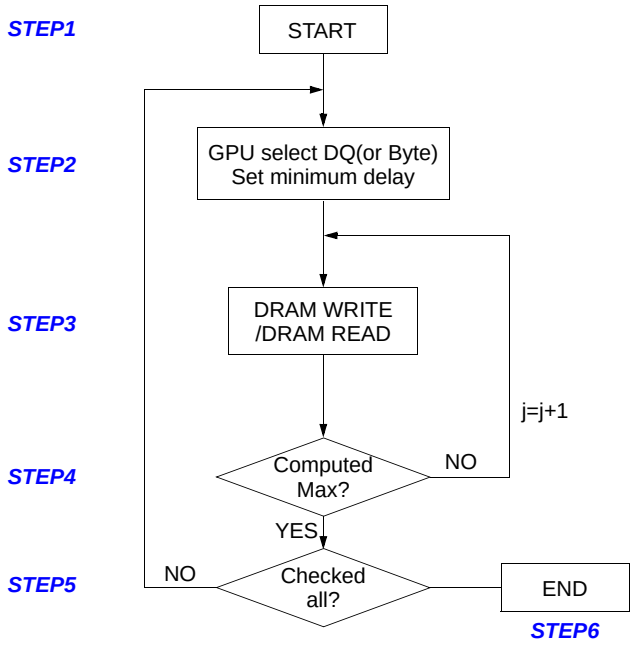
GDDR4 Write Data Training Sequence

Write data training procedure is almost same as read data training's, however it doesn't require DRAM frequency change what required to be done in read data training. To make sure the safe DRAM write, the low clock frequency need to be supplied for the DRAM write operation during the DRAM read data training while DRAM write data training case doesn't require such kind of frequency change because read data all trained already.

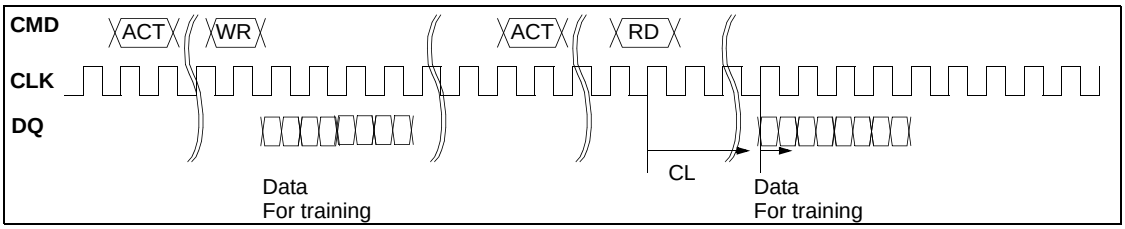
Step :

1. The controller needs to select a DQ(or Byte) to be trained, and then set minimum delay
2. Issue normal DRAM WRITE command and then READ the data for the validation. During the DRAM write and read operations, Refresh command can be issued if required.
3. Increase a delay step. If the step is not Max. then go to step1. Repeat step 3~4 until scan all the delay steps.
4. If all DQ(or Byte) is not checked, go to step2. Repeat step 2~5 until scan all DQs(or bytes)
5. END of DRAM WRITE data training

Write Data Training Flow chart



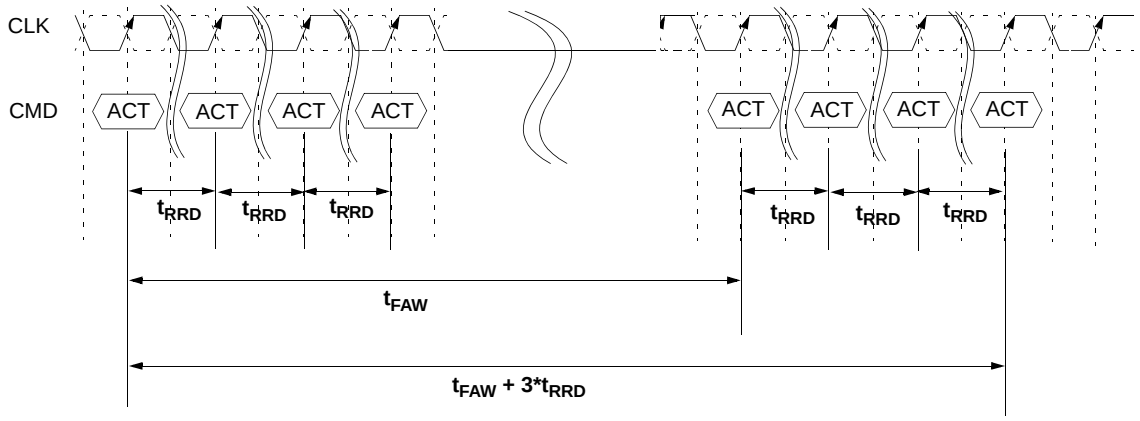
DRAM Write Data Training Timing Diagram



7.16 GDDR4 tFAW Definition

For 8 bank GDDR4 devices, there is a need to limit the number of activates in a rolling window to ensure that the instanteous current supplying capability of the devices is not exceeded.

8 bank device Sequential Bank Activation Restriction : No more than 4 banks may be activated in a rolling tFAW window. Converting to clocks is done by dividing tFAW(ns) by tCK(ns) and rounding up to next integer value. As an example of the rolling window, if (tFAW/tCK) rounds up to 10 clocks, and an activate command is issued in clock N, no more than three further activate commands may be issued in clocks N+1 through N+9.



8.0 TRUTH TABLE

TRUTH TABLE - Clock Enable ($\overline{CKE}$)

$\overline{CKE}$n-1	$\overline{CKE}$n	CURRENT STATE	COMMANDn	ACTIONn	Note
H	H	Power-Down	X	Maintain Power-Down	
		Self Refresh	X	Maintain Self Refresh	
H	L	Power-Down	DESELECT or NOP	Exit Power-Down	
		Self Refresh	DESELECT or NOP	Exit Self Refresh	5
L	H	All Banks Idle	DESELECT or NOP	Precharge Power-Down Entry	
		Bank(s) Active	DESELECT or NOP	Active Power-Down Entry	
		All Banks Idle	AUTO REFRESH	Self Refresh Entry	

Note :

1. $\overline{CKE}$n is the logic state of $\overline{CKE}$ at clock edge *n*; $\overline{CKE}$n-1was the state of $\overline{CKE}$ at the previous clock edge.
2. Current state is the state of the GDDR4(x32) immediately prior to clock edge *n*.
3. COMMANDn is the command registered at clock edge *n*, and ACTION*n* is a result of COMMAND*n*
4. All state and sequence not shown are illegal or reserved.
5. DESELECT or NOP commands should be issued on any clock edges occurring during the t_{XSA} period.

TRUTH TABLE - CURRENT STATE BANK *n* - COMMAND TO BANK *n*

CURRENT STATE	/CS	/RAS	/CAS	/WE	COMMAND/ ACTION	Note
Any	H	X	X	X	DESELECT (NOP/ continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	X	H	L	H	DATA TERMINATOR DISABLE	
Idle	L	L	H	H	ACTIVE (Select and activate row)	
	L	L	L	H	AUTO REFRESH	7
Row Active	L	L	L	L	LOAD MODE REGISTER	7
	L	H	L	H	READ (Select column and start READ burst)	10
	L	H	L	L	WRITE (Select Column and start WRITE burst)	10
	L	L	H	L	PRECHARGE (Deactivate row in bank or banks)	8
Read (Auto-Precharge Disable)	L	H	L	H	READ (Select column and start new READ burst)	10
	L	H	L	L	WRITE (Select column and start WRITE burst)	10, 12
	L	L	H	L	PRECHARGE (Only after the READ burst is complete)	8
Write (Auto-Precharge Disabled)	L	H	L	H	READ (Select column and start READ burst)	10, 11
	L	H	L	L	WRITE (Select column and start new WRITE burst)	10
	L	L	H	L	PRECHARGE (Only after the WRITE burst is complete)	8, 11

Note :

1. This table applies when $\overline{CKE}$n-1 was LOW and $\overline{CKE}$n is LOW (see CKE Truth Table) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table is bank-specific, except where noted (i.e., the current state is for a specific bank and the commands shown are those allowed to be issued to that bank when in that state). Exceptions are covered in the notes below.
3. Current state definitions :

Idle : The bank has been precharged, and t_{RP} has been met.
Row Active : A row in the bank has been activated, and t_{RCD} has been met.
No data bursts/accesses and no register accesses are in progress.
Read : A READ burst has been initiated, with auto precharge disabled.
Write : A WRITE burst has been initiated, with auto precharge disabled.

4. The following states must not be interrupted by a command issued to the same bank. COMMAND INHIBIT or NOP commands, or allowable commands to the other bank should be issued on any clock edge occurring during these states. Allowable commands to the other bank are determined by its current state and truth table- current state bank *n* - command to bank *n*. and according to truth table - current state bank *n* -command to bank *m.*

Precharging : Starts with registration of a PRECHARGE command and ends when t_{RP} is met. Once t_{RP} is met, the bank will be in the idle state.

Row Activating : Starts with registration of an ACTIVE command and ends when t_{RCD} is met. Once t_{RCD} is met, the bank will be in the :row active" state.

Read w/ Auto-Precharge Enabled : Starts with registration of an READ command with auto precharge enabled and ends when tRP has been met. Once t_{RP} is met, the bank will be in the idle state.

Write w/ Auto-Precharge Enabled : Starts with registration of a WRITE command with auto precharge enabled and ends when t_{RP} has been met. Once t_{RP} is met, the bank will be in the idle state.

5. The following states must not be interrupted by any executable command ; COMMAND INHIBIT or NOP commands must be applied on each positive clock edge during these states.

Refreshing : Starts with registration of an AUTO REFRESH command and ends when t_{RC} is met. Once t_{RC} is met, the GDDR4(x32) will be in the all banks idle state.

Accessing Mode Register : Starts with registration of a LOAD MODE REGISTER command and ends when t_{MRD} has been met. Once t_{MRD} is met, the GDDR4(x32) SGRAM will be in the all banks idle state.

Precharge All : Starts with registration of a PRECHARGE ALL command and ends when t_{RP} is met. Once t_{RP} is met, all banks will be in the idle state.

READ or WRITE : Starts with registration of the ACTIVE command and ends the last valid data nibble.

6. All states and sequences not shown are illegal or reserved.
7. Not bank-specific; requires that all banks are idle, and bursts are not in progress.
8. May or may not be bank-specific ; If multiple banks are to be precharged, each must be in a valid state for precharging.
9. Left blank
10. READs or WRITEs listed in the Command/Action column include READs or WRITaEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
11. Requires appropriate DM masking.
12. A WRITE command may be applied after the completion of the READ burst.

TRUTH TABLE - CURRENT STATE BANK n - COMMAND TO BANK m

CURRENT STATE	/CS	/RAS	/CAS	/WE	COMMAND/ ACTION	NOTE
Any	H	X	X	X	DESELECT (NOP/ continue previous operation)	
	L	H	H	H	NO OPERATION (NOP/continue previous operation)	
	X	H	L	H	DATA TERMINATOR DISABLE	
Idle	X	X	X	X	Any Command Otherwise Allowed to Bank m	
Row Activating, Active, or Prechrging	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	6
	L	H	L	L	WRITE (Select Column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (Auto-Precharge Disable)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	6
	L	H	L	L	WRITE (Select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (Auto-Precharge Disabled)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	6, 7
	L	H	L	L	WRITE (Select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	
Read (With Auto-Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start new READ burst)	6
	L	H	L	L	WRITE (Select column and start WRITE burst)	6
	L	L	H	L	PRECHARGE	
Write (With Auto-Precharge)	L	L	H	H	ACTIVE (Select and activate row)	
	L	H	L	H	READ (Select column and start READ burst)	6
	L	H	L	L	WRITE (Select column and start new WRITE burst)	6
	L	L	H	L	PRECHARGE	

Note :
1. This table applies when $\overline{CKE}$*n-1* was LOW and $\overline{CKE}$*n* is LOW (see TRUTH TABLE- $\overline{CKE}$) and after t_{XSNR} has been met (if the previous state was self refresh).
2. This table describes alternate bank operation, except where noted (i.e., the current state is for bank *n* and the commands shown are those allowed to be issued to bank *m*, assuming that bank m is in such a state that the given command is allowable). Exceptions are covered in the notes below.

3. Current state definitions :

Idle : The bank has been precharged, and t_{RP} has been met.

Row Active : A row in the bank has been activated, and t_{RCD} has been met. No data bursts/accesses and no register accesses are in progress.

Read : A READ burst has been initiated, with auto precharge disabled.

Write : A WRITE burst has been initiated, with auto precharge disabled.

Read w/ Auto-Precharge Enabled : See following text

Write w/ Auto-Precharge Enabled : See following text

3a. The read with auto precharge enabled or write with auto precharge enabled states can each be broken into two parts : the access period and the precharge period. For read with auto precharge, the precharge period is defined as if the same burst was executed with auto precharge disabled and then followed with the earliest possible PRE-CHARGE command that still accesses all of the data in the burst. For write with auto precharge, the precharge period begins when tWR ends, with tWR command and ends where the precharge period (or t_{RP}) begins. During the precharge period of the read with auto precharge enabled or write with auto precharge enabled states, ACTIVE, PRECHARGE, READ and WRITE commands to the other bank may be applied. In either case, all other related Limitations apply (e.g., contention between read data write data must be avoided).

3b. The minimum delay from a READ or WRITE command with auto precharge enabled, to a command to a different bank is summarized below.

From Command	To Command	Minimum delay (with concurrent auto precharge)
WRITE w/AP	READ or READ w/AP	[WL + (BL/2)]* tCK + tCDLR
	WRITE or WRITE w/AP	(BL/2) * tCK
	PRECHARGE	1 tCK
	ACTIVE	1 tCK
READ w/AP	READ or READ w/AP	(BL/2) * tCK
	WRITE or WRITE w/AP	[CL + (BL/2) + 2 - WL] * tCK
	PRECHARGE	1 tCK
	ACTIVE	1 tCK

4. AUTO REFRESH and LOAD MODE REGISTER commands may only be issued when all banks are idle.
5. All states and sequences not shown are illegal or reserved.
6. READs or WRITEs listed in the Command/Action column include READs or WRITEs with auto precharge enabled and READs or WRITEs with auto precharge disabled.
7. Requires appropriate DM masking.

9.0 AC & DC OPERATING CONDITIONS

9.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ V_{DDQ} + 0.5V	V
Voltage on VDD supply relative to Vss	V_{DD}	-0.5 ~ 2.5	V
Voltage on VDDQ supply relative to Vss	V_{DDQ}	-0.5 ~ 2.5	V
MAX Junction Temperature	TJ	+125	°C
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	4	W
Short Circuit Output Current	IOS	50	mA

Note : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure periods may affect reliability.

9.2 POWER & DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to 0°C ≤ Tc ≤ 85°C ; V_{DD}=1.8V ± 0.09V, V_{DDQ}=1.8V ± 0.09V)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	VDD	1.71	1.8	1.89	V	1
Output Supply voltage	VDDQ	1.71	1.8	1.89	V	1
Reference voltage	VREF	0.69*VDDQ	-	0.71*VDDQ	V	3
DC Input logic high voltage	VIH (DC)	VREF+0.15	-	-	V	4
DC Input logic low voltage	VIL (DC)	-	-	VREF-0.15	V	4
Output logic low voltage	VOL(DC)	-	-	0.76	V	
AC Input logic high voltage	VIH(AC)	VREF+0.25	-	-	V	4,5,6
AC Input logic low voltage	VIL(AC)	-	-	VREF-0.25	V	4,5,6
Input leakage current Any input 0V-<VIN -< VDDQ (All other pins not under test = 0V)	II	-5	-	5	uA	
Output leakage current (DQs are disabled ; 0V-<VOUT -< VDDQ)	IIOZ	-5	-	5	uA	

Note :

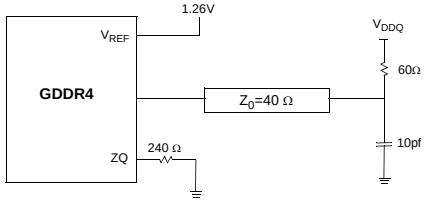
1. Under all conditions, VDDQ must be less than or equal to VDD.
2. VREF is expected to equal 70% of VDDQ for the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed ± 2 percent of the DC value. Thus, from 70% of VDDQ, VREF is allowed ± 25mV for DC error and an additional ±25mV for AC noise.
3. The DC values define where the input slew rate requirements are imposed, and the input signal must not violate these levels in order to maintain a valid level. The inputs require the AC value to be achieved during signal transition edge and the driver should achieve the same slew rate through the AC values.
4. Input and output slew rate =3V/ns. If the input slew rate is less than 3V/ns, input timing may be compromised. All slew rnate are measured between Vih and Vil. DQ and DM input slew rate must not deviate from DQS by more than 10%. If the DQ,DM and DQS slew rate is less than 3V/ns, timing is longer than referenced to the mid-point but to the VIL(AC) maximum and VIH(AC) minimum points.
5. VIH overshoot : VIH(max) = VDDQ + 0.5V for a pulse width ≤ 500ps and the pulse width can not be greater than 1/3 of the cycle rate.
   VIL undershoot : VIL(min)=0.0V for a pulse width ≤ 500ps and the pulse width can not be greater than 1/3 of the cycle rate.

9.3 CLOCK INPUT OPERATING CONDITIONS

Recommended operating conditions (0°C ≤ Tc ≤85°C ; VDD=1.8V ± 0.09V, VDDQ=1.8V ± 0.09V)

Parameter/ Condition	Symbol	Min	Max	Unit	Note
Clock Input Mid-Point Voltage ; CK and /CK	VMP(DC)	VREF-0.1	VREF+0.1	V	1,2,3
Clock Input Voltage Level; CK and /CK	VIN(DC)	0.42	VDDQ + 0.3	V	2
Clock Input Differential Voltage ; CK and /CK	VID(DC)	0.22	VDDQ + 0.5	V	2,4
Clock Input Differential Voltage ; CK and /CK	VID(AC)	0.50	VDDQ + 0.3	V	4
Clock Input Crossing Point Voltage ; CK and /CK	VIX(AC)	VREF - 0.15	VREF + 0.15	V	3

Note : 1. This provides a minimum of 1.16V to a maximum of 1.36V, and is always 70% of VDDQ
2. For AC operations, all DC clock requirements must be satisfied as well.
3. The value of VIX is expected to equal 70% VDDQ for the transmitting device and must track variations in the DC level of the same.
4. VID is the magnitude of the difference between the input level in CK and the input level on /CK.
5. The CK and /CK input reference level (for timing referenced to CK and /CK) is the point at which CK and /CK cross; the input reference level for signals other than CK and /CK is VREF.
6. CK and /CK input slew rate must be ≥ 4V/ns



Output Load Circuit

Note : 1 . Outputs measured into equivalent load of 10pf at a driver impedance of 40 Ω.

9.4 CAPACITANCE

(VDD=1.8V, TA= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance (CK, $\overline{CK}$)	C_{IN1}	1.0	2.0	pF
Input capacitance (A0~A11, BA0~BA2)	C_{IN2}	1.0	2.5	pF
Input capacitance ($\overline{CKE}$, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN3}	1.0	2.5	pF
Data & DQS input/output capacitance(DQ0~DQ31)	C_{OUT}	1.0	2.0	pF
Input capacitance(DM0 ~ DM3)	C_{IN4}	1.0	2.0	pF

9.5 DC characteristics

(0°C ≤ Tc ≤85°C ; VDD=1.8V ± 0.09V, VDDQ=1.8V ± 0.09V)

Parameter	Symbol	Test Condition	Version			Unit
			-07	-08	-09	
Operating Current (One Bank Active)	ICC1	Burst Length=8 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	684	611	586	mA
Precharge Standby Current in Power-down mode	ICC2P	$\overline{CKE}$ ≥VIH(min), tCC= tCC(min)	135	123	116	mA
Precharge Standby Current in Non Power-down mode	ICC2N	$\overline{CKE}$ ≤ VIL(max), $\overline{CS}$≥ VIH(min), tCC= tCC(min)	235	211	198	mA
Active Standby Current power-down mode	ICC3P	$\overline{CKE}$ ≥VIH(min), tCC= tCC(min)	174	156.3	147	mA
Active Standby Current in Non Power-down mode	ICC3N	$\overline{CKE}$ ≤ VIL(max), $\overline{CS}$ ≥ VIH(min), tCC= tCC(min)	596	530	493	mA
Operating Current (Burst Mode)	ICC4	IOL=0mA ,tCC= tCC(min), Page Burst, All Banks activated.	1310	1190	1130	mA
Refresh Current	ICC5	tRC≥ tRFC	526	464	451	mA
Self Refresh Current	ICC6	$\overline{CKE}$ ≤ 0.2V	45	45	45	mA
Operating Current (4Bank interleaving)	ICC7	Burst Length=8 tRC ≥ tRC(min) IOL=0mA, tCC= tCC(min)	1186	1044	968	mA

Note : 1. Measured with outputs open and ODT off
2. Refresh period is 32ms.

9.6 AC characteristics (I)

Parameter		Symbol	-06*		-07		-08		-09		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
DQS out access time from CK		t_{DQSCK}	-0.15	0.15	-0.16	0.16	-0.19	0.19	-0.2	0.2	ns	
CK high-level width		t_{CH}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low-level width		t_{CL}	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK cycle time	CL=19	t_{CK}	-06								tCK	
	CL=18	t_{CK}	-07	-	-07	-	-	-	-	-	tCK	
	CL=17	t_{CK}	-07A	-	-07A	-	-	-	-	-	tCK	
	CL=16	t_{CK}	-08	-	-08	-	-08	-	-	-	tCK	
	CL=15	t_{CK}	-09	-	-09	-	-09	-	-09	-	tCK	
	CL=14	t_{CK}	-1A	-	-1A	-	-1A	-	-1A	-	tCK	
Write Latency		t_{WL}		6		6		6		6	tCK	
DQ and DM input setup time relative to DQS		t_{DS}	0.11	-	0.12	-	0.12	-	0.13	-	ns	
DQ and DM input hold time relative to DQS		t_{DH}	0.11	-	0.12	-	0.12	-	0.13	-	ns	
Active termination setup time		t_{ATS}	10	-	10	-	10	-	10	-	ns	
Active termination hold time		t_{ATH}	10	-	10	-	10	-	10	-	ns	
DQS input high pulse width		t_{DQSH}	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
DQS input low pulse width		t_{DQSL}	0.48	0.52	0.48	0.52	0.48	0.52	0.48	0.52	tCK	
Data strobe edge to Dout edge		t_{DQSQ}	-	0.11	-	0.11	-	0.11	-	0.12	ns	
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	5
DQS read postamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Write command to first DQS latching transition		t_{DQSS}	WL-0.2	WL+0.2	WL-0.2	WL+0.2	WL-0.2	WL+0.2	WL-0.2	WL+0.2	tCK	
DQS write preamble		t_{WPRE}	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	1
DQS write postamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	2
Half strobe period		t_{HP}	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCK	
Data output hold time from DQS		t_{QH}	tHP-0.11	-	tHP-0.11	-	tHP-0.11	-	tHP-0.12	-	ns	
Data-out high-impedance window from CK and /CK		t_{HZ}	-0.25	-	-0.3	-	-0.3	-	-0.3	-	ns	3
Data-out low-impedance window from CK and /CK		t_{LZ}	-0.25	-	-0.3	-	-0.3	-	-0.3	-	ns	3
Address and control input hold time		t_{IH}	0.22	-	0.23	-	0.24	-	0.25	-	ns	
Address and control input setup time		t_{IS}	0.22	-	0.23	-	0.24	-	0.25	-	ns	
Address and control input pulse width		t_{IPW}	0.55	-	0.65	-	0.65	-	0.7	-	ns	
Jitter over 1~6 clock cycle error		tJ	-	0.03	-	0.03	-	0.03	-	0.03	tCK	4
Cycle to cyde duty cycle error		tDCERR	-	0.03	-	0.03	-	0.03	-	0.03	tCK	
Rise and fall times of CK		tR, tF	-	0.2	-	0.2	-	0.2	-	0.2	tCK	

Note: -06*(3.2Gbps) is a target spec and VDD/VDDQ = 1.95V ± 0.05V.

AC CHARACTERISTICS (II)

Parameter	Symbol	-06		-07		-08		-09		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Row active time	t_{RAS}	40	100K	40	100K	35	100K	32	100K	tCK	
Row cycle time	t_{RC}	57		57		50		46		tCK	
Refresh row cycle time	t_{RFC}	71		71		62		57		tCK	
RAS to CAS delay for Read	t_{RCDR}	18		18		16		15		tCK	
RAS to CAS delay for Write	t_{RCDW}	14		14		12		11		tCK	
Row precharge time	t_{RP}	17		17		15		14		tCK	
Row active to Row active	t_{RRD}	14		14		12		11		tCK	
Last data in to Row precharge(PRE or Auto-PRE)	t_{WR}	17		17		15		14		tCK	
Last data in to Read command	t_{CDLR}	9		9		8		8		tCK	
Mode register set cycle time	t_{MRD}	11		11		10		9		tCK	
Auto precharge write recovery time + Precharge	t_{DAL}	34		34		30		28		tCK	
Exit self refresh to Read command	t_{XSR}	20K		20K		20K		20K		tCK	
Exit self refresh to Non-Read command	t_{XSNR}	120		120		120		110		tCK	
Power-down exit time	t_{PDEX}	12tck +tIS		12tck +tIS		10tck +tIS		9tck +tIS		tCK	
Four Activate Window time	t_{FAW}	70		70		60		55		tCK	
CKE minimum pulse width (High and Low pluse width)	t_{CKE}	5		5		5		5		tCK	
Refresh interval time	t_{REF}	-	3.9	-	3.9	-	3.9	-	3.9	us	

Note :

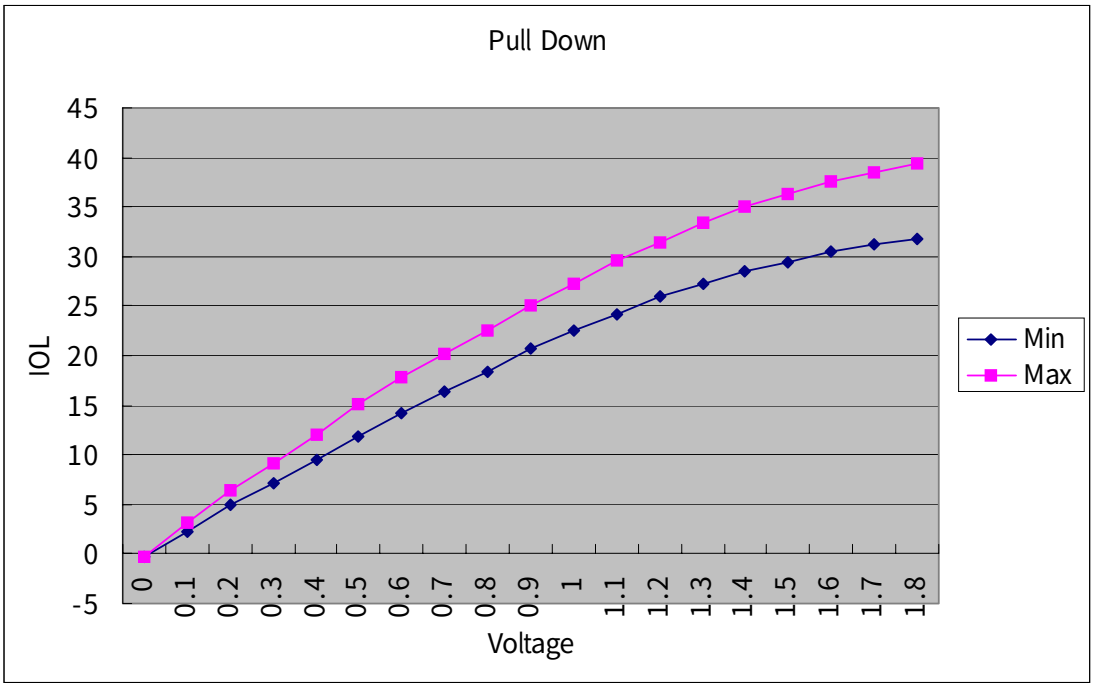
1. A low to high transition on the WDQS line is not allowed in the half clock prior to the write preamble.
2. The last rising edge of WDQS after the write postamble must be riven high by the controller. WDQS can not be pulled high by the on-die termination alone.
3. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referenced to a specific voltage level, but specify when the device output is no longer driving (HZ) or begins driving (LZ).
4. The cycle to cycle jitter over 1~6 cycle short term jitter
5. If Multi-preamble is enable,

10.0 IBIS : I/V Characteristics for Input and Output Buffers

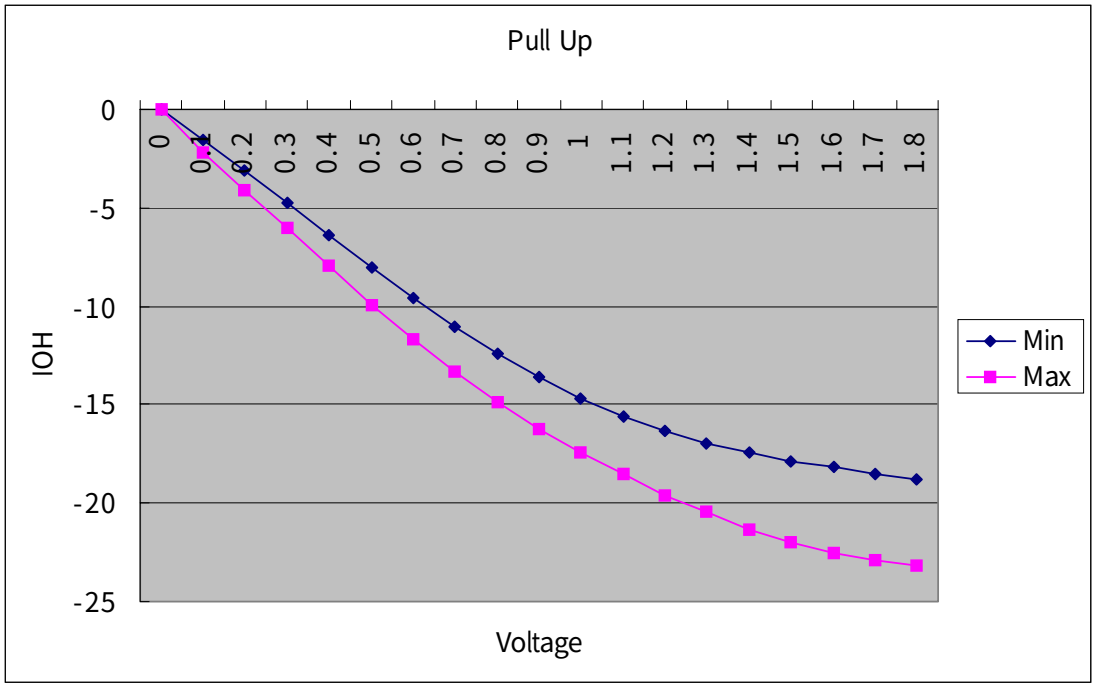
Pull down (40 Ω) & Pull up(60 Ω)

	Pulldown Current (mA)		Pullup Current (mA)	
Voltage (V)	Minimum	Maximum	Minimum	Maximum
0.1	2.25	3.12	-1.56	-2.21
0.2	4.89	6.45	-3.07	-4.12
0.3	7.21	9.16	-4.7	-5.99
0.4	9.56	12.01	-6.36	-7.95
0.5	11.78	15.1	-8.04	-9.99
0.6	14.21	17.75	-9.6	-11.68
0.7	16.43	20.11	-11.08	-13.31
0.8	18.45	22.54	-12.4	-14.89
0.9	20.75	25.13	-13.64	-16.25
1.0	22.45	27.32	-14.68	-17.43
1.1	24.12	29.58	-15.6	-18.48
1.2	26.02	31.44	-16.36	-19.62
1.3	27.21	33.43	-16.96	-20.45
1.4	28.59	34.97	-17.44	-21.32
1.5	29.46	36.33	-17.88	-21.96
1.6	30.42	37.53	-18.2	-22.54
1.7	31.23	38.41	-18.52	-22.89
1.8	31.8	39.43	-18.8	-23.19

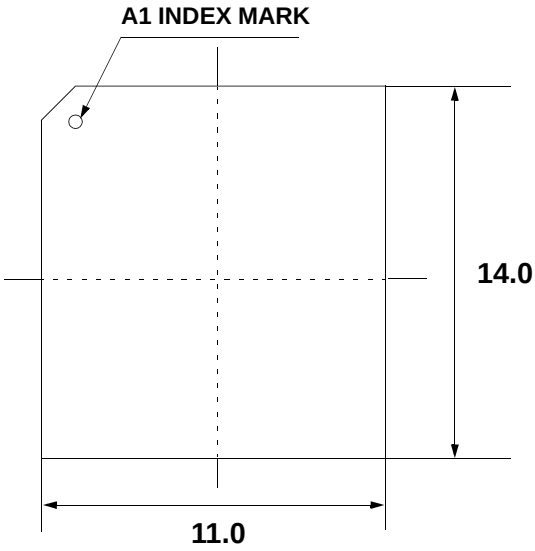
1) Pull down (40 Ω)



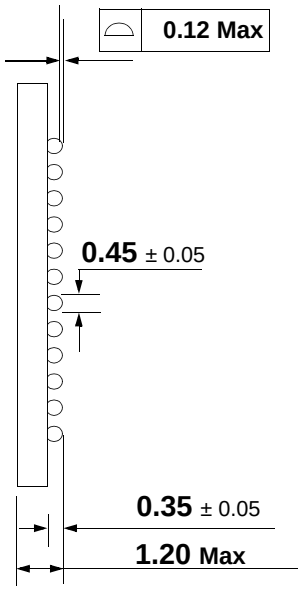
2) Pull down (60 Ω)

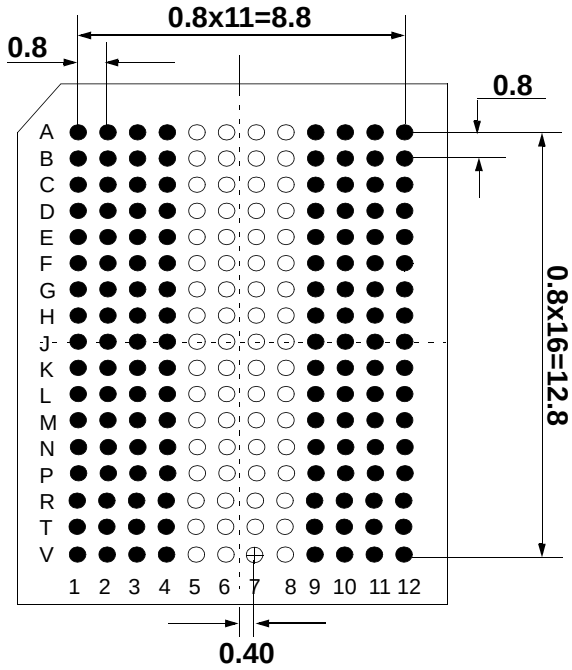


11.0 PACKAGE DIMENSIONS (FBGA)



<Top View>





<Top View: See the balls through the package>

● Ball existing
○ Depopulated ball