

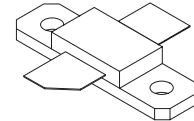
The RF MOSFET Line
RF Power Field Effect Transistors
N-Channel Enhancement-Mode Lateral MOSFETs

MRF21010R1
MRF21010SR1

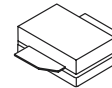
Designed for W-CDMA base station applications with frequencies from 2110 to 2170 MHz. Suitable for FM, TDMA, CDMA and multicarrier amplifier applications. To be used in Class AB for PCN-PCS/cellular radio and WLL applications.

2170 MHz, 10 W, 28 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs

- Typical W-CDMA Performance: -45 dBc ACPR, 2140 MHz, 28 Volts, 5 MHz Offset/4.096 MHz BW, 15 DTCH
Output Power — 2.1 Watts
Power Gain — 13.5 dB
Efficiency — 21%
- High Gain, High Efficiency and High Linearity
- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Capable of Handling 10:1 VSWR @ 28 Vdc, 2170 MHz, 10 Watts CW Output Power
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 Inch Reel.



CASE 360B-05, STYLE 1
NI-360
MRF21010R1



CASE 360C-05, STYLE 1
NI-360S
MRF21010SR1

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	Vdc
Gate-Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	43.75 0.25	W W/ $^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Junction Temperature	T_J	200	$^\circ\text{C}$

ESD PROTECTION CHARACTERISTICS

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

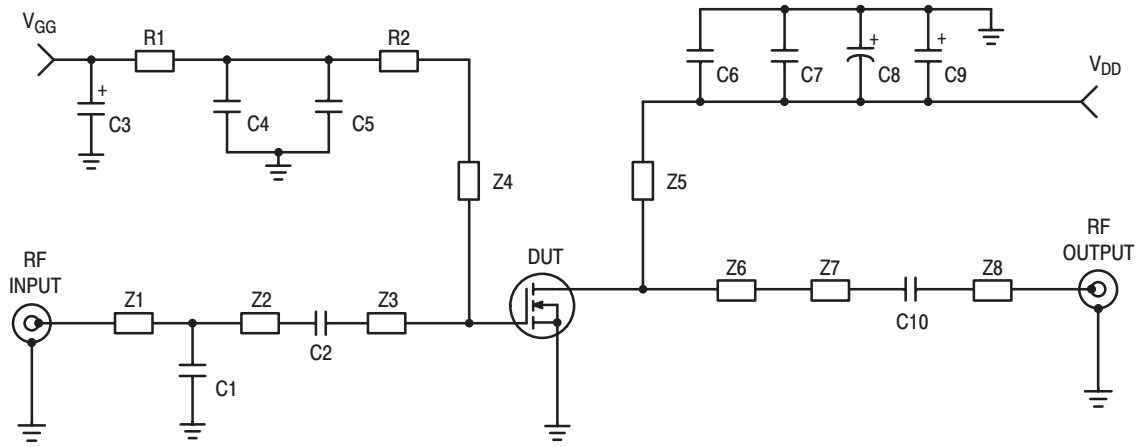
THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	5.5	$^\circ\text{C/W}$

NOTE - **CAUTION** - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain–Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 10\ \mu\text{A}$)	$V_{(BR)DSS}$	65	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	10	μAdc
Gate–Source Leakage Current ($V_{GS} = 5\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	1	μAdc
ON CHARACTERISTICS					
Gate Threshold Voltage ($V_{DS} = 10\text{ V}$, $I_D = 50\ \mu\text{A}$)	$V_{GS(th)}$	2.5	3	4	Vdc
Gate Quiescent Voltage ($V_{DS} = 28\text{ V}$, $I_D = 100\text{ mA}$)	$V_{GS(Q)}$	2.5	4	4.5	Vdc
Drain–Source On–Voltage ($V_{GS} = 10\text{ V}$, $I_D = 0.5\text{ A}$)	$V_{DS(on)}$	—	0.4	0.5	Vdc
Forward Transconductance ($V_{DS} = 10\text{ V}$, $I_D = 1\text{ A}$)	g_{fs}	—	0.95	—	S
DYNAMIC CHARACTERISTICS					
Reverse Transfer Capacitance ($V_{DS} = 28\text{ Vdc}$, $V_{GS} = 0$, $f = 1\text{ MHz}$)	C_{rss}	—	1	—	pF
FUNCTIONAL TESTS (In Motorola Test Fixture, 50 ohm system)					
Two–Tone Common Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	G_{ps}	12	13.5	—	dB
Two–Tone Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	η	31	35	—	%
Third Order Intermodulation Distortion ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	IMD	—	–35	–30	dBc
Input Return Loss ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W PEP}$, $I_{DQ} = 100\text{ mA}$, $f_1 = 2110\text{ MHz}$, $f_2 = 2170\text{ MHz}$, Tone Spacing = 100 KHz)	IRL	—	–12	–10	dB
Output Power, 1 dB Compression Point, CW ($V_{DD} = 28\text{ Vdc}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$)	P1dB	—	11	—	W
Common–Source Amplifier Power Gain ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$)	G_{ps}	—	12	—	dB
Drain Efficiency ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$)	η	—	42	—	%
Output Mismatch Stress ($V_{DD} = 28\text{ Vdc}$, $P_{out} = 10\text{ W CW}$, $I_{DQ} = 100\text{ mA}$, $f = 2170\text{ MHz}$, VSWR = 10:1, All Phase Angles at Frequency of Tests)	Ψ	No Degradation In Output Power Before and After Test			



Z1	0.964" x 0.087" Microstrip	Z5	0.752" x 0.087" Microstrip
Z2	0.905" x 0.087" Microstrip	Z6	0.453" x 1.118" Microstrip
Z3	0.433" x 0.512" Microstrip	Z7	0.921" x 0.154" Microstrip
Z4	1.068" x 0.087" Microstrip	Z8	0.925" x 0.087" Microstrip

Figure 1. MRF21010 Test Circuit Schematic

Table 1. MRF21010 Test Circuit Component Designations and Values

Part	Description	Value, P/N or DWG	Manufacturer
C1 *	(eared) 2.2 pF Chip Capacitor, B Case	100B2R2BW	ATC
	(earless) 1.8 pF Chip Capacitor, B Case	100B1R8BW	ATC
C2	0.5 pF Chip Capacitor, B Case	100B0R5BW	ATC
C3, C9	10 μ F, 35 V Tantalum Chip Capacitors	293D106X9035D2T	Sprague-Vishay
C4, C7	1 nF Chip Capacitors, B Case	100B102JW	ATC
C5, C6	5.6 pF Chip Capacitors, B Case	100B5R6BW	ATC
C8	470 μ F, 63 V Electrolytic Capacitor		
C10	10 pF Chip Capacitor, B Case	100B100GW	ATC
N1, N2	Type N Connector Flange Mounts	3052-1648-10	Macom
R1	1.0 k Ω Chip Resistor (0805)		
R2	12 Ω Chip Resistor (0805)		
PCB	Etched Circuit Board	C-XM-00-001-01	Cibel
Raw PCB material	0.030" Glass Teflon [®] ($\epsilon_r = 2.55$)	TLX8-0300	Taconic

* Piece part depending on eared / earless version of the device.

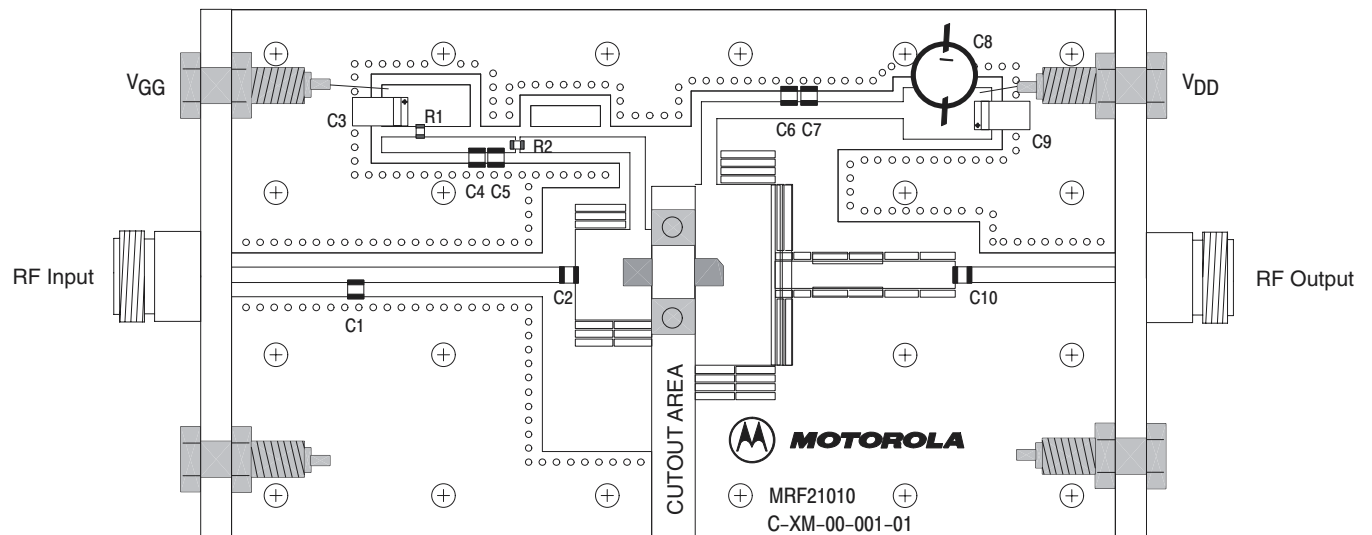


Figure 2. MRF21010 Test Circuit Component Layout

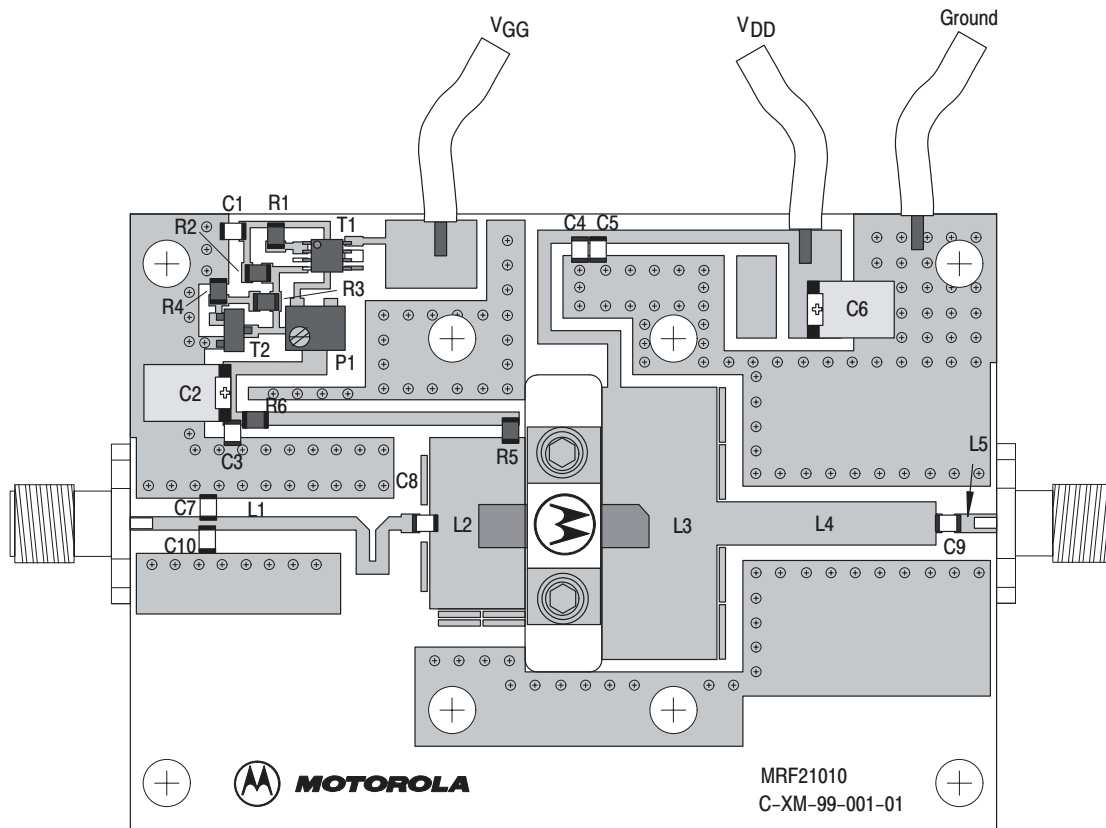


Figure 3. MRF21010 Demonstration Board Component Layout

Table 2. MRF21010 Demonstration Board Component Designations and Values

Designators	Description
C1	1 μ F Chip Capacitor (0805), AVX #08053G105ZATEA
C2, C6	10 μ F, 35 V Tantalum Capacitors, Vishay–Sprague #293D106X9035D
C3, C4	6.8 pF Chip Capacitors, ACCU–P (0805), AVX #08051J6R8CBT
C5	10 nF Chip Capacitor (0805), AVX #08055C103KATDA
C7	1.5 pF Chip Capacitor, ACCU–P (0805), AVX #08051J2R2BBT
C8, C10	0.5 pF Chip Capacitors, ACCU–P (0805), AVX #08051J0R5BBT
C9	10 pF Chip Capacitor, ACCU–P (0805), AVX #08055J100GBT
L1	19 mm \times 1.07 mm
L2	7.7 mm \times 13.8 mm
L3	9.3 mm \times 22 mm
L4	17.7 mm \times 3.5 mm
L5	3.4 mm \times 1.5 mm
R1, R6	10 Ω , 1/8 W Chip Resistors (0805)
R2, R3	1 k Ω , 1/8 W Chip Resistors (0805)
R4	2.2 k Ω , 1/8 W Chip Resistor (0805)
R5	0 Ω , 1/8 W Chip Resistor (0805)
P1	5 k Ω Potentiometer CMS Cermet Multi–Turn, Bourns #3224W
T1	Voltage Regulator, Micro–8, Motorola #LP2951
T2	Bipolar NPN Transistor, SOT–23, Motorola #BC847
	RF Connectors Type SMA, Johnson #142–0701–631
	Substrate: Rogers RO4350, Thickness 0.5 mm, $\epsilon_r = 3.53$

TYPICAL CHARACTERISTICS

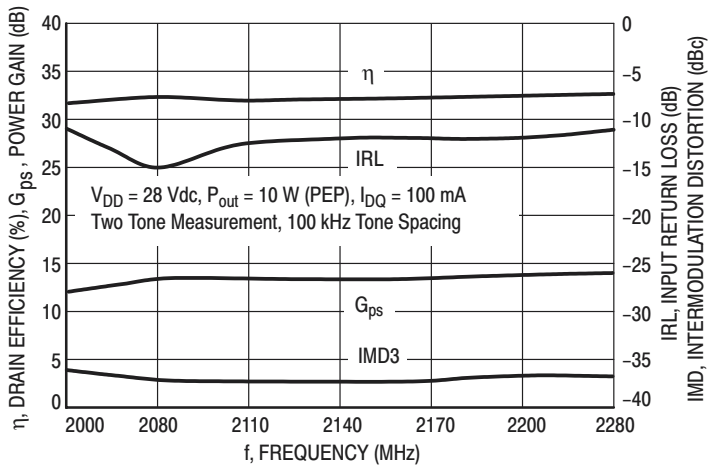


Figure 4. Class AB Broadband Circuit Performance

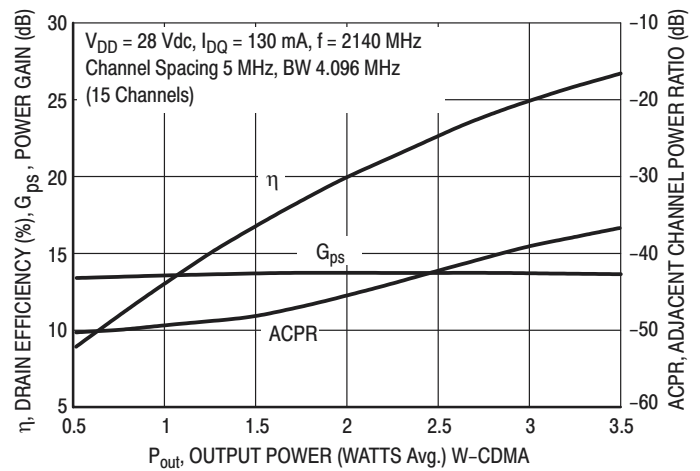


Figure 5. W-CDMA ACPR, Power Gain and Drain Efficiency versus Output Power

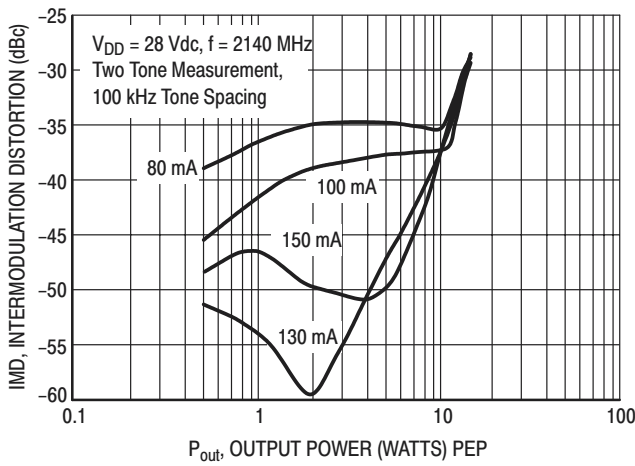


Figure 6. Intermodulation Distortion versus Output Power

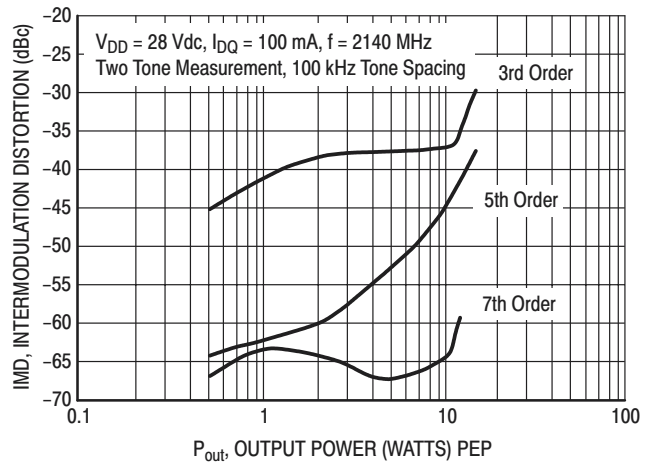


Figure 7. Intermodulation Distortion Products versus Output Power

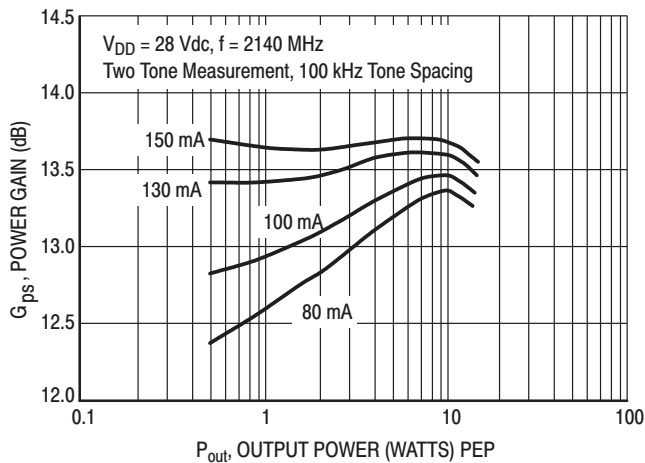


Figure 8. Power Gain versus Output Power

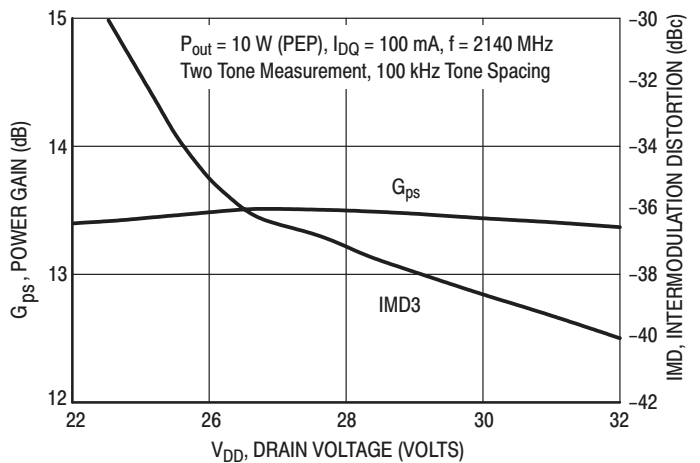
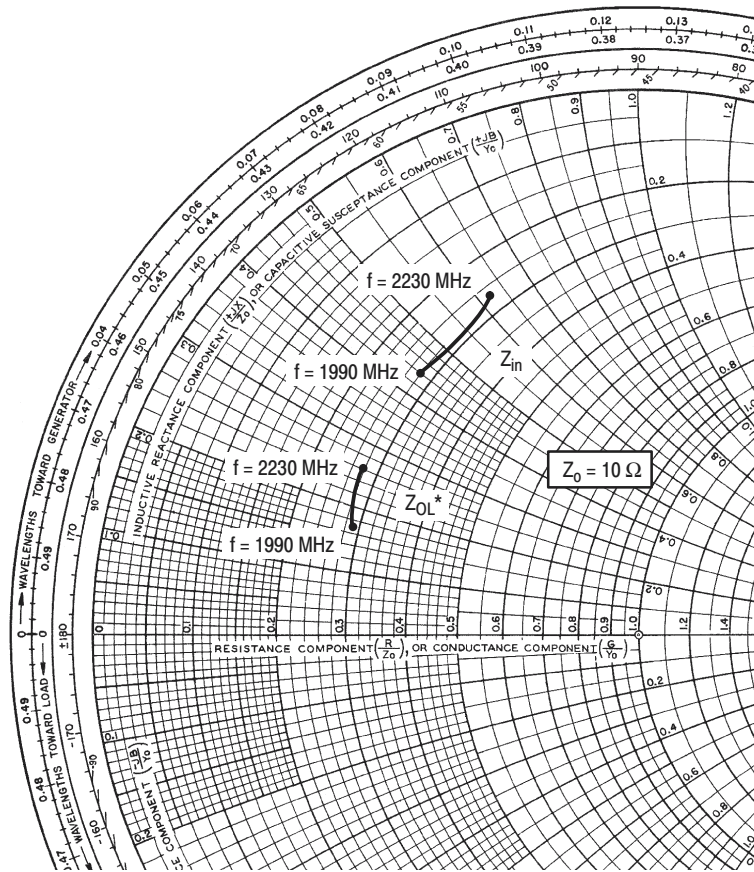


Figure 9. Intermodulation and Gain versus Supply Voltage



$V_{DD} = 28\text{ V}$, $I_{DQ} = 100\text{ mA}$, $P_{out} = P_{1dB\text{ CW}}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
1990	$2.85 + j4.38$	$2.93 + j1.71$
2110	$2.89 + j5.04$	$2.76 + j2.28$
2230	$2.73 + j6.19$	$2.83 + j2.59$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the optimum load impedance at a given output power, voltage, IMD, bias current and frequency.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, output power, drain efficiency and intermodulation distortion.

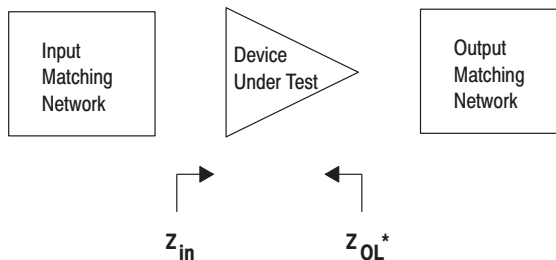
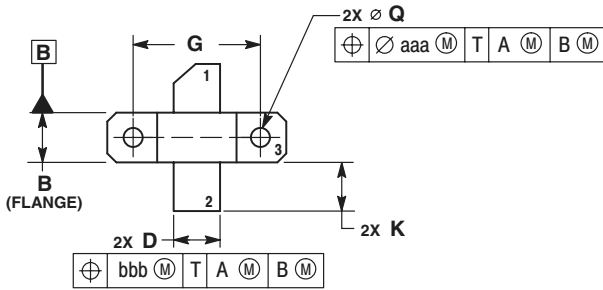


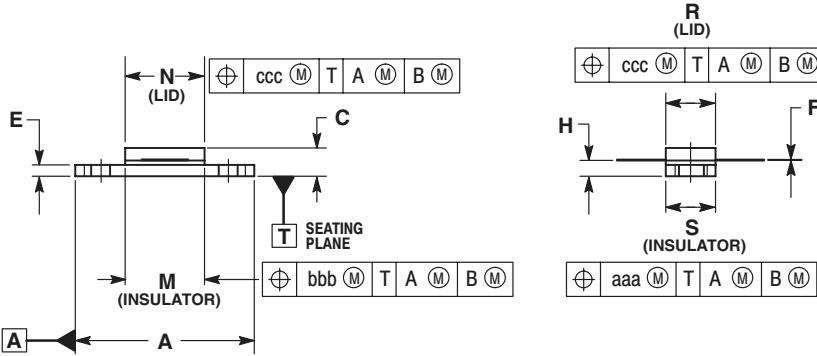
Figure 10. Series Equivalent Input and Output Impedance

PACKAGE DIMENSIONS



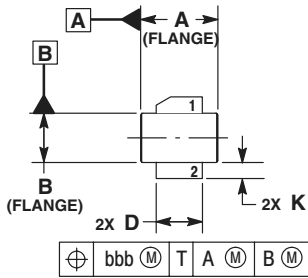
- NOTES:
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 - CONTROLLING DIMENSION: INCH.
 - DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.225	0.235	5.72	5.97
C	0.125	0.175	3.18	4.45
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.10	0.15
G	0.562 BSC		14.28 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
Q	0.125	0.135	3.18	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	



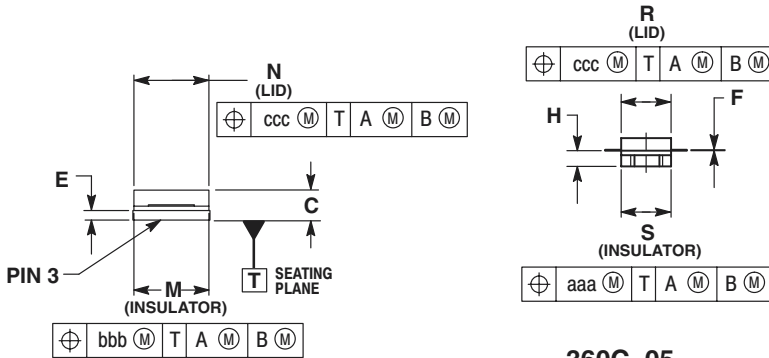
- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**CASE 360B-05
 ISSUE F
 NI-360
 MRF21010R1**




- NOTES:
- INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
 - CONTROLLING DIMENSION: INCH.
 - DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.375	0.385	9.53	9.78
B	0.225	0.235	5.72	5.97
C	0.105	0.155	2.67	3.94
D	0.210	0.220	5.33	5.59
E	0.035	0.045	0.89	1.14
F	0.004	0.006	0.10	0.15
H	0.057	0.067	1.45	1.70
K	0.085	0.115	2.16	2.92
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
R	0.227	0.23	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	



- STYLE 1:
 PIN 1. DRAIN
 2. GATE
 3. SOURCE

**360C-05
 ISSUE D
 NI-360S
 MRF21010SR1**

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