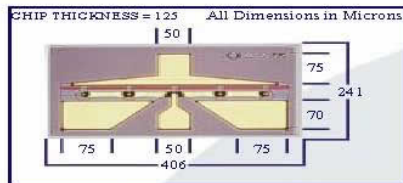


# MwT-3

## 26 GHz High Power GaAs FET



DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



### FEATURES

- 11 dB SMALL SIGNAL GAIN AT 12 GHz
- +21.0 dBm OUTPUT POWER AT 12 GHz
- 0.3 MICRON REFRACTORY METAL/GOLD GATE
- 300 MICRON GATE WIDTH
- CHOICE OF CHIP AND THREE PACKAGE TYPES

### DESCRIPTION

The MwT-3 is a GaAs MESFET device whose nominal quarter-micron gate length and 300 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 26 GHz frequency range with power outputs ranging from +18 to +21 dBm. The straight geometry of the MwT-3 makes it equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal system and devices from each wafer are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

### DC SPECIFICATIONS AT Ta = 25°C

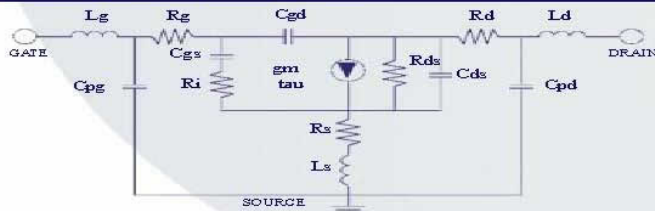
SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 4.0 V VGS= 0.0 V	mA	30		120
Gm	Transconductance Vds= 4.0 V VGS= 0.0 V	mS	35	55	
Vp	Pinch-off Voltage Vds= 3.0 V IDS= 2.0 mA	V		-2.0	-5.0
BVGS0	Gate-to-Source Breakdown Volt. Igs= -0.2 mA	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= -0.2 mA	V	-8.0	-12.0	
Rth	Thermal Resistance MwT-3 Chip, 371 Resistance MwT-370, 373	°C/W			150 320*

\*Overall Rth depends on case mounting.

### RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 6.0 V IDS= 0.6 x IDSS	12 GHz	dBm	20.0	21.0
SSG	Small Signal Gain VDS= 6.0 V IDS= 0.6 x IDSS	12 GHz	dB	10.0	11.0
PAE	Power Added Efficiency VDS= 6.0 V IDS= 0.6 x IDSS	12 GHz	%	30	35
IDSS	Recommended IDSS Range for Optimum P1dB		mA		80-110

### DEVICE EQUIVALENT CIRCUIT MODEL



### PARAMETER

### VALUE

Source Resistance	Rs	1.48	Ω
Source Inductance	Ls	0.034	nH
Drain-Source Resistance	Rds	253	Ω
Drain-Source Capacitance	Cds	0.074	pF
Drain Resistance	Rd	3.11	Ω
Drain Pad Capacitance	Cpd	0.012	pF
Drain Inductance	Ld	0.227	nH
Gate Bond Wire Inductance	Lg	0.136	nH
Gate Pad Capacitance	Cpg	0.034	pF
Gate Resistance	Rg	0.314	Ω
Gate-Source Capacitance	Cgs	0.348	pF
Channel Resistance	Ri	5.78	Ω
Gate-Drain Capacitance	Cgd	0.022	pF
Transconductance	gm	51.0	mS
Transit Time	tau	3.7	psec

### ORDERING INFORMATION

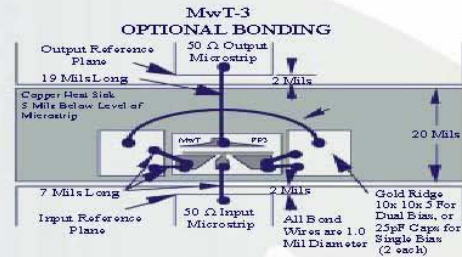
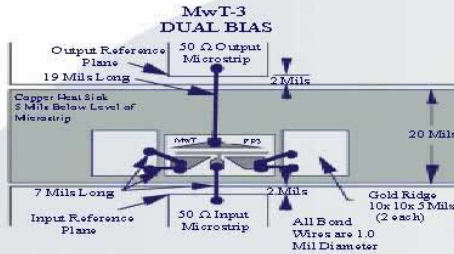
Chip	MwT-3
Package 70	MwT-370
Package 71	MwT-371
Package 73	MwT-373

### NOTE:

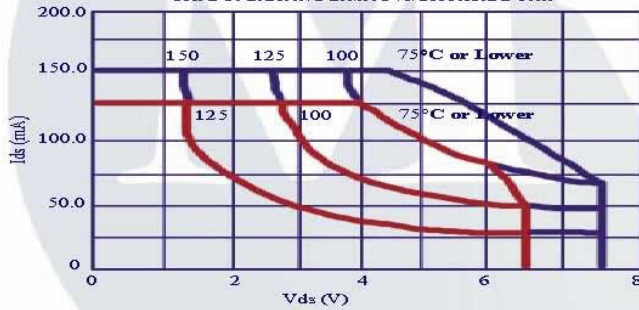
For Package information, please see supplementary application note from our website at [www.mwtinc.com](http://www.mwtinc.com). When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.

4268 Solar Way, Fremont, CA 94538 | Email [sales@mwtinc.com](mailto:sales@mwtinc.com) | Phone (510) 651-6700 | Fax (510) 952-4000

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SAFE OPERATING LIMITS vs. BACKSIDE CHIP



■ Absolute Maximum    ■ Continuous Maximum

**MAXIMUM RATINGS AT  $T_a = 25^\circ\text{C}$**

SYMBOL	PARAMETER	UNITS	CONT MAX <sup>1</sup>	ABSOLUTE MAX <sup>2</sup>
VDS	Drain to Source Voltage	V	See Safe Operating Limits	+175
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	R.F. Input Power	mW	120	180

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean time-to-failure below the design goals.  
 2. Exceeding any one of these limits may cause permanent damage.

**Bin Selection Guide**

Bin No.	A	B	C
Idss	30-	55-	95-
Range	55mA	95mA	120mA

**BIN ACCURACY STATEMENT**

*When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.*