ML6682

Token Ring Physical Interface

GENERAL DESCRIPTION

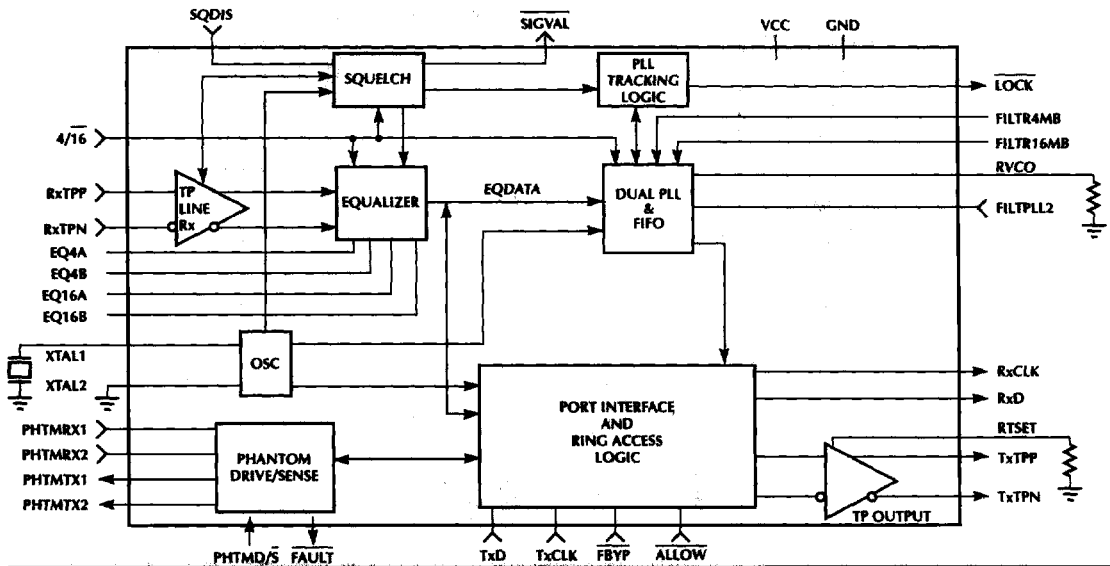
The ML6682 Token Ring Physical Interface Circuit is designed for use as a token ring concentrator port interface in 4Mb/s and 16Mb/s ISO/IEC 8802-5 networks using unshielded twisted pair (UTP) or shielded twisted pair (STP) cable. It can also be configured as a Ring-In or Ring-Out port for concentrator interface to the main network trunk. It includes a receiver equalizer for suppression of inter-symbol distortion, a narrow-bandwidth master PLL with a constant-gain phase/frequency detector for enhanced clock tracking and low VCO phase distortion, an 8 UI FIFO and slave PLL for additional jitter attenuation, internal frequency/phase tracking select logic, and a waveshaping twisted pair transmit driver which requires only a very simple external filter to meet the ISO/IEC 8802-5 standard. The circuit also includes phantom wire fault detection and output drivers for use with an external phantom switching mechanism in a concentrator-to-trunk interface application. The part has an on-chip single-pin crystal oscillator designed for a 16MHz crystal. It can also be used with an external clock of 32MHz frequency. The part uses a frequency squelch circuit at the twisted pair receiver to allow detection of incorrect network speed.

External components are minimized by the use of internally-controlled station fault, receiver pulse width squelch, on-chip crystal oscillator, and internal 4/16 Mbps switching logic. The ML6682 performs the hybrid switching functions, eliminating the need for relays. Isolation can be achieved optically.

FEATURES

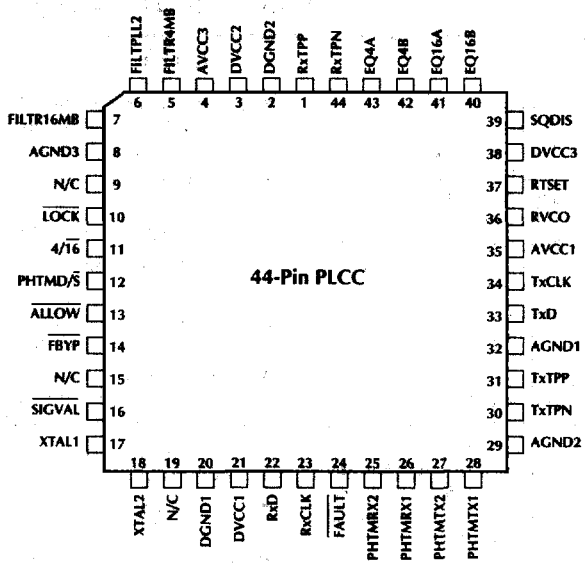
- Supports dual PLL jitter attenuator and clock regeneration for each lobe port and Ring In/Ring Out ports for UTP/STP extended distance concentrators.
- Compatible with ISO/IEC 8802-5-1989 standard for Token Ring
- Pin selectable 16 and 4Mb/s data rates
- Supports dual ring fault tolerant Ring In/ Ring Out trunks
- Fault isolation capability at each concentrator port available for network management.
- Provides dual phase-locked loop with single edge constant gain phase detector and 8 UI FIFO for clock regeneration, jitter attenuation and data recovery.
- Phantom voltage drive/sense for both transmit and receive cable pairs.
- On-chip crystal oscillator can also be driven by external clock.
- On-chip receiver channel equalization switchable for both 4 and 16 Mbps

BLOCK DIAGRAM

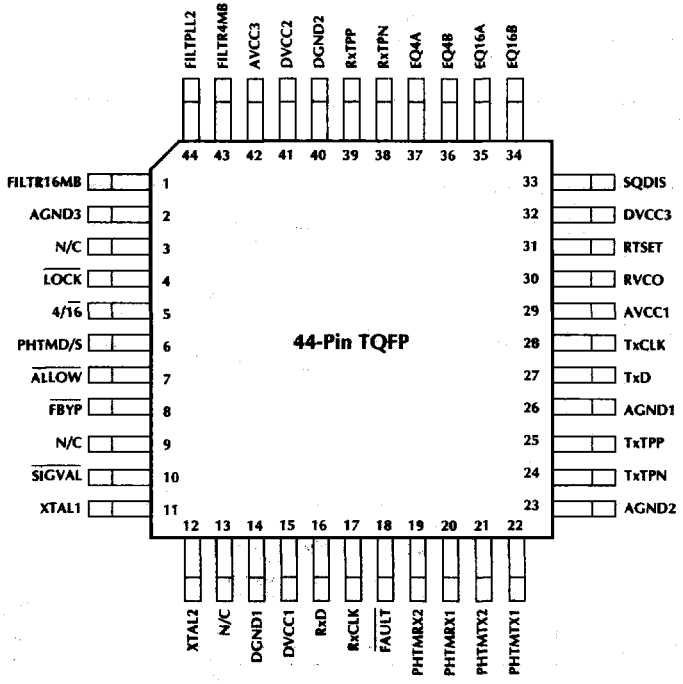


PIN CONFIGURATIONS

ML6682
44-Pin PLCC (Q44)



ML6682
44-Pin TQFP (H44)



PIN DESCRIPTION (For PLCC Package)

PIN #	NAME	FUNCTION
1 44	RxTPP RxTPN	Receive wire pair inputs. These inputs receive data from the twisted pair media through the receive isolation transformer. The common-mode bias point for these pins is set internally.
2 20	DGND2 DGND1	Digital ground pins.
3 21 38	DVCC2 DVCC1 DVCC3	Positive power supply pins (+5V) for digital part of the chip.
4 35	AVCC3 AVCC1	Positive power supply pins (+5V) for analog part of the chip.
5	FILTR4MB	4Mbps PLL filter input. Connection point for external PLL filter components for 4 Mbps data rate.
6	FILTPLL2	Second PLL filter input. Connection point for external PLL filter components for second (slave) PLL.
7	FILTR16MB	16 Mbps PLL filter input. Connection point for external PLL filter components for 16 Mbps data rate.
8 29 32	AGND3 AGND2 AGND1	Analog ground pins.
9	N/C	
10	$\overline{LOCK}$	PLL phase lock indicator output. This output goes low when both PLLs achieve lock. May be externally gated with $\overline{FBYP}$ for zero delay lockout. (Prevent a 4 Mbps station from entering a 16 Mbps Ring).
11	4/$\overline{16}$	Data rate selection input. A logic one selects 4 Mbps operation. A logic zero selects 16 Mbps operation. The pin automatically switches the receive equalizer and the PLL loop filter for the appropriate data rate.
12	PHTMD/$\overline{S}$	"Phantom drive/sense" select input. When set low, the chip is configured for "phantom sense". In the "phantom sense" state PHTMRX1 pin serves as an input coming from an opto-isolator to sense phantom current and PHTMTX1 is an output. When PHTMD/$\overline{S}$ is set high, the chip is configured for "phantom drive". In the "phantom drive" state PHTMTX1 and PHTMTX2 provide the phantom drive and fault detect for the transmit pair of wires, and PHTMRX1 and PHTMRX2 sense fault detect for the receive pair of wires.
13	$\overline{ALLOW}$	$\overline{ALLOW}$ is a digital input that allows the port to control INSERT/BYPASS through phantom current, or allows the port to be forced into INSERT mode using $\overline{FBYP}$.
14	$\overline{FBYP}$	Force Bypass input. This digital input provides network management control to force the ML6682 into BYPASS mode.
15	N/C	
16	$\overline{SIGVAL}$	Valid signal indicator output. This output goes low when the signal at RxTPP/N meets frequency and amplitude squelch requirements.
17	XTAL1	Crystal/external clock input. Connecting a 16MHz crystal between this pin and ground provides the required reference frequency. XTAL2 must be connected to ground when XTAL1 is used.
18	XTAL2	Clock input pin. Connecting a 32MHz external clock between this pin and ground provides the required reference frequency. When XTAL2 is used, XTAL1 must be grounded.
19	N/C	
22	RxD	Receive data output. When the ML6682 is in INSERT mode, RxD is sourced by the PLL reclocked data from receive twisted pair inputs RxTPP, RxTPN. When the ML6682 is in the BYPASS mode, RxD is sourced by the TxD input.
23	RxCLK	Synchronized data clock output. When the ML6682 is in INSERT mode, RxCLK is sourced by the PLL. When the ML6682 is in BYPASS mode, RxCLK is sourced by the TxCLK input.
24	$\overline{FAULT}$	Phantom wire fault detection output. When this output is low, the phantom current test has failed. In the "phantom drive" mode this will be detected as an open or a short by the PHTMTX1, PHTMTX2, PHTMRX1, PHTMRX2 pins. In the "phantom sense" mode, $\overline{FAULT}$ is an output that simply buffers the PHTMRX1 input.
25 26	PHTMRX2 PHTMRX1	Receive pair phantom sense inputs. In the "phantom drive" mode (PHTMD/$\overline{S}$ pin is tied to V_{CC}) these inputs sense phantom current on the receive pair wires to detect a phantom circuit fault condition. In "phantom sense" configuration (PHTMD/$\overline{S}$ pin is tied to GND) PHTMRX1 is the sense input for phantom current coming from an opto isolator and PHTMRX2 should be grounded.

PIN DESCRIPTION (For PLCC Package)

(Continued)

PIN #	NAME	FUNCTION
27 28	PHTMTX2 PHTMTX1	Transmit pair phantom drive/sense pair. In the "phantom drive" mode, these pins output a +5 volt phantom signal and sense opens and shorts as a phantom circuit fault condition. In the "phantom sense" mode, PHTMTX1 is an open collector pin that can be used to drive an LED to reflect the INSERT/BYPASS state. In the INSERT state, PHTMTX1 is low to light the LED and in the BYPASS state PHTMTX1 is high. PHTMTX2 should be left floating in the "phantom sense" mode.
30 31	TxTPN TxTPP	Transmitter wire pair outputs. This differential current output pair drives the network coupling transformer to the transmit wire pair.
33	TxD	Data input from the previous lobe or Ring In/Ring Out port. In INSERT mode TxD is clocked out by TxCLK at the TxTPP and TxTPN pins. In BYPASS mode the TxD input is internally connected to the RxD output.
34	TxCLK	Synchronized data clock input from the previous lobe or Ring In/Ring Out port. In INSERT mode TxCLK clocks TxD out onto the transmit twisted pair at TxTPP, TxTPN. In BYPASS mode the TxCLK input is internally connected to the RxCLK output.
36	RVCO	External resistor input. A precision resistor of the appropriate value connected to this input sets the phase detector gain.
37	RTSET	External resistor input. A precision resistor of the appropriate value connected to this input sets the twisted pair transmitter output level.
39	SQDIS	Squelch disable input. Normally wired to ground. A high level input disables the RX wire pair pulse width squelch function.
40 41	EQ16B EQ16A	Differential connection for external equalization components for 16 Mbps operation. The equalizer is disabled when these two pins are tied together.
42 43	EQ4B EQ4A	Differential connection for external equalization components for 4 Mbps operation. The equalizer is disabled when these two pins are tied together.

ABSOLUTE MAXIMUM RATINGS

V_{CC} Supply Voltage Range 6V
Input Voltage Range
  Digital Inputs ..... GND –0.3V to V_{CC} +0.3V
  TxD, TxCLK, RxTPP,
  RxTPN, XTAL1, XTAL2 ..... GND –0.3V to V_{CC} +0.3V
Output Current
  TxTPP, TxTPN 50mA
  PHTMRX1, PHTMRX2, PHTMTX1, PHTMTX2 ... 25mA
  All Other Outputs 10mA
Junction Temperature ..... 150°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance (θ_{JA})
  PLCC ..... 54°C/W
  TQFP ..... 67°C/W

OPERATING CONDITIONS

V_{CC} Supply Voltage ..... 5V ± 5%
Temperature Range ..... 0°C to 70°C
RTSET ..... 1.66kΩ ± 1%
RVCO ..... 2.42kΩ ± 1%
All V_{CC} supply pins must be within 0.1V of each other.
All GND pins must be within 0.1V of each other.

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ± 5%, RTSET = 1.66kΩ, RVCO = 2.42kΩ, T_A = Operating Temperature Range. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TTL Inputs (4/$\overline{16}$, PHTMD/$\overline{S}$, SQDIS, $\overline{ALLOW}$, TxD, TxCLK, $\overline{FBYP}$)						
V_{IL}	Input Low Voltage	I_{IL} = 400µA			0.8	V
V_{IH}	Input High Voltage	I_{IH} = 100µA	2.0			V
I_{IL}	Input Low Current	All except TxD, TxCLK; V_{IN} = 0.4V	–400			µA
		TxD, TxCLK; V_{IN} = 0.4V	–1600			µA
I_{IH}	Input High Current	V_{IN} = 2.7V			100	µA
TTL Outputs ($\overline{FAULT}$, $\overline{LOCK}$, RxCLK, RxD):						
V_{OL}	Output Low Voltage	I_{OL} = 1mA			0.40	V
V_{OH}	Output High Voltage	I_{OH} = –0.1mA	2.4			V
Receiver						
V_{OSR}	RxTPP–RxTPN Differential Offset Voltage	V_{SQDIS} = V_{IH}	–35		35	mV
V_{IBR}	RxTPP–RxTPN Open-Circuit Common-Mode Bias Voltage		2.6		3.2	V
R_{IDR}	RxTPP–RxTPN Differential Input Resistance	Input differential voltage = 2V, centered at V_{IBR}	10.5		13.5	KΩ
V_{STX}	XTAL1 Input Switching Threshold Voltage		1.5		3.5	V
I_{RTSET}	RTSET Input Current	RTSET = 1.66kΩ	575		625	µA
I_{RVCO}	RVCO Input Current	RVCO = 2.42kΩ	387		438	µA
Transmitter						
I_{TOUT}	TxTPP Differential Output Current	R_L = 100 or 150Ω	28		33	mA
I_{TOFF}	TxTPP–TxTPN Off-state Output Current	$V_{\overline{FBYP}}$ = V_{IL}; R_L = 200Ω			1.5	mA
I_{TXI}	TxTPP–TxTPN Differential Current Imbalance	R_L = 200Ω	–900		900	µA

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Phantom Output Driver (PHTMD/$\overline{S}$ = V_{IH}, except as noted)						
V_{OHP}	PHTMTX1/PHTMTX2 Output High Voltage	I_{OHP} = –1mA	4.1			V
		I_{OHP} = –2mA	3.5			V
I_{OHP}	PHTMTX1/PHTMTX2 Output Short Circuit Current	V_{OHP} = 0V	–2		–0.7	mA
I_{OZP}	PHTMTX1/Tx2/Rx1/Rx2 Output Off Current	PHTMD/$\overline{S}$ = V_{IL} 0V ≤ V_{OHP} ≤ V_{CC}	–100		+100	µA
Phantom Output Fault Sensing (PHTMD/$\overline{S}$ = V_{IH})						
V_{OPN}	$\overline{FAULT}$ Output Voltage, Normal Condition	Notes 3, 4	2.4			V
V_{OPF}	$\overline{FAULT}$ Output Voltage, Fault Condition	Notes 3, 5			0.45	V
Power Supply Current						
I_{CC1}	Supply Current, Transmitting	Note 2			225	mA

AC CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ± 5%, RTSET = 1.66kΩ, RVCO = 2.42kΩ, T_A = Operating Temperature Range. (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Transmitter (Note 9)						
t_{DF01}	TxTPP–TxTPN Output Delay Mismatch, Zeros and Ones	16Mb/s, Note 6A	0.3		1.0	ns
		4Mb/s	–0.5		0.5	ns
t_{DFMX}	TxTPP–TxTPN Output Delay Mismatch, Random Data	4Mb/s & 16Mb/s, Note 6B	–2.0		2.0	ns
t_{DCD}	TxTPP–TxTPN Output Duty Cycle Distortion	16Mb/s, Note 7	–1.5		1.5	ns
		4Mb/s, Note 7	–6.0		6.0	ns
Receiver, General						
t_{RPWL}	Maximum RxTPP-RxTPN Period To Turn On	16Mb/s, RxTP V_{DIFP-P} = 1V	167		244	ns
		4Mb/s, RxTP V_{DIFP-P} = 1V	667		976	ns
t_{RPWS}	Minimum RxTPP-RxTPN Period To Turn On	16Mb/s, RxTP V_{DIFP-P} = 1V	40		59	ns
		4Mb/s, RxTP V_{DIFP-P} = 1V	167		236	ns
t_{PL}	PLL Phase-Lock After Freq. Lock	See Figure 1			1.5	ms
t_{FL}	PLL Frequency-Lock After Power-Up	Power-up to 2BR ± 1% Hz frequency at RxCLK; Note 8			500	ms
t_{DL}	PLL Phase Unlock Time	See Figure 1			100	µs
t_{PVC1}	RxCLK Period, $V_{FILTR4MB}$ = 2.2V	$V_{4/\overline{16}}$ = V_{OH} (4Mb/s), Note 10	225		150	ns
t_{PVC2}	RxCLK Period, $V_{FILTR4MB}$ = 2.8V	$V_{4/\overline{16}}$ = V_{OH} (4Mb/s), Note 10	75		112	ns
t_{PVC3}	RxCLK Period, $V_{FILTR16MB}$ = 2.2V	$V_{4/\overline{16}}$ = V_{OL} (16Mb/s), Note 10	56.3		37.5	ns
t_{PVC4}	RxCLK Period, $V_{FILTR16MB}$ = 2.8V	$V_{4/\overline{16}}$ = V_{OL} (16Mb/s), Note 10	18.8		28	ns
K_d	Phase Detector Gain	4Mb/s; Note 11 and Figure 2	0.25		0.35	µA/ns
		16Mb/s; Note 11 and Figure 2	1.0		1.4	µA/ns
t_{RSTE}	PLL Static Phase Error	Note 12	–2		+2	ns
t_{RDC}	RxD to RxCLK Delay		–2		2	ns
t_{RTD}	RxTP to RxD Delay		1		4	BT
t_{RCFS}	RxCLK 90-10% Fall Time	RxCLK t_{PER} = 31.25ns			5	ns
t_{PTRD}	TxD to RxD Propagation Delay	$V_{\overline{FBYP}}$ = V_{OL}, Figure 4	22		30	ns
t_{PTRC}	TxCK to RxCK Propagation Delay	$V_{\overline{FBYP}}$ = V_{OL}, Figure 4	22		30	ns
t_{SRM}	Setup Time, RxD Valid to RxCLK Rising Edge (1.5V point)	RxCLK t_{PER} = 31.25ns, Figure 4	10			ns
t_{HRM}	Hold Time, RxD Valid After RxCLK Rising Edge (1.5V)	RxCLK t_{PER} = 31.25ns, Figure 4	2			ns
t_{RCRM}	RxCLK 10-90% Rise Time	RxCLK t_{PER} = 31.25ns, C_L = 15pF; Figure 4			5	ns
t_{RCFM}	RxCLK 90-10% Fall Time	RxCLK t_{PER} = 31.25ns, C_L = 15pF; Figure 4			5	ns

Note 1: *Limits are guaranteed by 100% testing, sampling or correlation with worst case test conditions.*
Note 2: Current into all V_{CC} pins, V_{CC} = 5.25V, transmitting and receiving 16MHz data.
Note 3: Use a 2kΩ load at $\overline{FAULT}$ for these tests.
Note 4: 2.9k < RL1 < 5.5k, 2.9k < RL2 < 5.5k. RL1 connected between PHTMTX1 and PHTMRX1; RL2 connected between PHTMTX2 and PHTMRX2.
Note 5: Tested under the following conditions:
A. RL1 > 9.9k and 2.9k < RL2 < 5.5k, or RL2 > 9.9k and 2.9k < RL1 < 5.5k.
B. RL1 < 100Ω and 2.9k < RL2 < 5.5k, or RL2 < 100Ω and 2.9k < RL1 < 5.5k.
Note 6: A. Difference between the delay from the nearest TxCLK rising edge to the TxTPPN differential BR edge and the delay from the nearest TxCLK rising edge to the TxTPPN differential BR/2 edge. Measured for either rising output edges or falling output edges only, with measurements made for each. Measurements are to be made at the output of both test circuits shown in Figure 3. (See waveforms in Figure 7 –4 of draft ISO/IEC 8802-5q/D4).
B. Difference between the delay from the nearest TxCLK rising edge to the TxTPPN differential edge and the delay from the nearest TxCLK rising edge to the TxTPPN differential edge. Measured for either rising output edges or falling output edges only, with measurements made for each using random data (JKs, 0s, 1s). Measurements are to be made at the output of both test circuits shown in Figure 3. (See waveforms in Figure 7 –4 of draft ISO/IEC 8802-5q/D4).
Note 7: One-half the difference between the positive-going differential output pulsewidth and the negative-going differential output pulsewidth. Measured at the output of both test circuits in Figure 3 with a constant stream of all zeros or all ones. Measurements are to be averaged over 128 data pulses. Measured with input drive to TxD/TxCLK.
Note 8: Not tested in production. Guaranteed by characterization measurements.
Note 9: The transmitter TxTPP-TxTPN output waveform must also meet the waveform templates shown in section 7.2.2.2 of ISO/IEC 8802-5q.
Note 10: Disconnect the filter components at the FILT4MB or FILT16MB pins and apply the indicated voltage to that pin. Measure the output period at RxCLK. Disconnect RxTPPN from all input.
Note 11: See Figure 2 for timing. With the circuit in phase-lock, inject I1 = +5μA and measure the propagation delay t_{PD1} between an RxTPP rising edge and the corresponding RxCLK falling edge. Make a second delay measurement t_{PD2} while injecting I2 = –5μA. Phase detector gain is given by $K_d = (I2-I1)/(t_{PD1}-t_{PD2})$.
Note 12: The ML6682 is phase-locked to the RxTPP waveform with RxTPN biased to 2.5V (see Figure 5). Monitor RxD to observe correct data being latched. For one pulse, shorten the positive pulse at RxTPP by moving the rising edge, and check to see if the short pulse was latched. Continue to shorten the pulse in this manner until incorrect data appears at RxCLK. The time between the rising edge and the unshortened positive pulse midpoint is t_{RSTE}. Repeat this procedure for the other 3 cases shown in Figure 5.

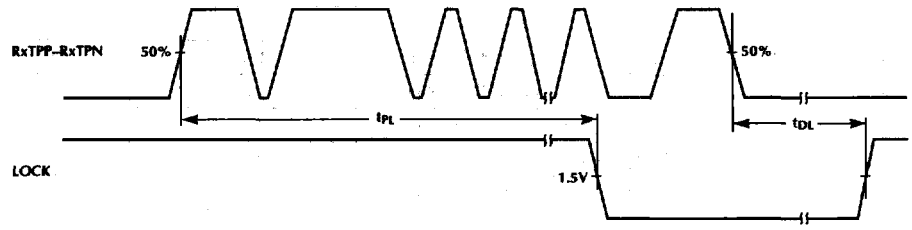


Figure 1. PLL Phase Lock Timing.

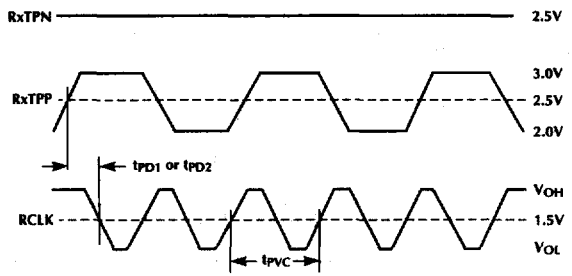


Figure 2. Phase Detector Gain Test.

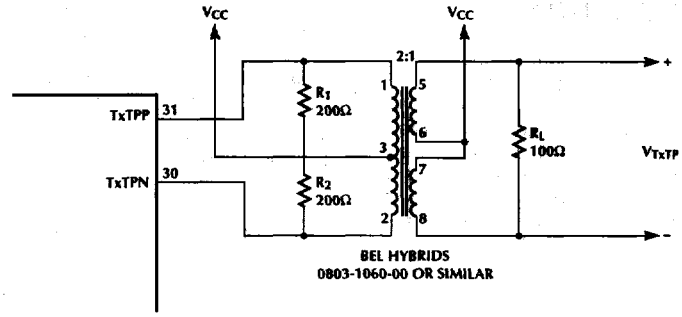


Figure 3A. Transmitter AC Test Circuit, 100Ω (UTP).

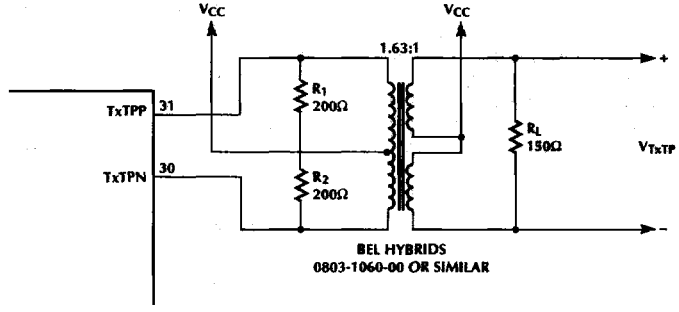


Figure 3B. Transmitter AC Test Circuit, 150Ω (STP).

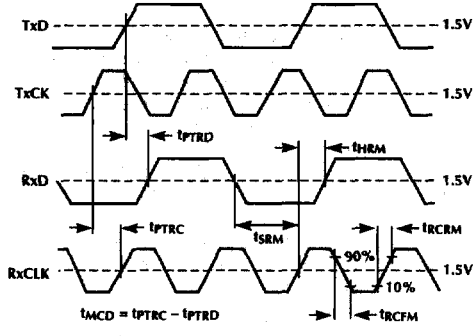


Figure 4. Receiver Timing.

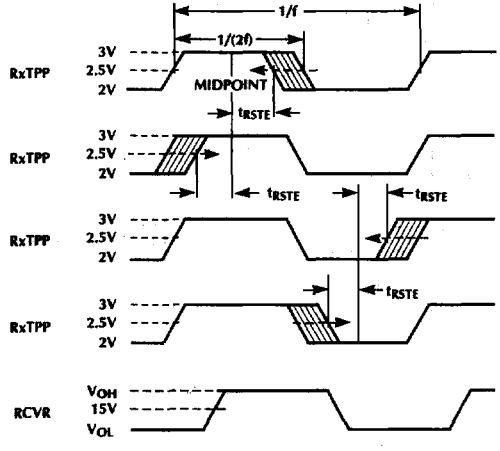


Figure 5. Receiver Static Timing Error Test.

FUNCTIONAL DESCRIPTION

Page 1 shows the functional block diagram of the ML6682. The device contains four major functional blocks; twisted pair line interface, port interface, PLL retiming circuit and crystal oscillator. In normal operation, the data is retransmitted from the previous port on to the transmit TP wire pair (to the station) by the use of TxD and TxCLK. The data from the station via the receive wire pair is retimed through the use of a dual PLL/FIFO. The retimed data at RxD is then clocked out to the next port by RxCLK.

PORT INTERFACE

The ML6682 can be used for implementing Lobe, Ring In and Ring Out ports in a concentrator. The device can be placed into either the INSERT state or the BYPASS state. Figure 6 is a functional illustration of the INSERT and BYPASS states.

When ML6682 is in the BYPASS state, the station is bypassed. The data input from the previous port is retimed and fed directly through to the next port (see figure 6). Signal from the receive twisted pair is retimed via the PLL and looped back to the transmit twisted pair. However, if the signal does not meet the receive frequency squelch criteria, the signal will not be fed to the PLL. The PLL will transmit the local clock signal onto the transmit twisted pair.

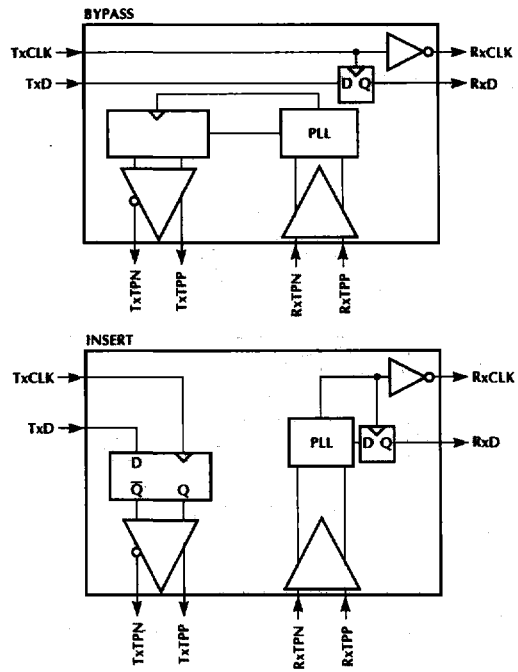


Figure 6. Bypass and Insert States.

When the port is INSERTed into the network, the transmit data TxD from the previous port is clocked by transmit clock TxCLK, and fed out on the twisted pair lines. The data from the receive twisted pair input is passed through the PLL and output on RxD and RxCLK pins.

Through various input pins, the ML6682 may be selected for one of three options:

1. Forced into the INSERT state
2. Forced into the BYPASS state
3. Allow the remote station to place the ML6682 into INSERT or BYPASS state with phantom control.

The logic equation to implement these options is as follows:

$$\overline{FBYP} \times (\overline{ALLOW} + \overline{FAULT}) = INSERT$$

When INSERT is a logic 1, the ML6682 is placed into the INSERT state as shown in Figure 6. When INSERT is a logic 0, the ML6682 is placed into the BYPASS state. Truth table 1 illustrates how the three above options can be achieved.

	$\overline{FBYP}$	$\overline{ALLOW}$	$\overline{FAULT}$	INSERT State
Forced Bypass Mode	0	X	X	0
Phantom Controlled Bypass	1	0	0	0
Phantom Controlled Insert	1	0	1	1
Forced Insert	1	1	X	1

X = Don't Care

Table 1. Logic for INSERT/BYPASS.

TP LINE INTERFACE

TP Line Receiver consists of a line equalizer, receive squelch circuit and a resistive attenuator.

RECEIVE EQUALIZER

This receive equalizer compensates for twisted-pair cable dispersion, which otherwise would give rise to inter-symbol interference (ISI). The amount of equalization varies with the average amplitude of the received signal. The received signal amplitude gives a rough value for the length of the attached cable. The filter/equalizer characteristic is the inverse of the cable's dispersion characteristic. Both UTP and STP cables approximate a low-pass filter, so the filter/equalizer approximates an inverse root equalizer. There are two sets of equalizers, one for 4 Mbps operation and one for 16 Mbps operation. This is switched automatically when the $4/\overline{16}$ pin is toggled. Each equalizer has its own external components which consist of two resistors and a capacitor.

RECEIVE SQUELCH CIRCUIT

The TP line receiver consists of a resistive attenuator with common-mode bias set circuit.

The receive squelch circuit qualifies the incoming signal to determine whether the signal contains valid data. The circuit qualifies the signal on the basis of the pulse width of the signal. This prevents the PLL from trying to lock onto the wrong frequency when using 4 or 16 Mbps data rates. Once the signal has been qualified, the circuit will then unsquelch. The 4/$\overline{16}$ pin selects one of two frequency squelch criteria.

Pulse Width and Frequency Squelch Criteria

4 Mbps max limit	4.5MHz to 6.5MHz
4 Mbps max pulse width limit	396ns to 480ns
16 Mbps max limit	18MHz to 26MHz
16 Mbps max pulse width limit	99ns to 120ns

When squelch is on, the PLL is tracking the internal clock frequency coming from an external clock or the internal oscillator. When the part unsquelches the PLL switches into phase acquisition mode, attempting to phase lock onto the incoming data.

PHASE LOCK LOOP

The PLLs are third-order, type II charge pump loops (see F.M. Gardner, "Charge-Pump Phase-Lock Loops", IEEE Trans Comm, Vol. COM-28, No. 11, pp. 1849-1858, November 1980). They have high damping factor and low loop bandwidth to minimize accumulated jitter. The loop filter is externally connected. The third pole is at a very high frequency, since the ratio of the second and third order pole capacitors C1/C3 is about 20,000:1. This, too, is done to minimize accumulated jitter.

The 16 Mbps loop filter, slave loop filter, and 4 Mbps loop filter are external to the chip. Each filter consists of two capacitors and a resistor. The switching between the 16Mbps and 4Mbps loop filters is automatic when the 4/$\overline{16}$ pin is toggled. Each data rate uses a different charge pump.

The VCO uses a MOS voltage-to-current converter at its input to give a very high input impedance and low static phase error. The high VCO input impedance also allows the elimination of a loop filter buffer and the parasitic poles a buffer would add to the loop. The oscillator itself is a bipolar ring type oscillator with temperature and voltage-compensated output frequency for low jitter.

The first PLL will achieve lock after several microseconds of a static phase error of less than ± 4 nsec. Hysteresis is built into the lock circuit so that it is more difficult to achieve lock than it is to lose lock. This will also prevent any oscillation of the $\overline{LOCK}$ pin. Lock will be lost if the phase error exceeds ±4 nsec for several micro-seconds. Once lock is lost, the PLL will try to achieve phase lock for several milli-seconds. If it is unsuccessful, the ML6682 will switch to internal frequency acquisition mode and re-center the VCO. Once it has achieved frequency lock with its internal oscillator, it will automatically switch to phase acquisition mode and try again to phase lock onto the data.

The frequency squelch circuit will limit the frequency range allowed to pass into the PLL. This limited frequency range in addition to the stringent lock criteria will insure that the PLL will not lock onto harmonics or sidebands of the fundamental data rate.

The first PLL clocks the data into an 8 UI FIFO. Each flip-flop in the FIFO stores one UI which is one half bit. The second (slave) PLL has a much narrower bandwidth set by the external filter connected to pin FILTPLL2. The second PLL is fed the first PLL's clock so that it can remove more of the jitter. The clock out of the second PLL is used to clock the data out of the FIFO and onto the RxD pin. The second PLL's clock output appears at RxCLK. This dual PLL architecture is the most effective way to reduce jitter and insure optimal performance from a token ring network.

TP LINE DRIVER

The TP OUTPUT driver uses a current mode switch which develops the output voltage by driving current through the terminating resistor and the output filter. Both TxTPP and TxTPN outputs are open collector, intended to drive a center-tapped transformer, with the center tap connected to V_{CC}. The driver is capable of driving 150Ω doubly-terminated transmission lines to a minimum 4.1V_{P-P} level or 100Ω doubly-terminated transmission lines to a minimum 2.7V_{P-P} level. The driver's output is waveshaped, allowing the use of a simple external transmit filter.

PHANTOM CURRENT DETECTION

The ML6682 provides a phantom current detection function. With PHTMD/$\overline{S}$ driven high, the phantom voltage and wire fault detection circuit provides correct phantom DC output voltage under normal conditions. It also senses short-circuit and open-circuit fault conditions, and removes phantom voltage when appropriate.

In the LOBE port application with PHTMD/$\overline{S}$ tied low ($\overline{FBYP}$ is tied high and $\overline{ALLOW}$ is tied low), driving PHTMRX1 high places the device into the INSERT mode. Driving PHTMRX1 low places the device in the BYPASS mode, in which data from the previous port will be passed on to the next port.

CLOCK OSCILLATOR

The ML6682 provides an on-chip clock oscillator by connecting a crystal to the XTAL1 pin. The ML6682 can also be driven by an external 16MHz clock at the XTAL1 pin, or by an external 32MHz clock at the XTAL2 pin. In either case, the unused XTAL pin should be grounded.

APPLICATIONS

Figure 7 shows a block diagram of an intelligent UTP Hub implementation with active retiming on each port. The architecture shown has a back up ring for fault tolerant operation. The Ring In and Ring Out ports use phantom current to detect wire faults. When a fault is detected, the Ring-In and Ring-Out port go into the bypass state and perform an automatic loopback onto the Back-up Ring. This feature is especially useful in stackable hub designs.

A micro processor can be used to manage each individual port. All the ports including the Ring In and Ring Out ports can be individually programmed into "Force INSERT", "Force BYPASS" or "Allow phantom control".

LOBE PORT

Figure 8 shows a typical implementation of a lobe port. Lobe ports are configured as phantom sense ports using opto isolators for sensing phantom current. Phantom current is sensed with an opto isolated output signal fed into pin PHTMRX1. PHTMTX1 will go low with an open collector output when the ML6682 goes into the INSERT state. PHTMTX1 may either be used to drive an LED indicator or another opto isolator to signal the remote station whether it is inserted or not.

By connecting the signal from the $\overline{LOCK}$ pin to the $\overline{FBYP}$ pin, the ML6682 is forced into bypass mode until the PLL achieves lock. When a station with a frequency different than the ring frequency attempts to insert into the ring, the PLL will not achieve lock and thus the station will not be inserted.

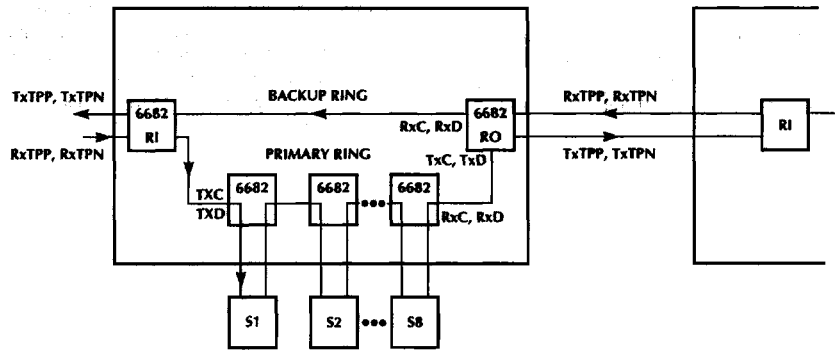


Figure 7. Intelligent UTP Hub.

RING-OUT PORT

The Ring-Out port may also be configured for phantom sense with automatic loopback fault detection. When Phantom current is detected the part is in the INSERT state. If phantom current is lost, the ML6682 will automatically switch to the BYPASS state. Using the $\overline{FBYP}$ and $\overline{ALLOW}$ pins the part can also be forced into INSERT state, for compatibility with older standard type hubs, or forced into BYPASS for diagnostic purposes.

The configuration of a fault tolerant Ring-Out port is implemented exactly like a lobe port. The TxD and TxCLK pins are connected to the RxD and the RxCLK pins of the ring out port to create a "back up" ring. When the fault tolerant feature is not needed for compatibility with the older hubs, the phantom current sense capability of the ML6682 should be disabled and the device should be placed in the forced insert state by using $\overline{FBYP}$ and $\overline{ALLOW}$. The $\overline{LOCK}$ pin should still be used to ensure that the proper ring speed is maintained.

RING-IN PORT

Tie the PHTMD/$\overline{S}$ pin high to configure the ML6682 as a Ring-In port. In this mode the Ring-In port looks like a station; however, when a FAULT is detected on the transmit or receive twisted pair wires, the ML6682 will automatically go into BYPASS state. The PHTMRX1 and PHTMRX2 pins drive the receive pair transformer center taps, and the PHTMX1 and PHTMTX2 pins drive the transmit pair transformer center taps on the cable side of the transformers in this mode.

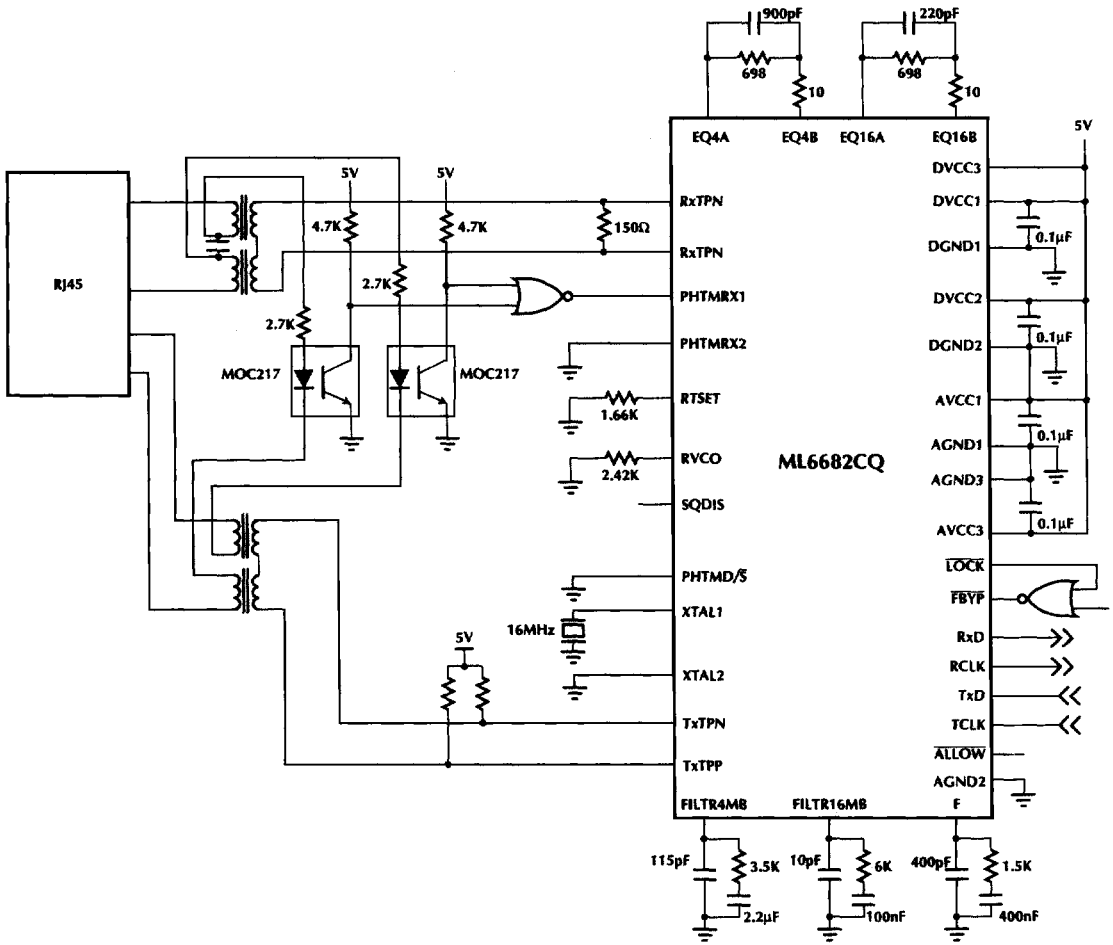


Figure 8. Typical Circuit for a Lobe Port.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML6682CQ	0°C to 70°C	44-Pin PLCC (Q44)
ML6682CH	0°C to 70°C	44-Pin TQFP (H44)