# M5M4V16409ATP-8,-10,-12,-15

Oct 26,1992

**16MCDRAM:16M (4194304 - WORD BY 4 - BIT) Cache DRAM with 16k (4096-WORD BY4 -BIT) SRAM**

*Preliminary*
**This document is a preliminary Target Spec. and some of the contents are subject to change without notice.**

## DESCRIPTION

1. The M5M4V16409TP is a 16M-bit Cache DRAM which integrates input registers, a 4,194,304-word by 4-bit dynamic memory array and a 4096-word by 4-bit static RAM array as a Cache memory (block size 16x4) onto a single monolithic circuit. The block data transfer between the DRAM and the data transfer buffer(DTBx) is performed in one instruction cycle, a fundamental advantage over a conventional DRAM/ SRAM cache.
2. The RAM is fabricated with a high performance CMOS process, and is ideal for large-capacity memory systems where high speed, low power dissipation, and low cost are essential. The use of quadruple-layer polysilicon process combined with silicide and double layer aluminum wiring technology, a single-transistor dynamic storage stacked capacitor cell, and a six-transistor static storage cache cell provide high circuit density at reduced costs.

## PIN CONFIGURATION (TOP VIEW)

400mil TSOP Type II, 0.65mm lead pitch

| | | | |
|---|---|---|---|
| Vcc | 1 | 62 | Vss |
| NC | 2 | 61 | Ad11 |
| NC | 3 | 60 | Ad10 |
| DQC | 4 | 59 | Ad9 |
| CC1# | 5 | 58 | Ad8 |
| CC0# | 6 | 57 | Ad7 |
| WE# | 7 | 56 | As11 |
| CS# | 8 | 55 | As10 |
| CMd# | 9 | 54 | As9 |
| CMs# | 10 | 53 | As8 |
| K | 11 | 52 | NC |
| VssQ | 12 | 51 | VssQ |
| M0/D0 | 13 | 50 | M3/D3 |
| DQ0/Q0 | 14 | 49 | VccQ |
| VccQ | 15 | 48 | Vss |
| Vcc | 16 | 47 | VccQ |
| VccQ | 17 | 46 | DQ2/Q2 |
| DQ1/Q1 | 18 | 45 | M2/D2 |
| M1/D1 | 19 | 44 | VssQ |
| VssQ | 20 | 43 | G# |
| As0 | 21 | 42 | As7 |
| As1 | 22 | 41 | As6 |
| As2 | 23 | 40 | As5 |
| As3 | 24 | 39 | As4 |
| RAS# | 25 | 38 | As3 |
| CAS# | 26 | 37 | Ad6 |
| DTD# | 27 | 36 | Ad5 |
| Ad0 | 28 | 35 | Ad4 |
| Ad1 | 29 | 34 | Ad3 |
| Ad2 | 30 | 33 | NC |
| Vcc | 31 | 32 | Vss |

**K** : **Master Clock**
**CS#** : **Chip Select**
**CMd#** : **DRAM Clock Mask**
**RAS#** : **Row Addr. Strobe**
**CAS#** : **Column Addr. Strobe**
**DTD#** : **Data Transfer Direction**
**Ad** : **DRAM Address**
**CMs#** : **SRAM Clock Mask**
**CC0#,CC1#**: **Control Clocks**
**WE#** : **SRAM Write Enable**
**DQC** : **I/O Byte Control**
**As** : **SRAM Address**
**G#** : **Output Enable**
**DQ** : **Data I/O**
**D** : **Data Input**
**Q** : **Data Output**
**M** : **Mask Enable**
**Vcc** : **Power Supply**
**Vss** : **Ground**

## FEATURES

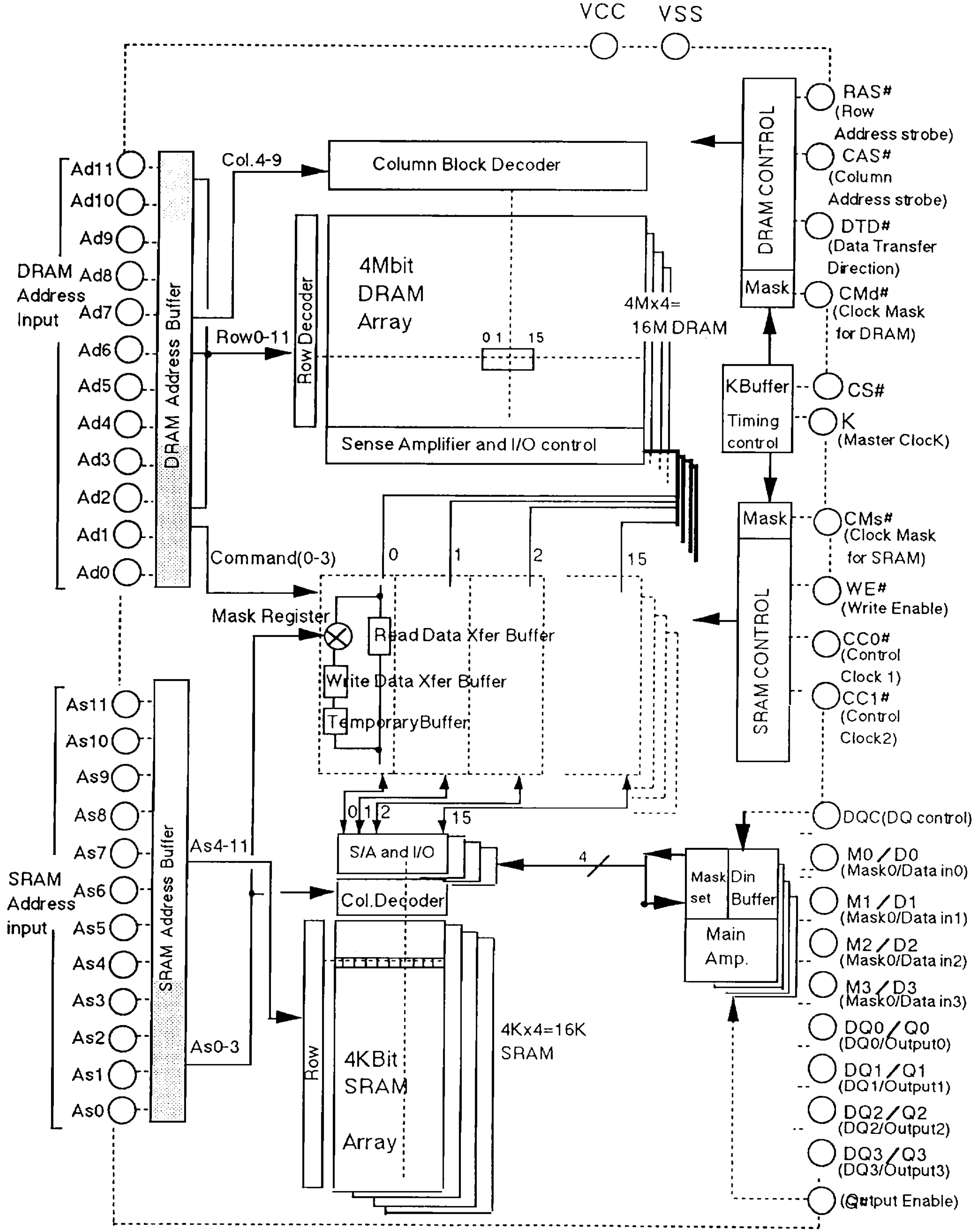
| Type name | SRAM Access/cycle | Fast Copy Back Access/cycle | Direct Array Access/cycle | Power Dissipation |
|---|---|---|---|---|
| M5M4V16409TP-8 | 8ns/8ns | 64ns/(208ns)* | 64ns/104ns | DRAM:TBD SRAM:TBD |
| M5M4V16409TP-10 | 10ns/10ns | 64ns/(208ns)* | 64ns/104ns | DRAM:TBD SRAM:TBD |
| M5M4V16409TP-12 | 12ns/12ns | 66ns/(216ns)* | 66ns/108ns | DRAM:TBD SRAM:TBD |
| M5M4V16409TP-15 | 15ns/15ns | 69ns/(228ns)* | 69ns/114ns | DRAM:TBD SRAM:TBD |

*** : Write back cycle after the miss write/read access can be hidden in the next hit cycle. (Fast copy back scheme)**

- 62-pin,400-mil TSOP (type II) with 0.65mm lead pitch and 20.95mm package length.
- Multiplexed DRAM address inputs for reduced pin count and higher system densities.
- Selectable output operation (transparent / latched / registered) and I/O configuration (separate D/Q / Masked Write) using command registers.
- Single 3.3V +/- 0.3V Power Supply.
- 4096 refresh cycles every 64ms (Ad0->Ad11).
- Synchronous design for precise control with an external clock (K).
- Suspended input/output by advanced mask clock (CMs#).
- All inputs/outputs low capacitance and LVTTL compatible.
- Asynchronous output enable (G#) for bus control.
- Separate DRAM and SRAM address inputs for fast SRAM access.
- Page Mode.
- Auto Refresh.

*MITSS004*

# BLOCK DIAGRAM



# FUNCTION TRUTH TABLE

| Mnemonic CODE | | SRAM | | | | | As(SRAM address) | DRAM | | | | Ad (DRAM address) | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | CS# | Previous CMs# | CC0# | CC1# | WE# | DQC | As0-11 | Previous CMd# | RAS# | CAS# | DTD# | Ad0-11 | Ad2 | Ad1 | Ad0 |
| NOP | H | X | X | X | X | X | X | X | X | X | X | X | | | |
| SPD | X | L | X | X | X | X | X | X | X | X | X | X | | | |
| DES | L | H | H | H | X | X | X | X | X | X | X | X | | | |
| SR | L | H | H | L | H | "H | As0-9 | X | X | X | X | X | | | |
| SW | L | H | H | L | L | "H | As0-9 | X | X | X | X | X | | | |
| BRT | L | H | L | H | H | L | @As3-7 | X | X | X | X | X | | | |
| BWT | L | H | L | H | L | L | @As3-7 | X | X | X | X | X | | | |
| BRTR | L | H | L | H | H | H | As0-9 | X | X | X | X | X | | | |
| BWTW | L | H | L | H | L | H | As0-9 | X | X | X | X | X | | | |
| BR | L | H | L | L | H | "H | @As0-2 | X | X | X | X | X | | | |
| BW | L | H | L | L | L | "H | @As0-2 | X | X | X | X | X | | | |
| DPD | X | X | X | X | X | X | X | L | X | X | X | X | | | |
| DNOP | L | X | X | X | X | X | X | H | H | H | X | X | | | |
| DRT | L | X | X | X | X | X | X | H | H | L | H | @Ad3-7 (Col.Block) | 0 | 0 | 0 |
| DWT1 | L | X | X | X | X | X | X | H | H | L | L | @Ad3-7 (Col.Block) | 0 | 0 | 0 |
| DWT1R | L | X | X | X | X | X | X | H | H | L | L | @Ad3-7 (Col.Block) | 0 | 0 | 1 |
| DWT2 | L | X | X | X | X | X | X | H | H | L | L | @Ad3-7 (Col.Block) | 0 | 1 | 0 |
| DWT2R | L | X | X | X | X | X | X | H | H | L | L | @Ad3-7 (Col.Block) | 0 | 1 | 1 |
| ACT | L | X | X | X | X | X | X | H | L | H | H | Ad0-9 (Row Add.) | | | |
| PCG | L | X | X | X | X | X | X | H | L | H | L | X | | | |
| ARF | L | X | X | X | X | X | X | H | L | L | H | X | | | |
| SCR | L | X | X | X | X | X | X | H | L | L | L | Command | | | |

"H; If DQC is L , data inputs and main amps. do not work. SR,SW,BR and BW cycles with DQC of low result in Deselect SRAM.

@; The unused addresses must be set to Low

| Data Transfer Buffer | | | | | DQ pin | | | Function | |
|---|---|---|---|---|---|---|---|---|---|
| DTBW | | Xfer Mask | | DTBR | | | | | |
| Tempo-rary | DTBW | Tempo-rary | Xfer Mask | | Write Mask | Din | Dout | | |
| – | – | – | – | – | – | – | Hi-Z | No Operation | |
| – | – | – | – | – | – | – | Suspend | SRAM Power Down& Data suspend | |
| – | – | – | – | – | – | – | Hi-Z | Deselect SRAM | |
| – | – | – | – | – | – | – | Valid | SRAM Read | SRAM->DO |
| – | – | – | – | – | Load /Use | Valid | Hi-Z | SRAM Write | DIN->SRAM |
| – | – | – | – | Use | – | – | Hi-Z | Buffer Read Xfer | DTBR->SRAM |
| Load | – | Reset All mask | – | – | Load /Use | – | Hi-Z | Buffer Write Xfer | SRAM->DTBW |
| – | – | – | – | Use | – | – | Valid | Buffer Read Xfer & Read | DTBR->SRAM ->DO |
| Load | – | Reset All mask | – | – | Load /Use | Valid | Hi-Z | Buffer Write Xfer & Write | DIN->SRAM ->DTBW |
| – | – | – | – | Use | – | – | Valid | Buffer Read | DTBR->DO |
| Load | – | ***Reset 1 bit | – | – | Load /Use | Valid | Hi-Z | Buffer Write | DIN->DTBW |
| – | – | – | – | – | – | – | – | DRAM Power Down | |
| – | – | – | – | – | – | – | – | DRAM No Operation | |
| – | – | – | – | Load | – | – | – | DRAM Read Xfer | DRAM->DTBR |
| – | **Load /Use | *Set All | **Load /Use | – | – | – | – | DRAM Write Xfer1 | DTBW->DRAM |
| – | **Load /Use | *Set All | **Load /Use | Load | – | – | – | DRAM Write Xfer1 & Read | DTBW->DRAM ->DTBR |
| – | Use | – | Use | – | – | – | – | DRAM Write Xfer2 | DTBW->DRAM |
| – | Use | – | Use | Load | – | – | – | DRAM Write Xfer2 & Read | DTBW->DRAM ->DTBR |
| – | – | – | – | – | – | – | – | DRAM Activate | |
| – | – | – | – | – | – | – | – | DRAM Precharge | |
| – | – | – | – | – | – | – | – | Auto Refresh | |
| – | – | – | – | – | – | – | – | Set Command Register | |

**Load/Use; If BW or BWT or BWTW happens at the first K cycle of DWT1 or DWT1R, data is loaded and transferred to DRAM.

***Reset 1 bit; Reset 1 Xfer mask bit of 16 word accumulatively.

* Set All; BW and BWT and BWTW cycle can reset all or each bit just after mask set all

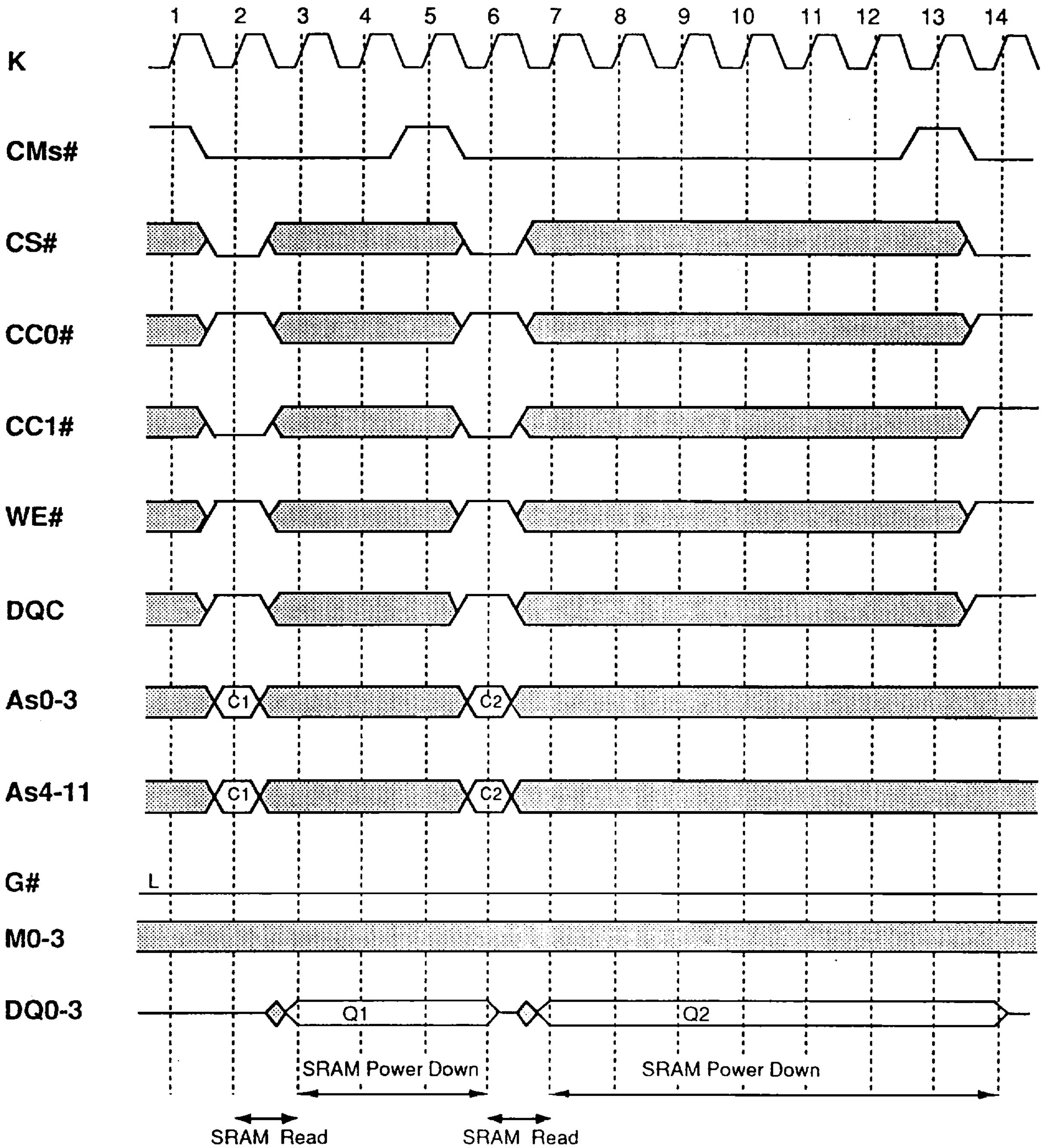
# PIN DESCRIPTIONS

| | | |
|---|---|---|
| K | Input | *Master Clock* Provides the fundamental timing and the internal clock frequency for the CDRAM. All external timing parameters (with the exception of G#) are specified with respect to either the rising or falling edge of K. |
| CMd# | Input | *DRAM Clock Mask* controls the operation of the internal DRAM master clock (K). When CMd# is asserted at the rising edge of K, the internal DRAM master clock (K) for the following cycle is suspended, resulting in the power down of the DRAM portion of the circuit. |
| RAS# | Input | *Row Address Strobe* is used in conjunction with Master clock K (depending on the states of CMd#, CAS#, and DTD#) to activate the DRAM (latching the Row Address lines and accessing 1 of 1024 rows), initiate a DRAM precharge cycle, perform a DRAM Read or Write Transfer, DRAM Write transfer & Read, set the Command registers, start an Auto-Refresh cycle, create a DRAM NOP cycle, or power down the DRAM. |
| CAS# | Input | *Column Address Strobe* is used in conjunction with the Master Clock K to latch the Column address lines. When preceded by RAS# in a DRAM access cycle, CAS# initiates a DRAM Write Transfer (DTBW -> DRAM, if DTD#=L), DRAM Write Transfer & Read (DTBW -> DRAM -> DTBR, if DTD#=L) or DRAM Read Transfer (DRAM -> DTBR, if DTD#=H), depending on the state of DTD# (see DTD# pin description). |
| DTD# | Input | *Data Transfer Direction* controls DRAM-to-DTBR/DTBW Read/Write direction. If preceded by a RAS# low cycle, both CAS# and DTD# low (on the rising edge of K) initiate a DRAM Write Transfer cycle (DTBW -> DRAM) and DRAM Write Transfer & Read(DTBW -> DRAM -> DTBR). If DTD# stays high with the above conditions, a DRAM -> DTBR cycle results.<br>Also, when DTD# going low is synchronized with RAS# going low, the DRAM goes into a precharge mode, locking out any DRAM access operations until the precharge cycle is complete. |
| Ad0-Ad11 | Inputs | *DRAM Address Lines* are Multiplexed to reduce pin count. Ad0-Ad11 (@ RAS=Low, K=Rising edge) specify the Row Address of the DRAM and Ad4-Ad9 (@ CAS=Low, K=Rising edge) specify the Block Address of the DRAM. In addition, Ad0-Ad11(@RAS=Low, K=Rising Edge) specify the refresh address (which is carried out in 4096 refresh cycles within 64ms). |

| | | |
|---|---|---|
| CS# | Input | The *Chip Select* controls the operation of the CDRAM. When CS#=H at the rising edge of K, the chip is in No Operation mode. |
| CMs# | Input | *SRAM Clock Mask* controls the operation of the internal SRAM master clock (Ks). When CMs is asserted at a rising edge of K, the internal SRAM master clock for the following cycle is suspended, resulting in the power down of the SRAM portion of the circuit, including the Sense Amps. CMs# can also be used to retain output data during SRAM power-down. |
| DQC | Inputs | DQC is a *I/O Byte control signal.* If G#=Low, DQC has a control of output impedance, and common I/O Read/Write is possible. |
| WE# | Input | *Write Enable* controls SRAM and DTBR/DTBW read and write operations. A high on the WE# pin causes either a Buffer Read, SRAM Read, Buffer Read Transfer and/or a Buffer Read transfer & Read to occur (depending on the state of the CC0# and CC1# bits). A low on the WE# pin causes either a Buffer Write, SRAM Write, Buffer Write Transfer and/or a Buffer Write Transfer & Write to occur (depending on the state of the CC0# and CC1# inputs) |
| CC0#,CC1# | Inputs | The *Control Clock Inputs* allow SRAM and Buffer access control. CC0# and CC1# determine what mode the device is in:<br>CC0#=CC1#=Low : Buffer Read/Write (WE#=H/L)<br>CC0#=L, CC1#=H : Buffer Read/Write Transfer, Buffer Read Transfer&Read and Buffer Write Transfer & Write(WE#=H/L,DQC=H/L)<br>CC0#=H, CC1#=L : SRAM Read/Write (WE#=H/L)<br>CC0#=CC1#=High : Deselect SRAM (CS#=L,previous CMs#=H) |
| As0-As9 | Inputs | *SRAM Address Lines* are non-multiplexed, and access 4096 - 4-bit words ( configured as 256 Rows X 16 Columns X 4 Bits, where the Block Size is 16 X 4) in the SRAM cache. As0-As3 Select Block Address, and As4-As11 select the SRAM row. |
| G# | Input | The *Output Enable* is the only asynchronous input. G#=high makes the outputs high impedance. |
| DQ0-DQ3 | Inputs / Outputs | These are the *Data Lines* for the CDRAM and are asynchronously controlled by G#. Output operation is either transparent, latched, or registered depending on the state of the command register. |

| | | |
|---|---|---|
| Q0-Q3 | Outputs | These are *Data Output lines* for the CDRAM when the separate D/Q option is selected (by command register). Output operation is either transparent, latched, or registered, depending on the state of the command register. |
| D0-D3 | Inputs | These are the *Data Input lines* for the CDRAM when the separate D/Q option is selected (by command register). When in a Write Buffer or Write SRAM mode, the data on the D pins are latched in at the rising edge of K. |
| M0-M3 | Inputs | The *Mask Enable* pins are enabled when the common D/Q option is selected (by command register). The corresponding DQ bits (e.g. M0 -> DQ0) are masked or not masked depending on the state of M0-M3 (Low=masked) at the rising edge of K for a SRAM Write or Buffer Write cycle. |

## SRAM Power-down

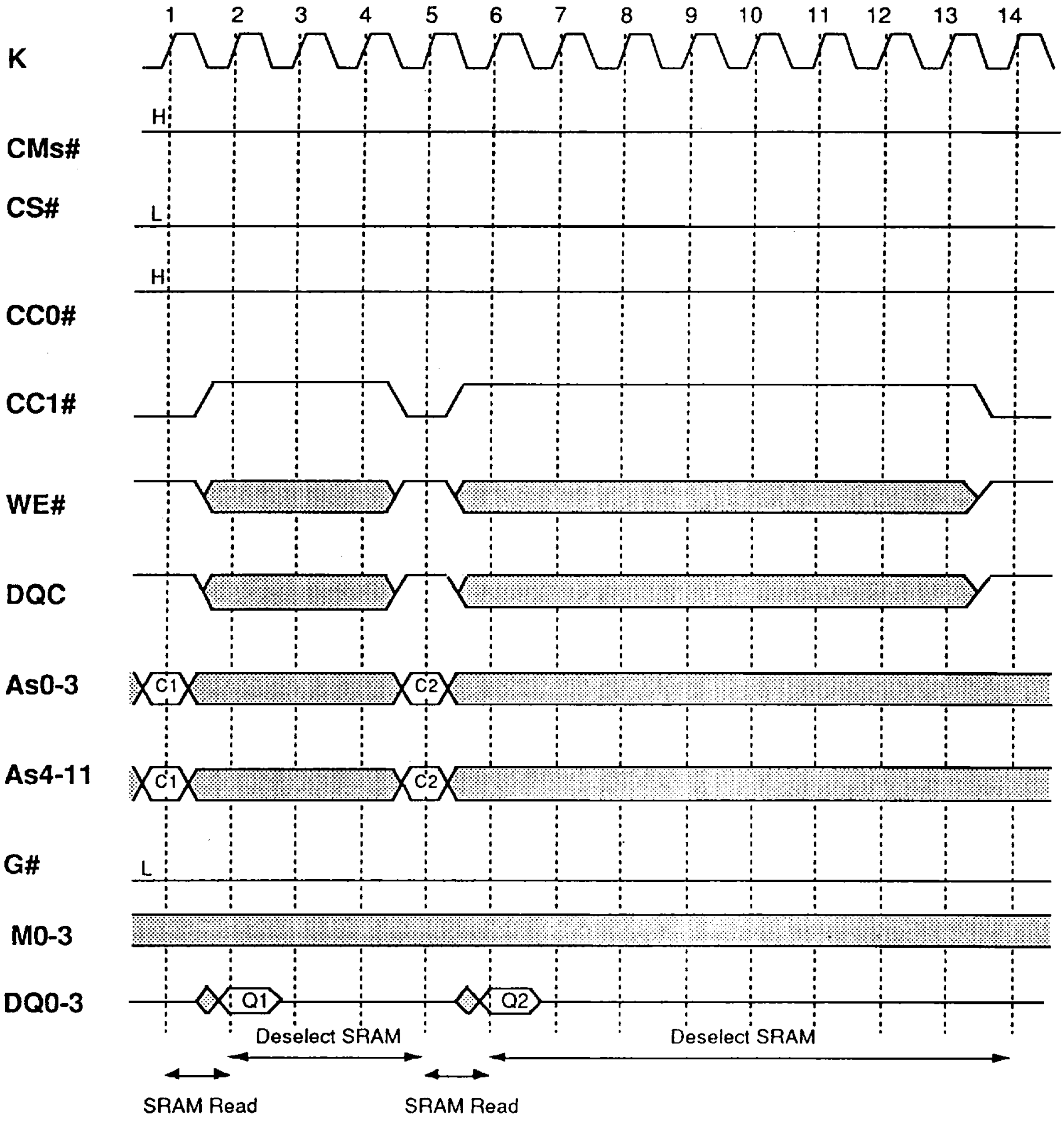



Note : Output is transparent.

## SRAM Power Down

| | |
|---|---|
| **SRAM Power Down** | **If CMs#=Low at the rising edge of K, the SRAM goes into Power-down mode at the next rising edge of K. During this mode, the internal SRAM K clock becomes inactive, and the SRAM Sense Amps are powered down. The Output Buffers remain powered-up, enabling outputs to be driven after SRAM is powered-down.** |
| SRAM Read | If CMs#=Low at the rising edge of K and CS#=CC1#= Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data. |

## Deselect SRAM




Note : Output is transparent.

# Deselect SRAM

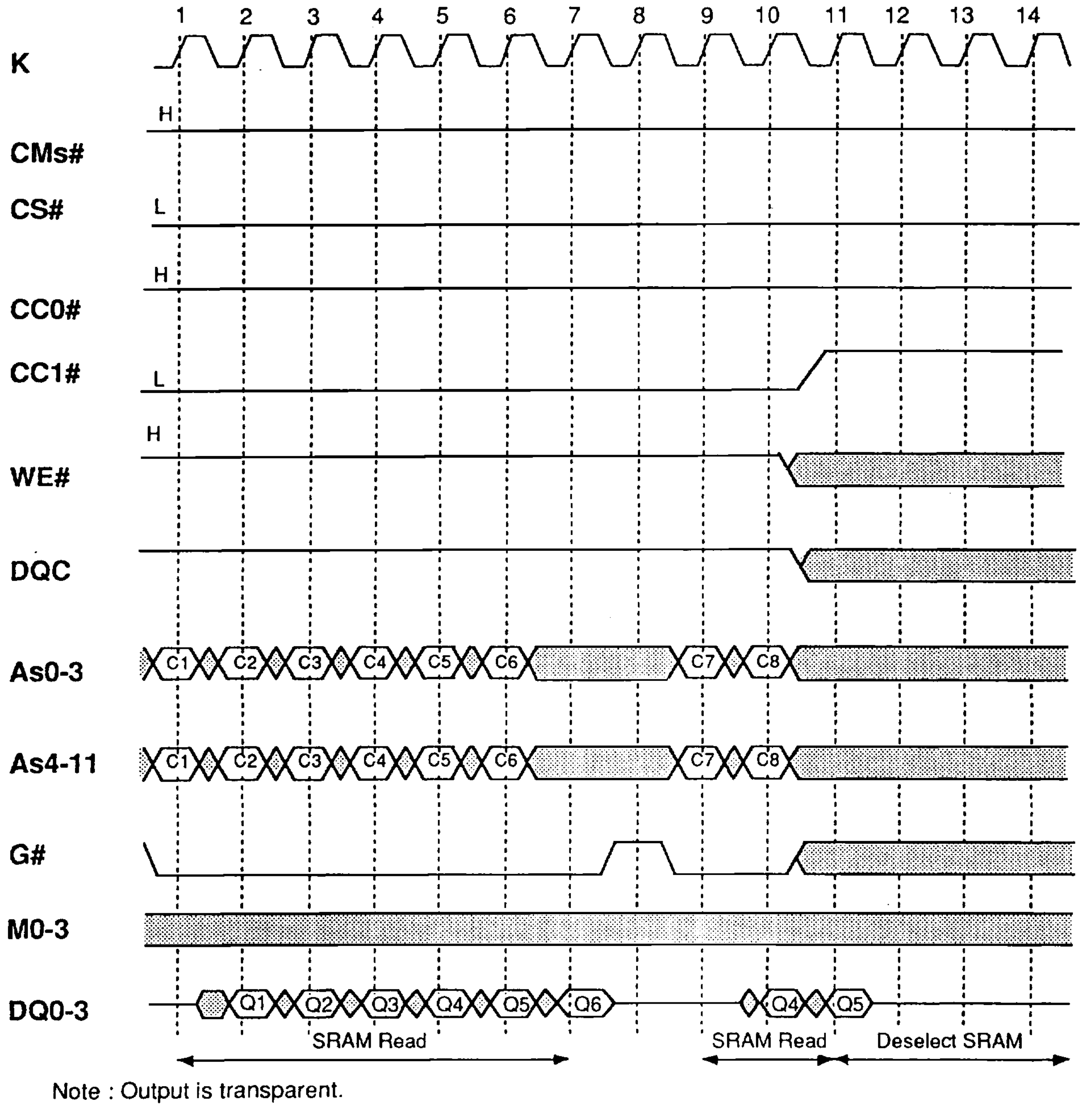
SRAM Read

If CMs#=Low at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.

**Deselect SRAM**

**If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.**

## SRAM Read




Note : Output is transparent.

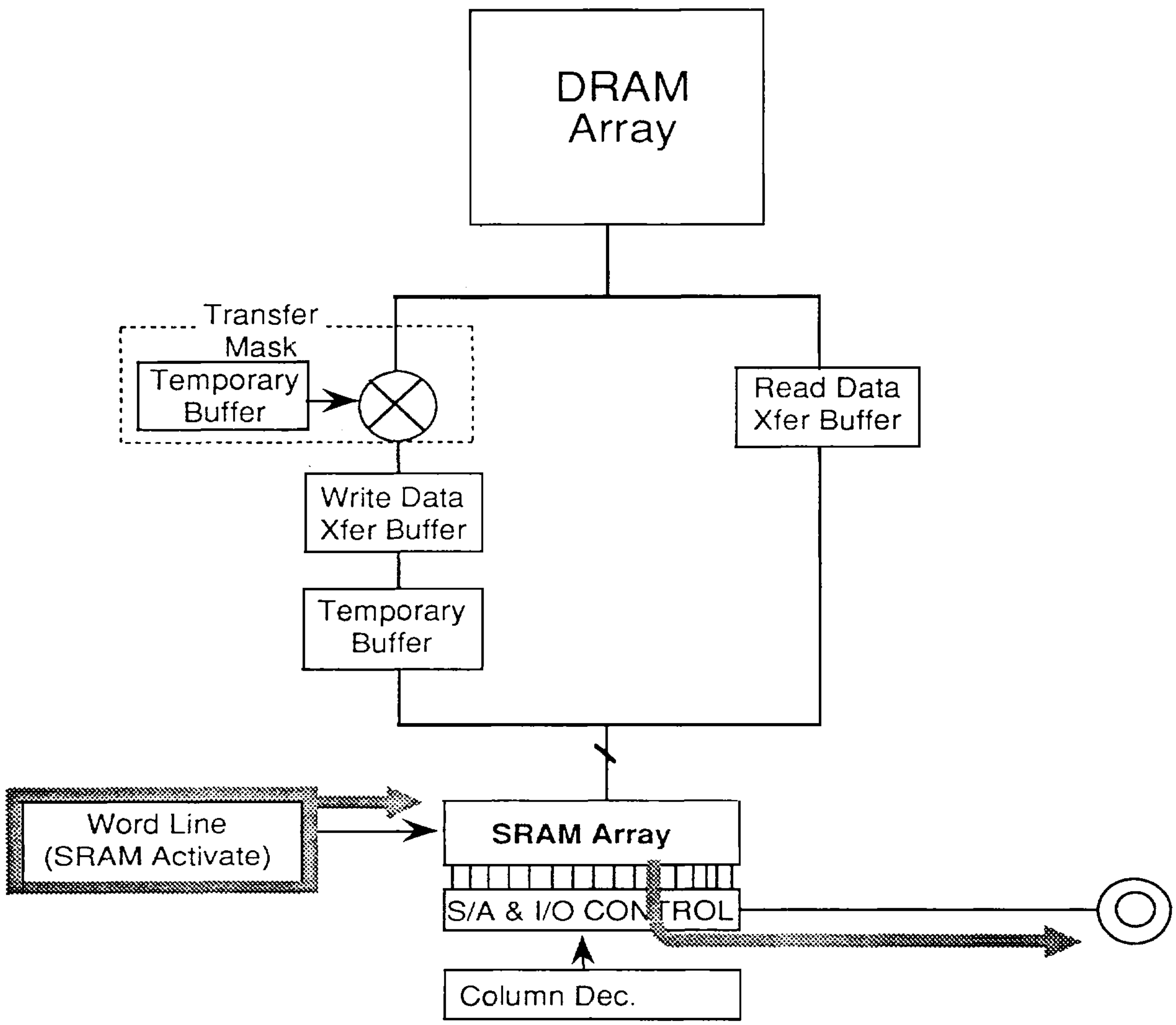
## SRAM Read

Deselect SRAM

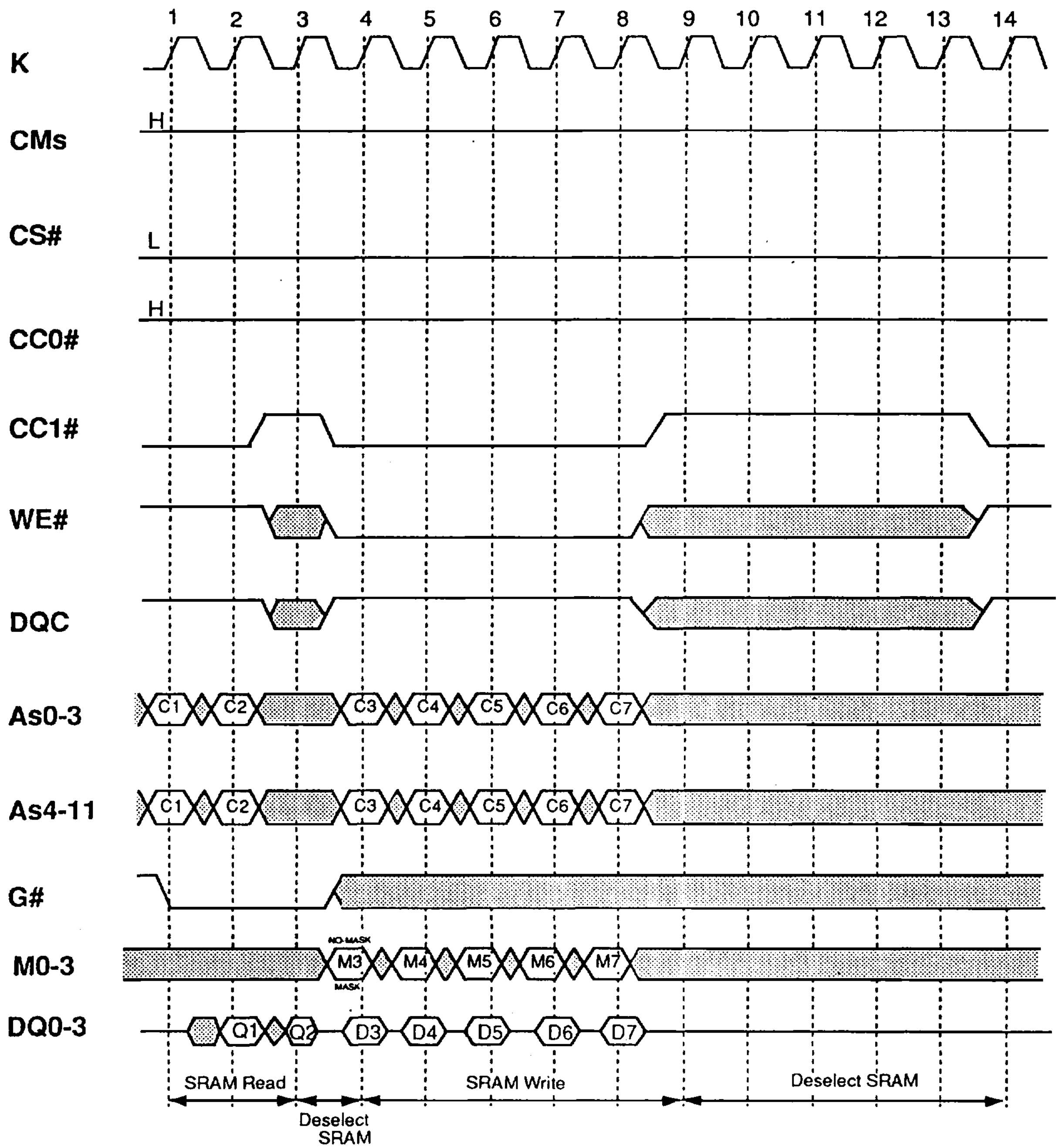
If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.

**SRAM Read**

**If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.**



## SRAM Write




Note : Output is transparent.

# SRAM Write

SRAM Read

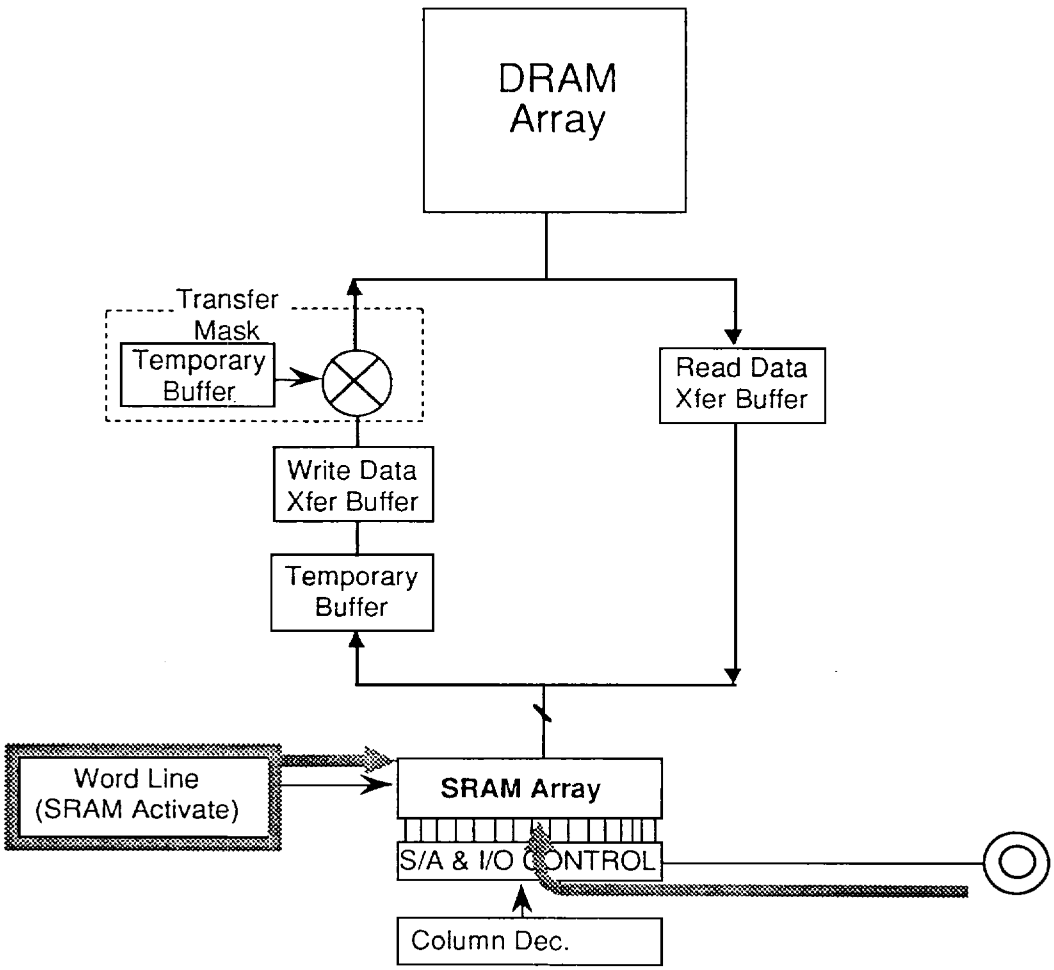
If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.

Deselect SRAM

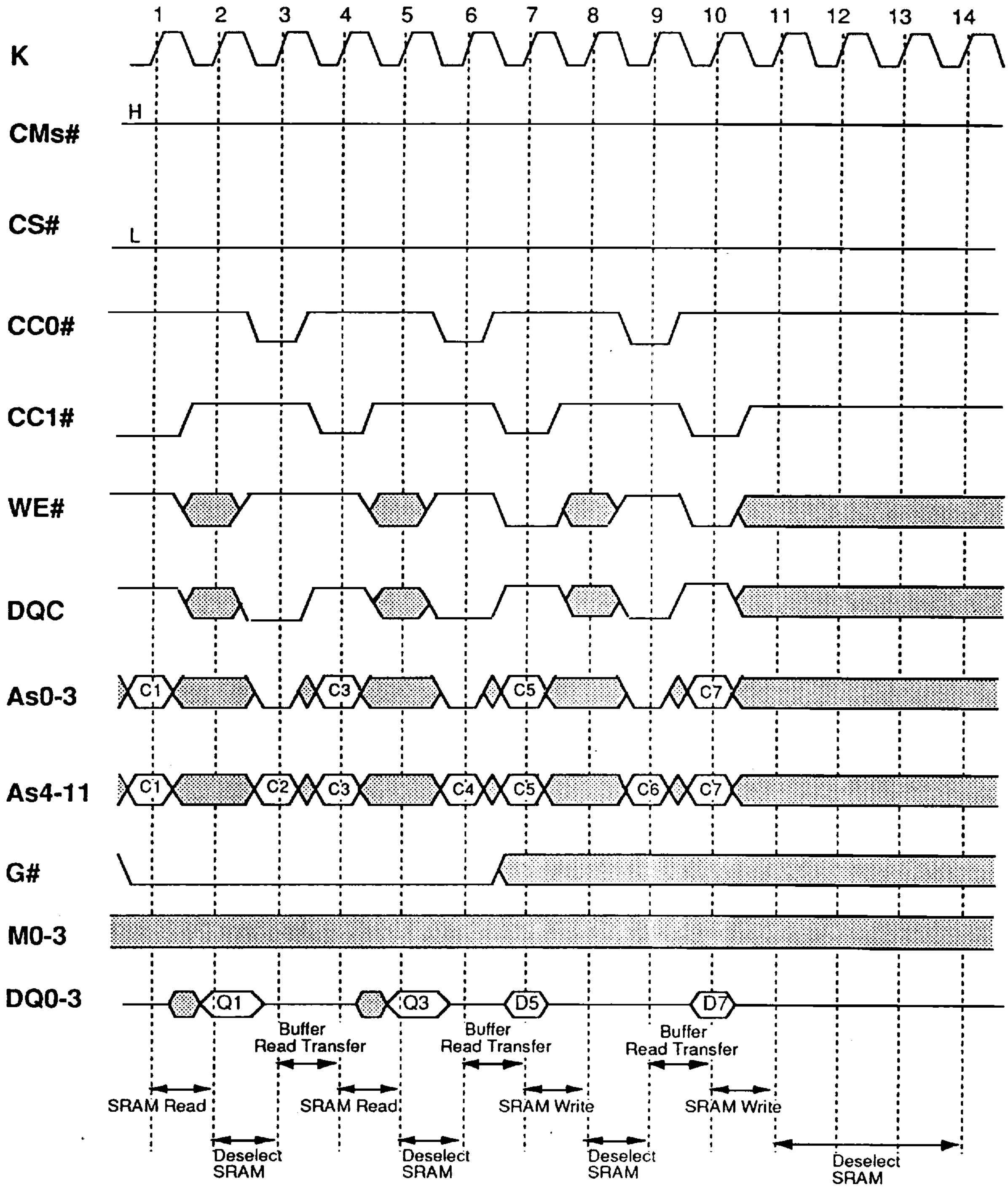
If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.

**SRAM Write**

**If CMs#=High at the rising edge of K and CC0#=DQC=High and CS#=CC1=WE#=Low at the rising edge of K of the following cycle, the device enters the SRAM Write mode. Write data from the I/O pins to the SRAM. Addresses As0-As11are used to select the location to be written.**



## Buffer Read Transfer (DTBR→SRAM)




Note : Output is transparent.

# Buffer Read Transfer

SRAM Read

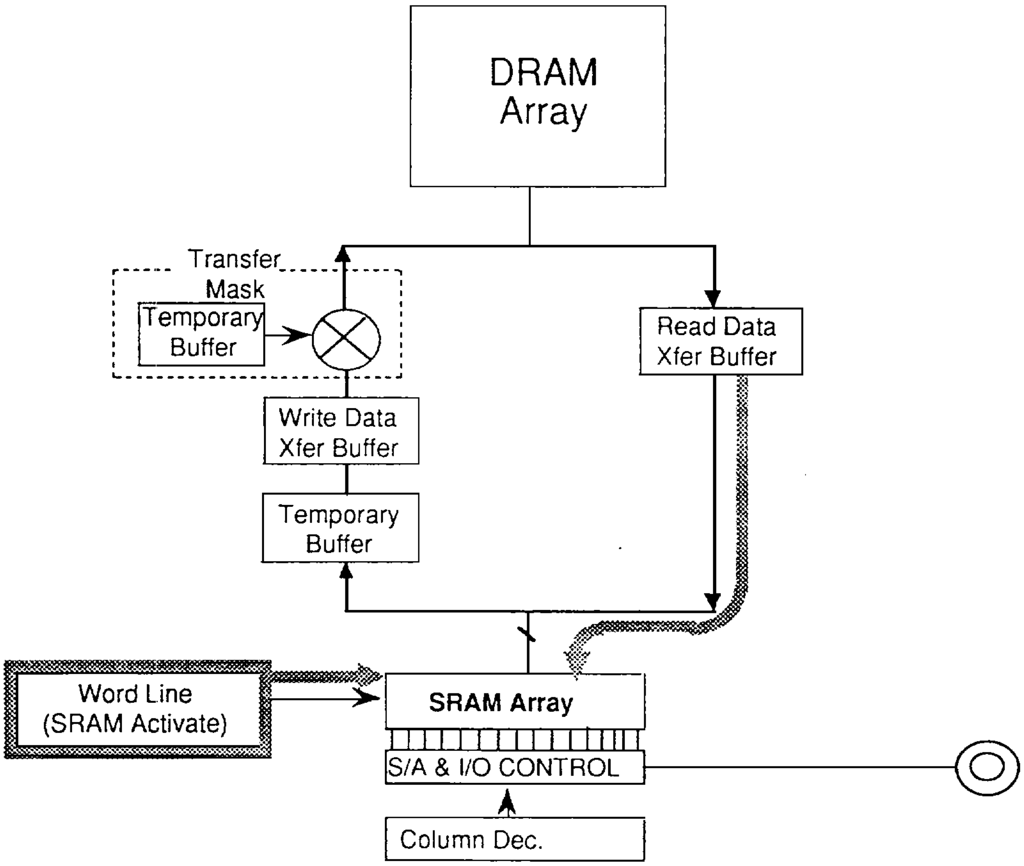
If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.

**Buffer Read Transfer**

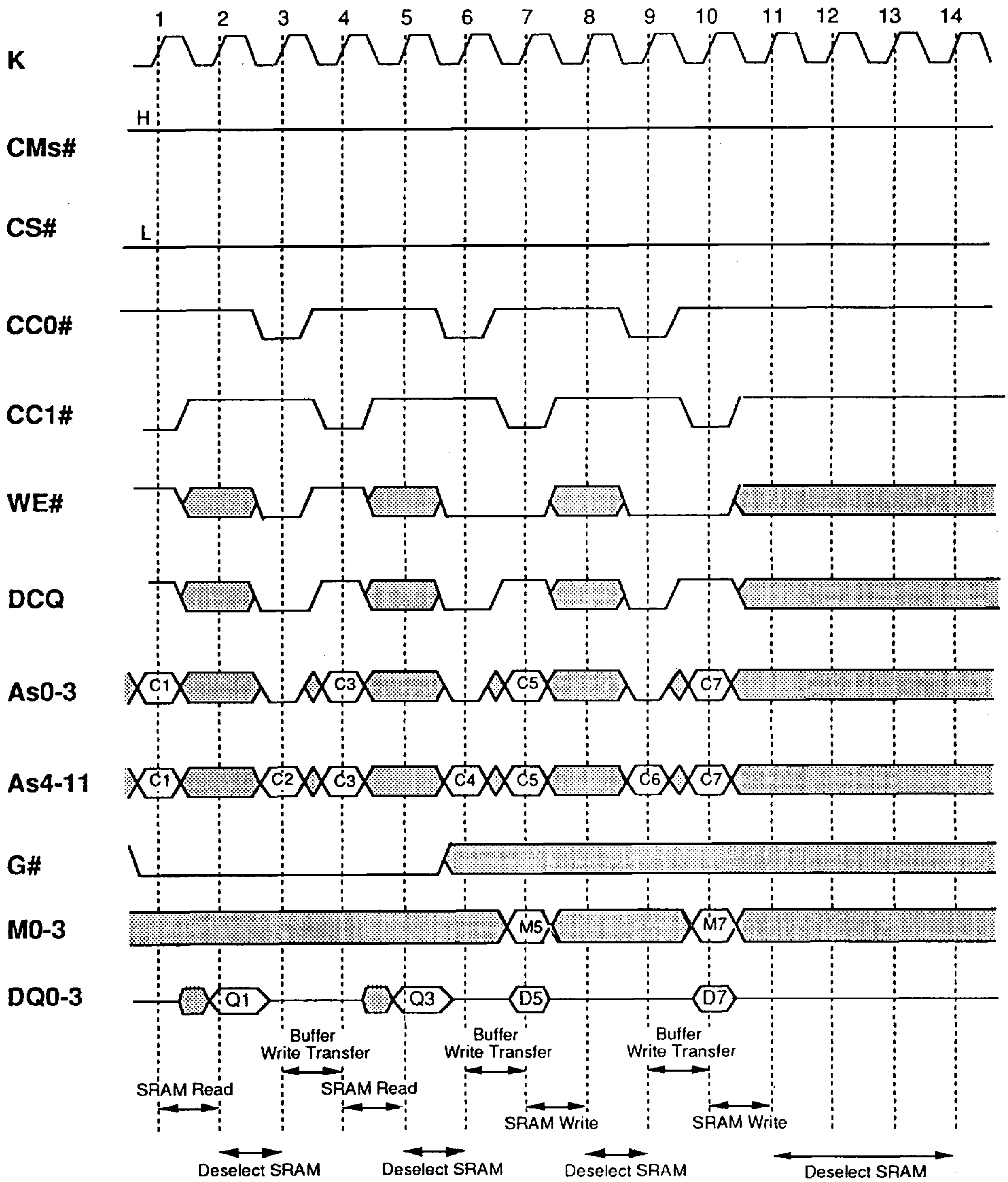
**If CMs#=High at the rising edge of K and CS#=CC0#=DQC=Low and CC1#=WE#=High at the rising edge of K of the following cycle, the device enters the Buffer Read Transfer mode. Data is transferred from the Read Data Transfer Buffer (DTBR) to the SRAM. Addresses As4-As9 are used to select the 16X4 bit block to be transferred. Addresses As0-As3 and A10-A11 must be set low.**

SRAM Write

If CMs#=High at the rising edge of K and CC0#=DQC=High and CS#=CC1#=WE#=Low at the rising edge of K of the following cycle, the device enters the SRAM Write mode. Write data from the I/O pins to the SRAM. Addresses As0-As11 are used to select the location to be written.



## Buffer Write Transfer (SRAM→DTBW)




Note: Output is transparent.

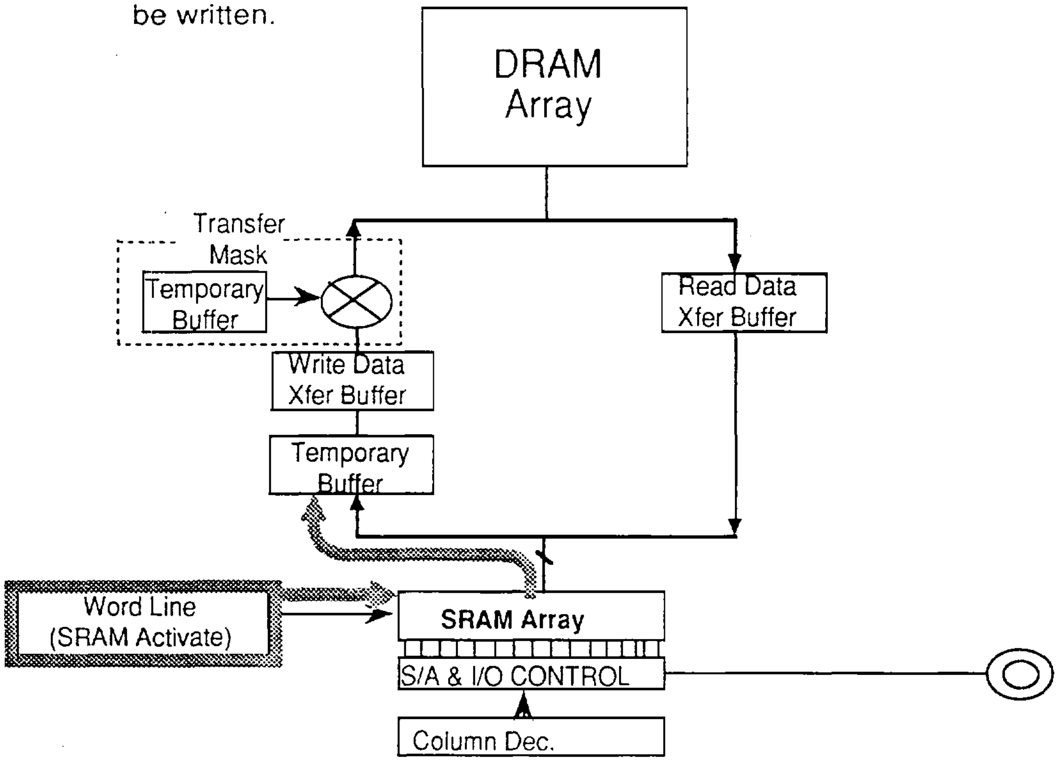
## Buffer Write Transfer

**SRAM Read** — If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.

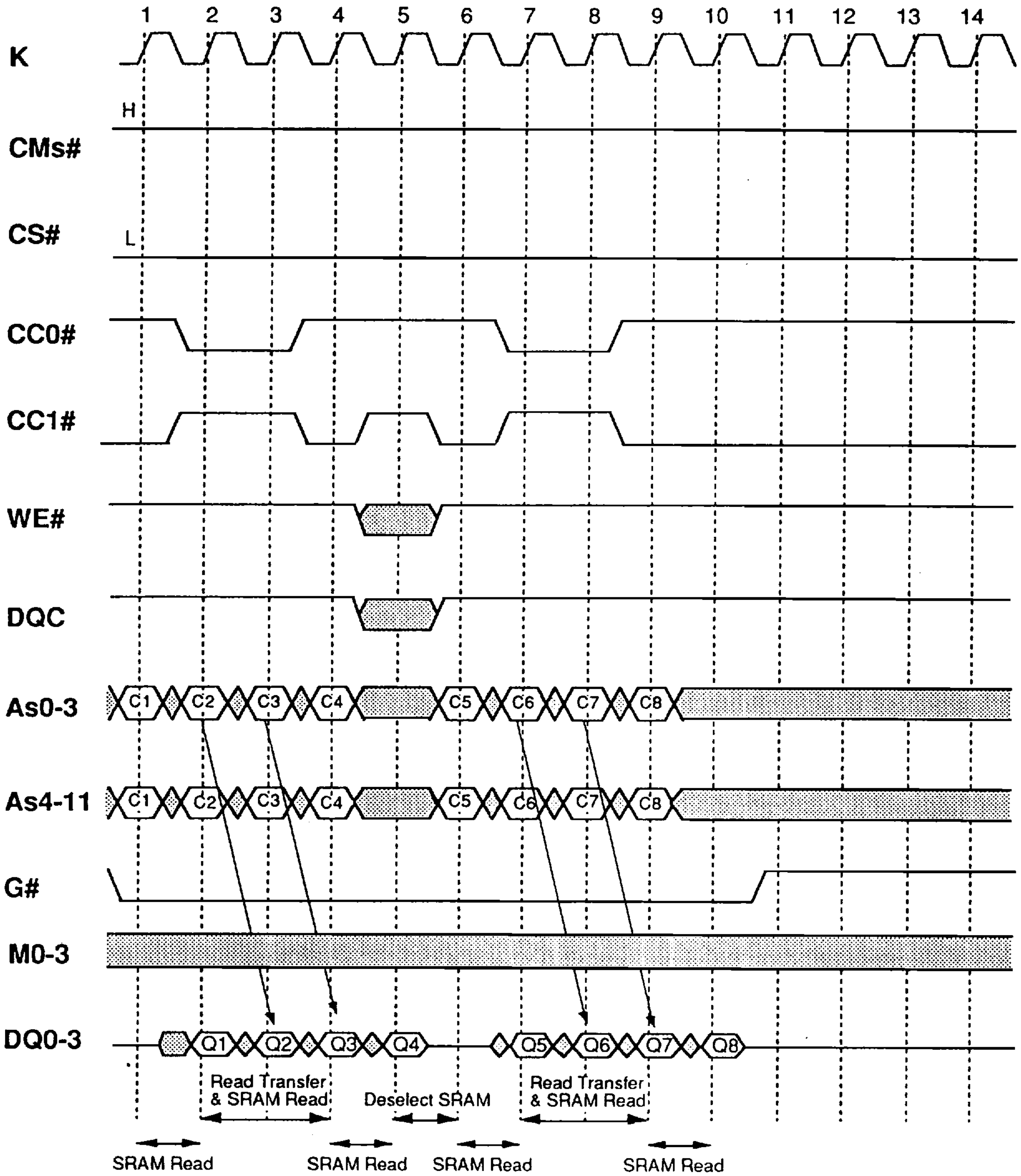
**Deselect SRAM** — If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.

**Buffer Write Transfer** — **If CMs#=High at the rising edge of K and CS#=CC0#=WE#=DQC=Low and CC1#=High at the rising edge of K of the following cycle, the device enters the Buffer Write Transfer mode. Data is transferred from the SRAM to the Temporary Buffer. Addresses As4-As11 are use to select the 16X4 bit block to be transferred. Addresses As0-As3 and A10-A11 must be set low. The Buffer Write Transfer cycle "Resets" (=0) all mask bits in the 16X4 bit mask register (All Data can be transferred).**

**SRAM Write** — If CMs#=High at the rising edge of K and CC0#=DQC=High and CS#=CC1#=WE#=Low at the rising edge of K of the following cycle, the device enters the SRAM Write mode. Write data from the I/O pins to the SRAM. Addresses As0-As11 are used to select the location to be written.



## Buffer Read Transfer & SRAM Read (DTBR→SRAM→Output)




Note: Output is transparent.

# Buffer Read Transfer and SRAM Read

SRAM Read

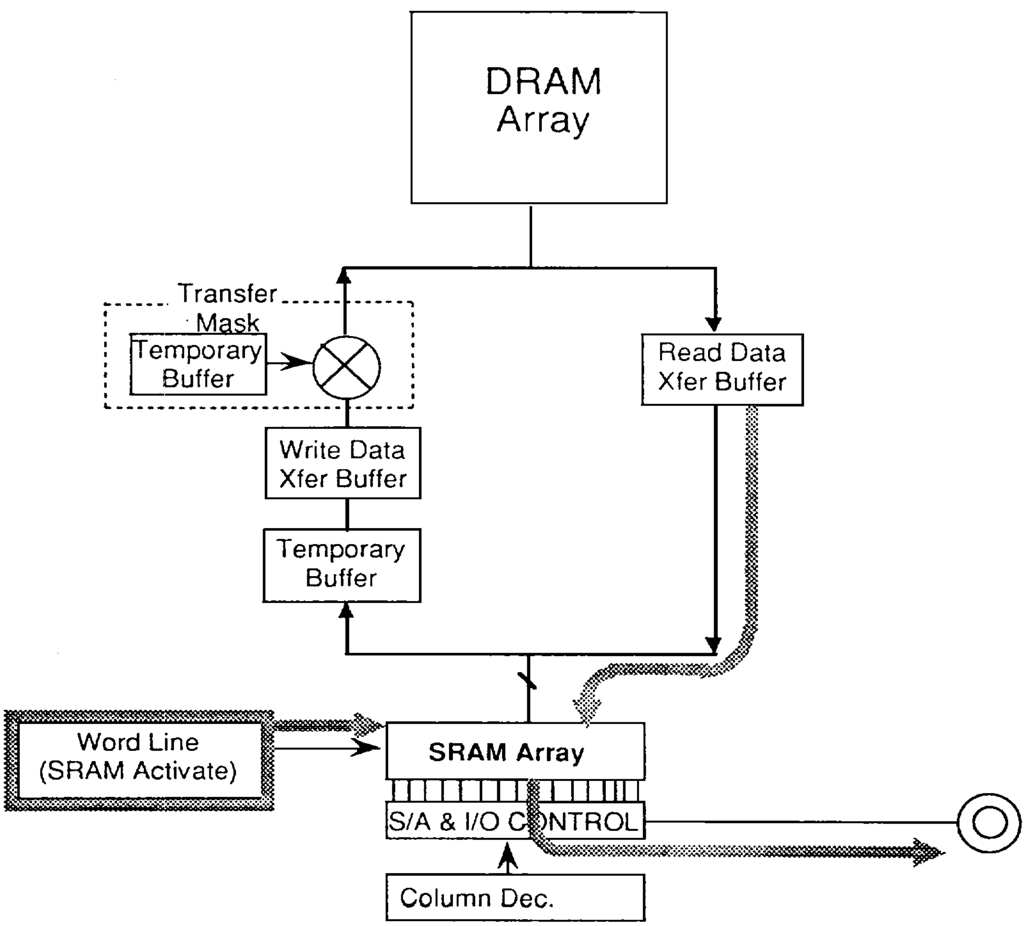
If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.

**Buffer Read Transfer and SRAM Read**

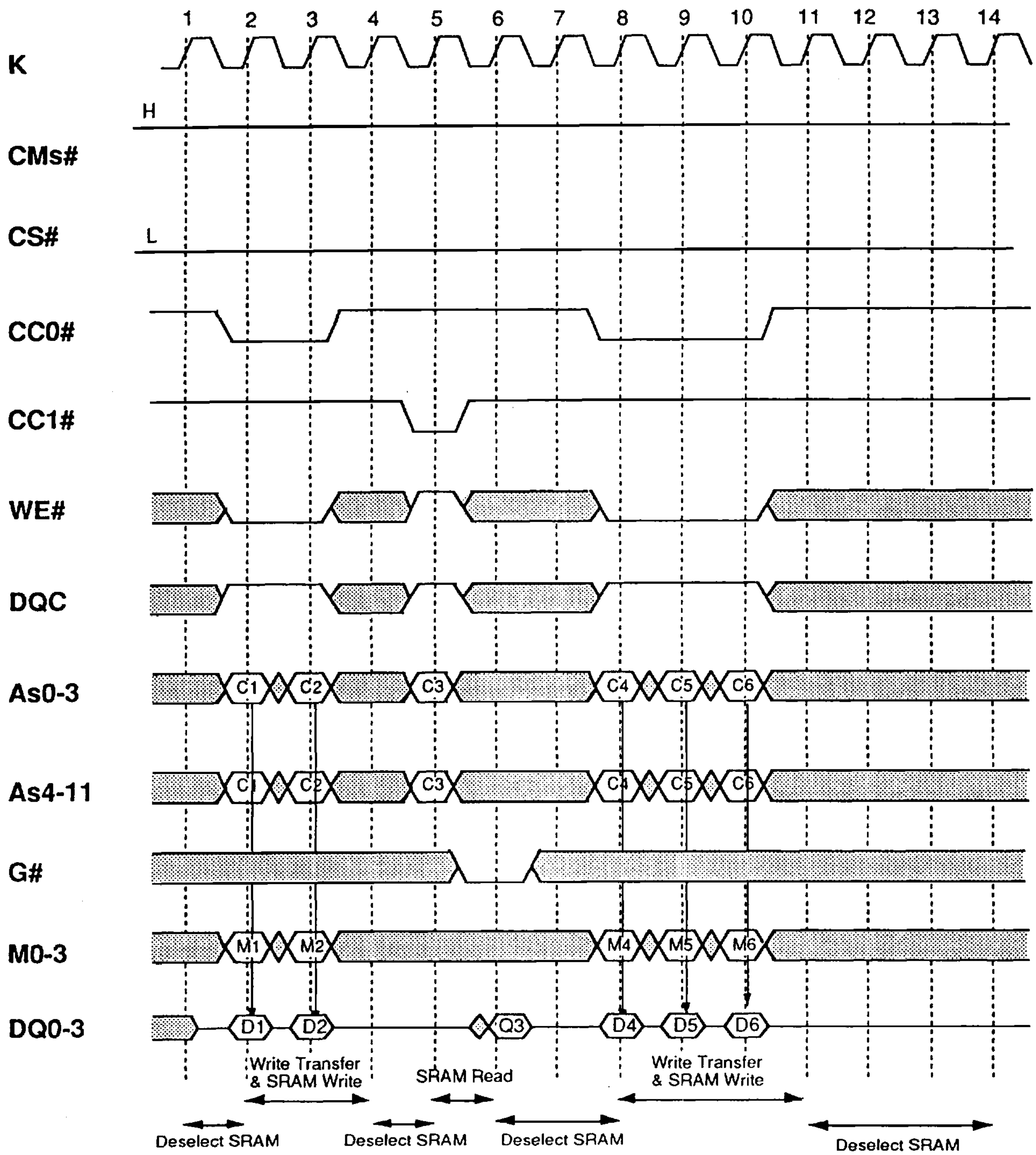
**If CMs#=High at the rising edge of K and CS#=CC0#=Low and CC1#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the Buffer Read Transfer and SRAM Read mode. Data (16 X4 bit block) is transferred from the Read Data Transfer Buffer (DTBR) to the SRAM, and simultaneously, data (16 bit word) is read from the DTBR to the I/O pins.**

Deselect SRAM

If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.



## Buffer Write Transfer & SRAM Write (Input→SRAM→DTBW)




Note: Output is transparent.

# Buffer Write Transfer and SRAM Write

**Deselect SRAM**

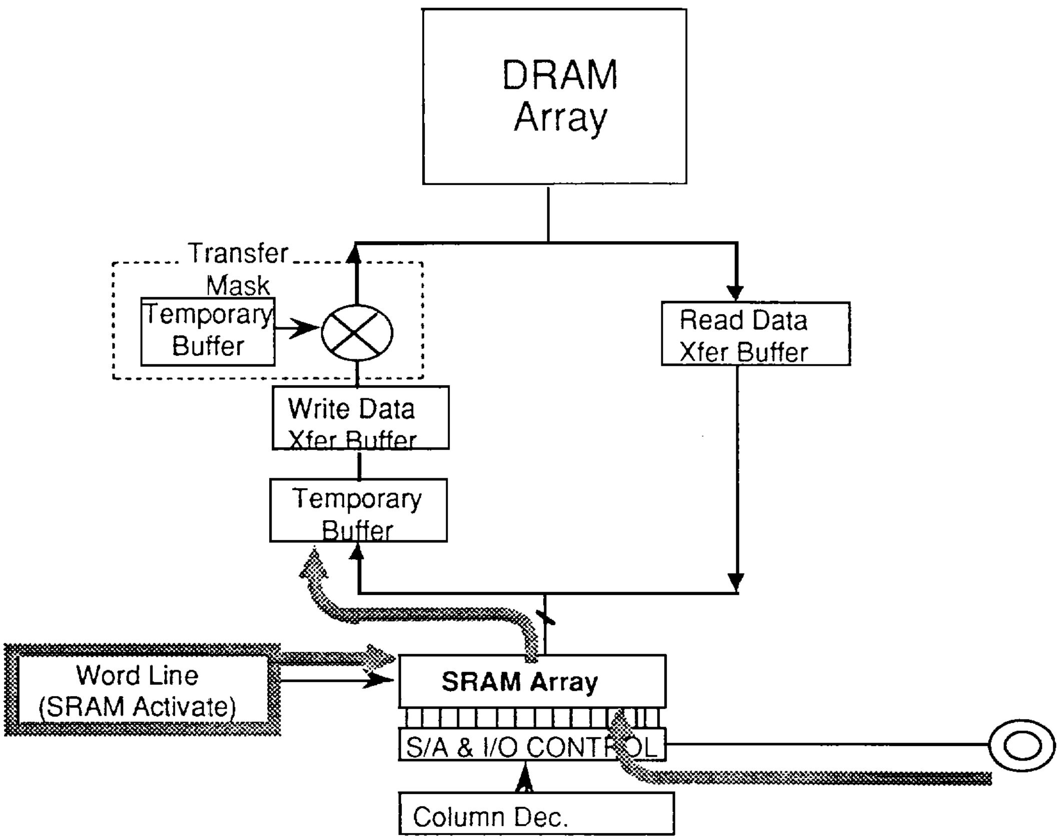
If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.

**SRAM Read**

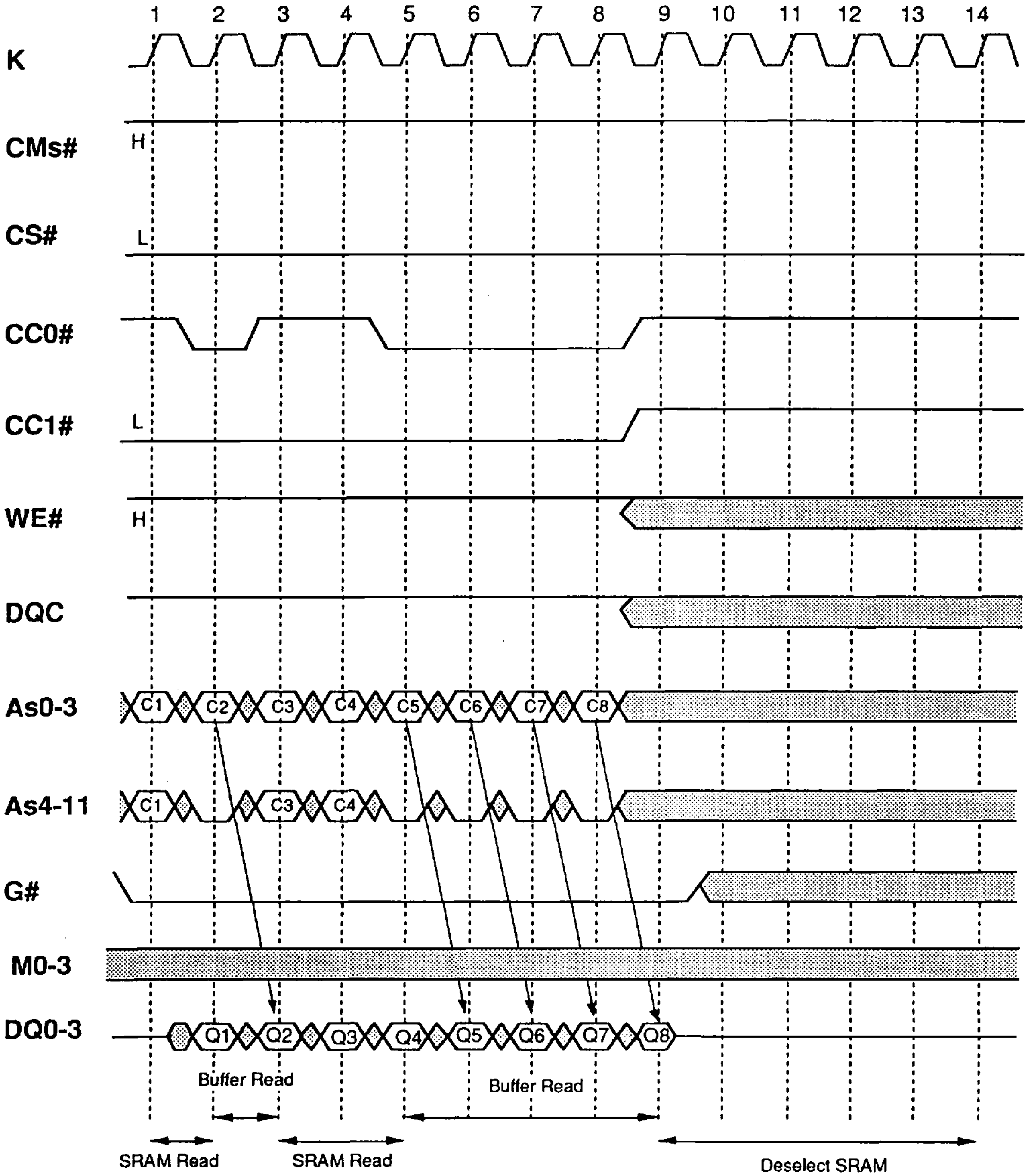
If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.

**Buffer Write Transfer and SRAM Write**

**If CMs=High at the rising edge of K and CS#=CC0#=WE#=Low and CC1#=DQC=High at the rising edge of K of the following cycle, the device enters the Buffer Write Transfer and SRAM Write mode. Data (4-bit word) is written from the I/O pins to SRAM, and then the 16X4 bit block is transferred from SRAM to the Temporary Buffer. This operation is completed in one cycle. This operation "Resets" (=0) all mask bits in the 16X4 bit mask register (All Data can be transferred).**



## Buffer Read (DTBR→ Output)




Note: Output is transparent.

# Buffer Read

SRAM Read

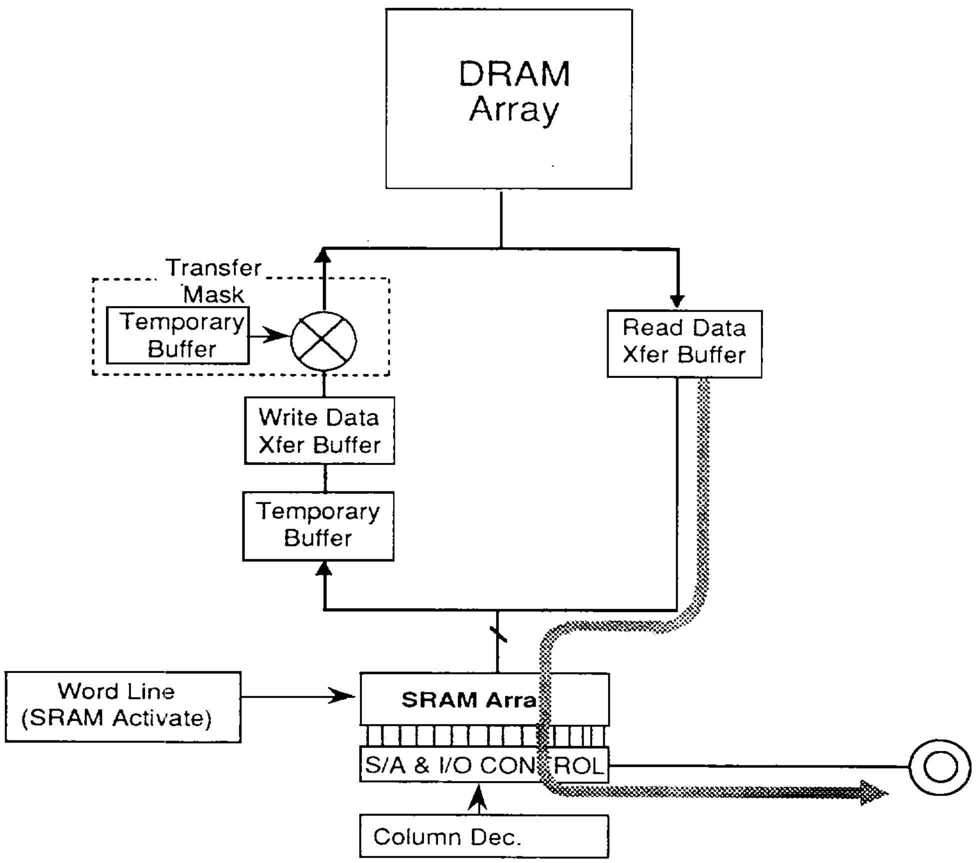
If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.

**Buffer Read**

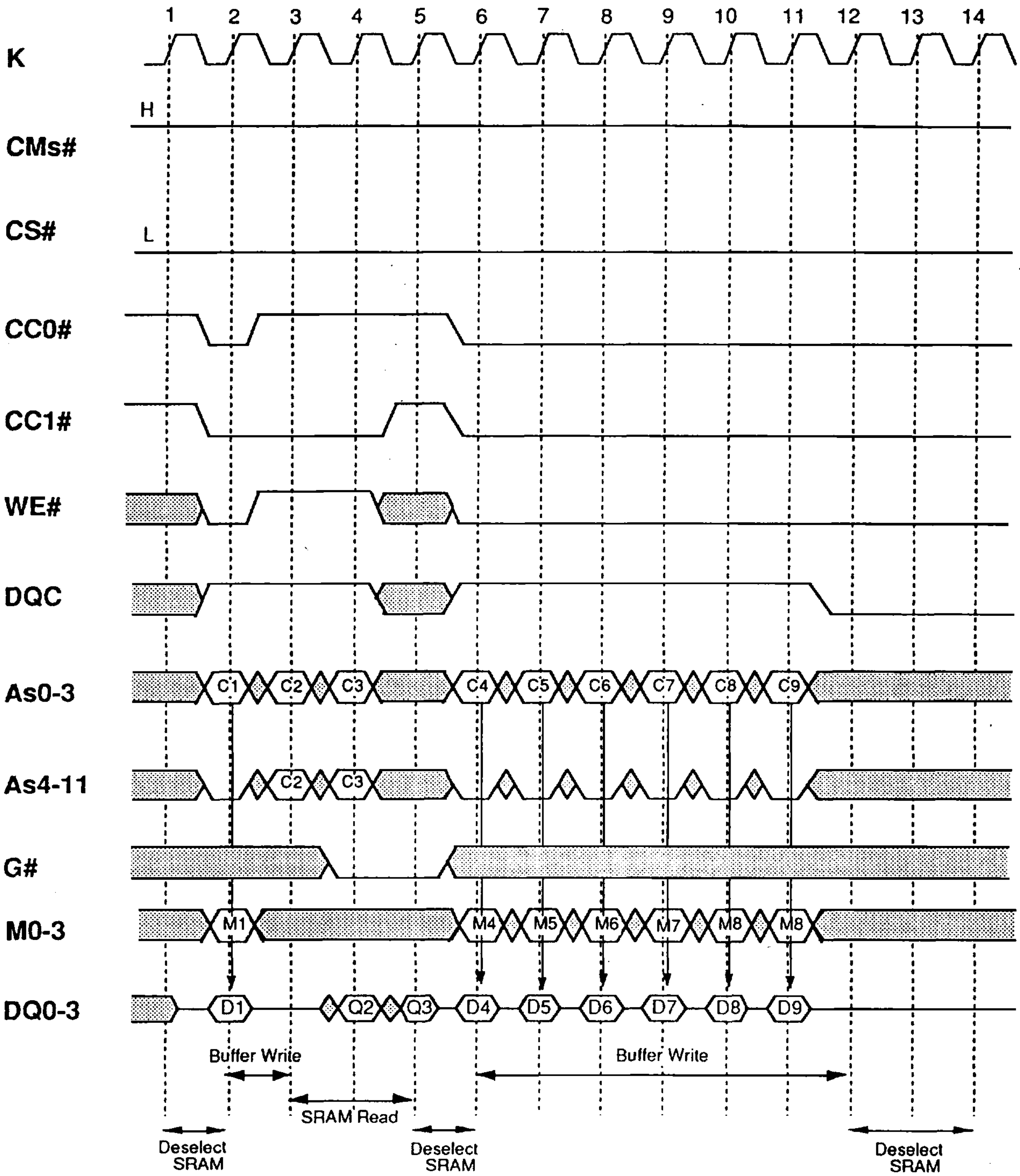
**If CMs#=High at the rising edge of K and CS#=CC0#=CC1#=Low and WE#=DQC=High at the rising edge of K of the following cycle, the device enters the Buffer Read mode.Data is read from the Read Data Transfer Buffer (DTBR) to the I/O pins. Addresses As0-As3 are used to select (1 of 16) the 4-bit word to be read from the DTBR. Addresses As4-As11 must be set low for this operation.**

Deselect SRAM

If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.



## Buffer Write (Input→DTBW)



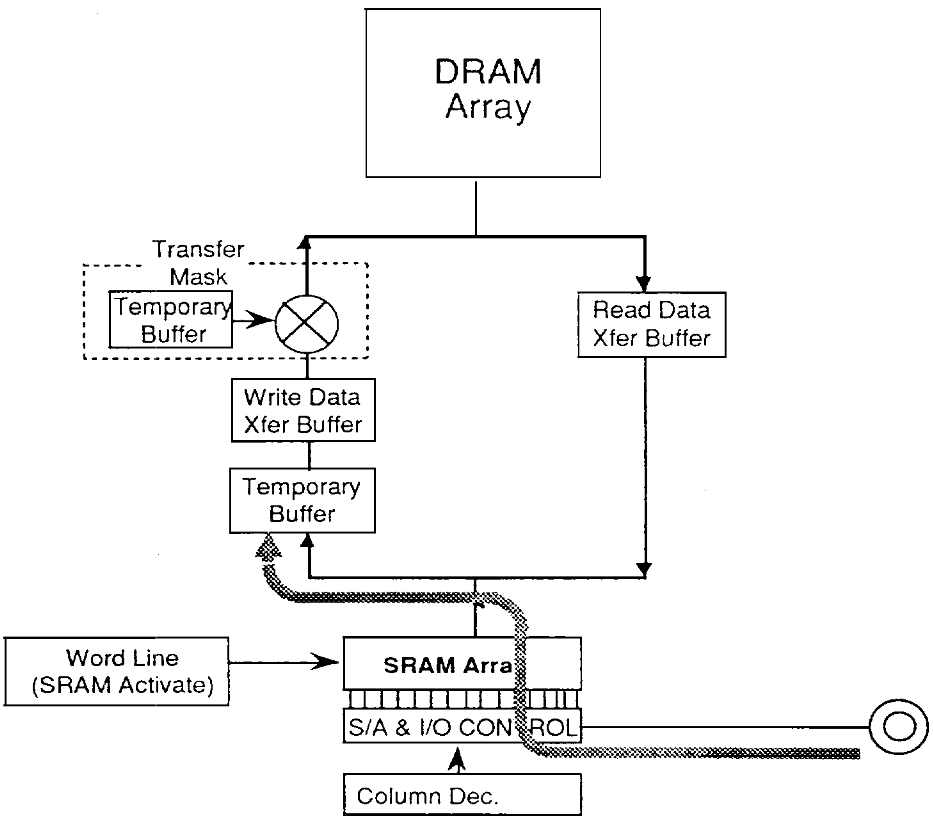

Note: Output is transparent.

# Buffer Write

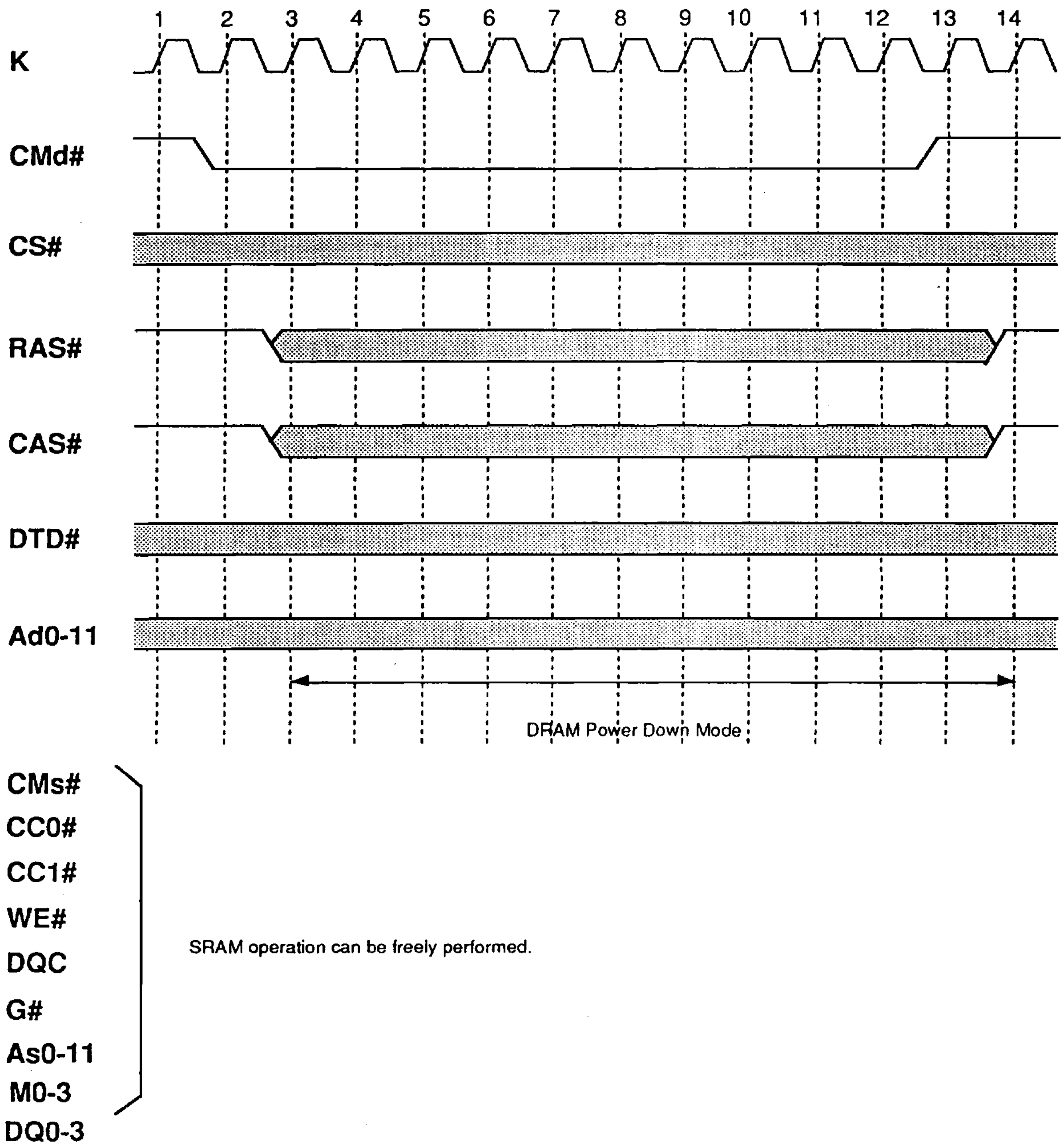
**Deselect SRAM**
If CMs#=High at the rising edge of K, and CS#=Low and CC0#=CC1#=High at the rising edge of K of the following cycle, the SRAM is deselected. During this mode, all transfer functions and input/output operations to and from the SRAM and Buffer are disabled. The SRAM Sense Amps are not powered down. This cycle is useful for change in output impedance (R->W, W->R) without G# control.

**Buffer Write**
**If CMs#=High at the rising edge of K and CS#=CC0#=CC1#=WE#=Low and DQC=High at the rising edge of K of the following cycle, the device enters the Buffer Write mode. Data is written from the I/O pins to the Write Data Transfer Buffer (DTBW). Addresses As0-A3 are used to select (1 of 16) the 4-bit word to be written. Addresses As4-As11 must be set low for this operation.**

**SRAM Read**
If CMs#=High at the rising edge of K and CS#=CC1#=Low and CC0#=WE#=DQC=High at the rising edge of K of the following cycle, the device enters the SRAM Read mode. Data is read from the SRAM to the I/O pins. Addresses As0-As11 are used to select the data.



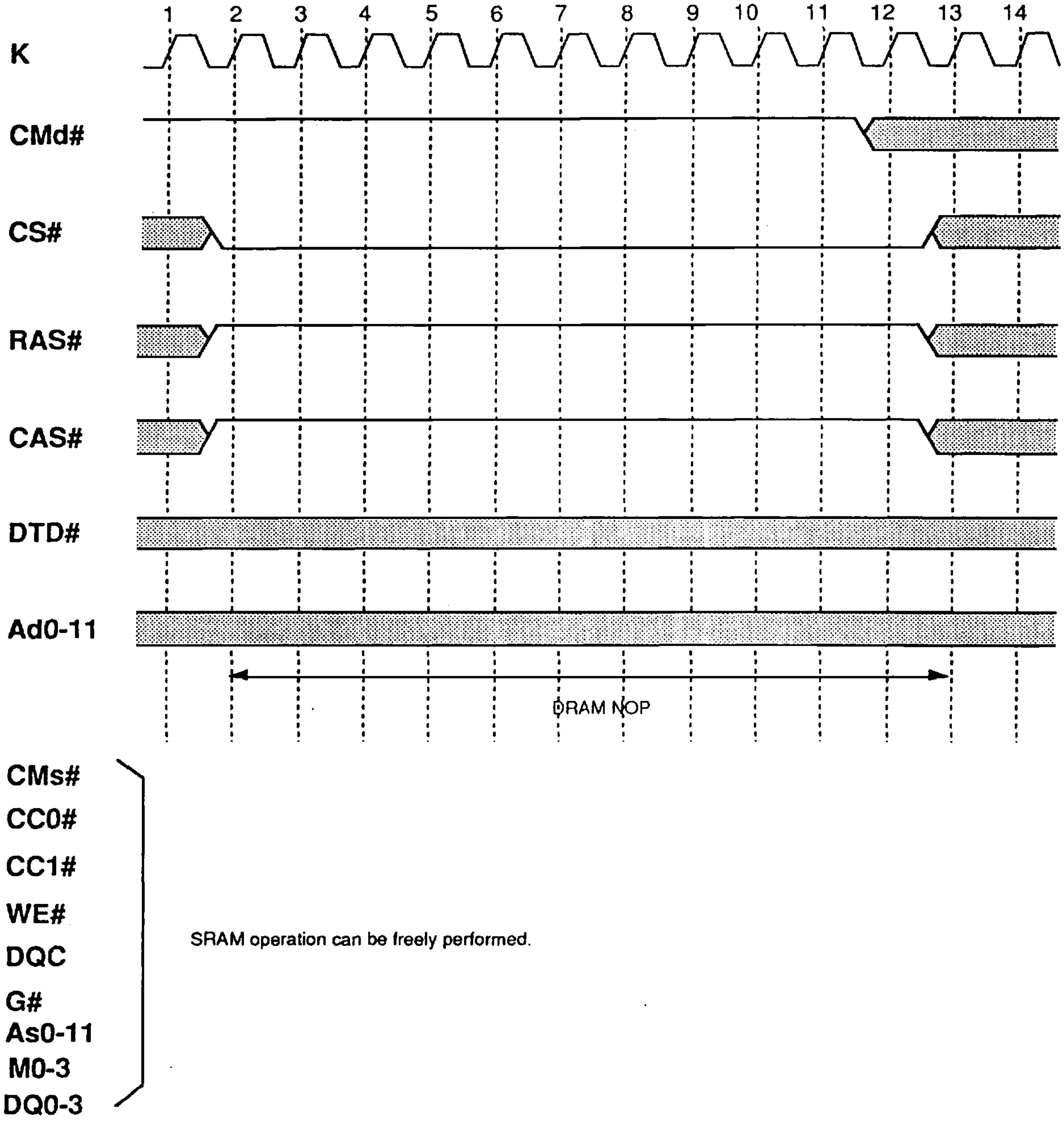
## DRAM Power Down



# DRAM Power Down

| | |
|---|---|
| DRAM Power Down | If CMd#=Low at the rising edge of K, the DRAM goes into power down mode at the next rising edge of K. During this mode, the internal DRAM K clock becomes inactive. |

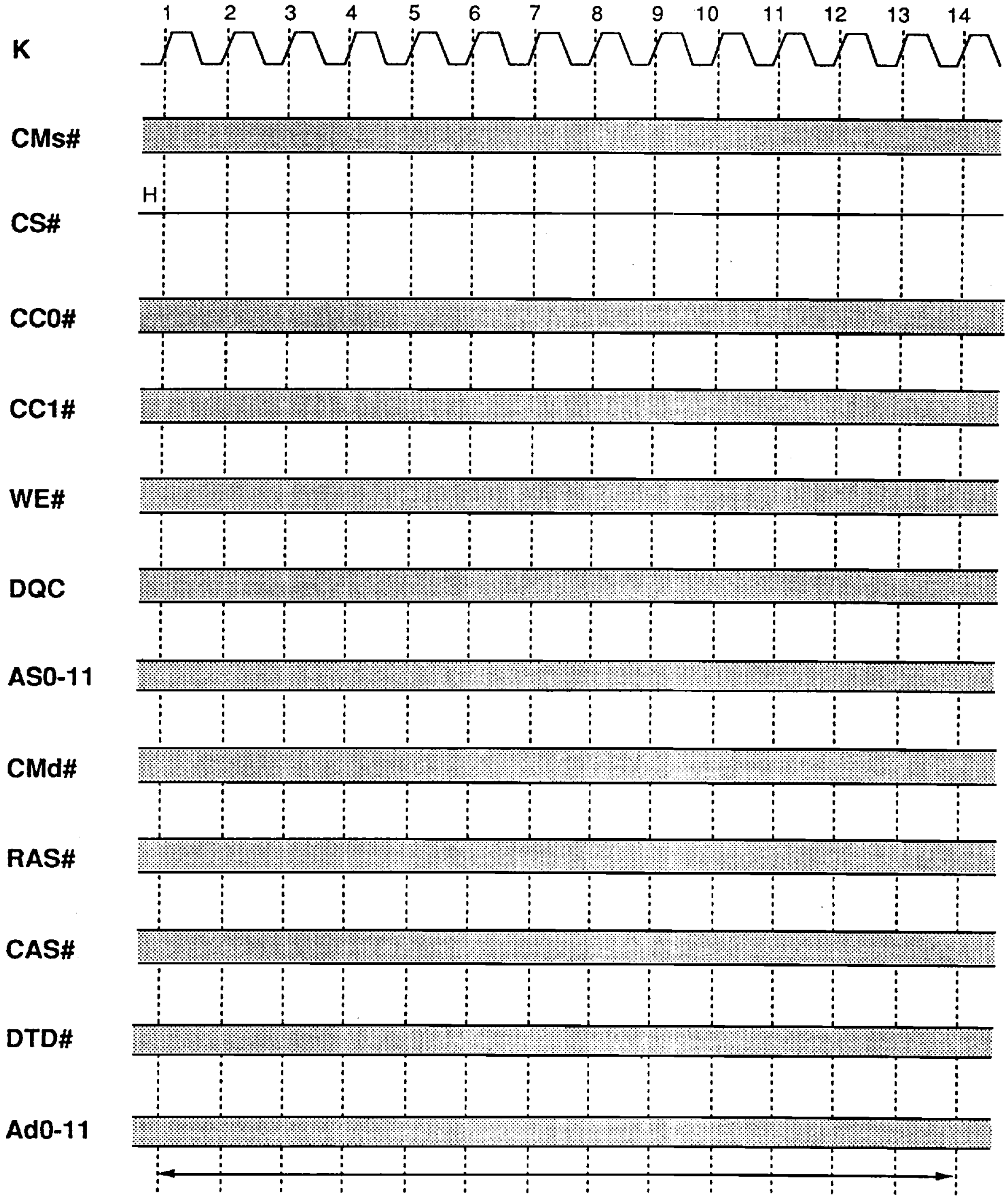
## DRAM NOP


1
2
3
4
5
6
7
8
9
10
11
12
13
14
K
CMd#
CS#
RAS#
CAS#
DTD#
Ad0-11
DRAM NOP
CMs#
CC0#
CC1#
WE#
DQC
G#
As0-11
M0-3
DQ0-3
SRAM operation can be freely performed.

# DRAM No-Operation (NOP)

**DRAM NOP** If CMd#=High at the rising edge of K, and CS#=Low and RAS#=CAS#=High at the rising edge of K of the following cycle, a DRAM NOP cycle is performed. The NOP cycle is used when no other DRAM operations are desired, allowing the DRAM to stay in its present (precharge/activate) state.

## NO - Operation

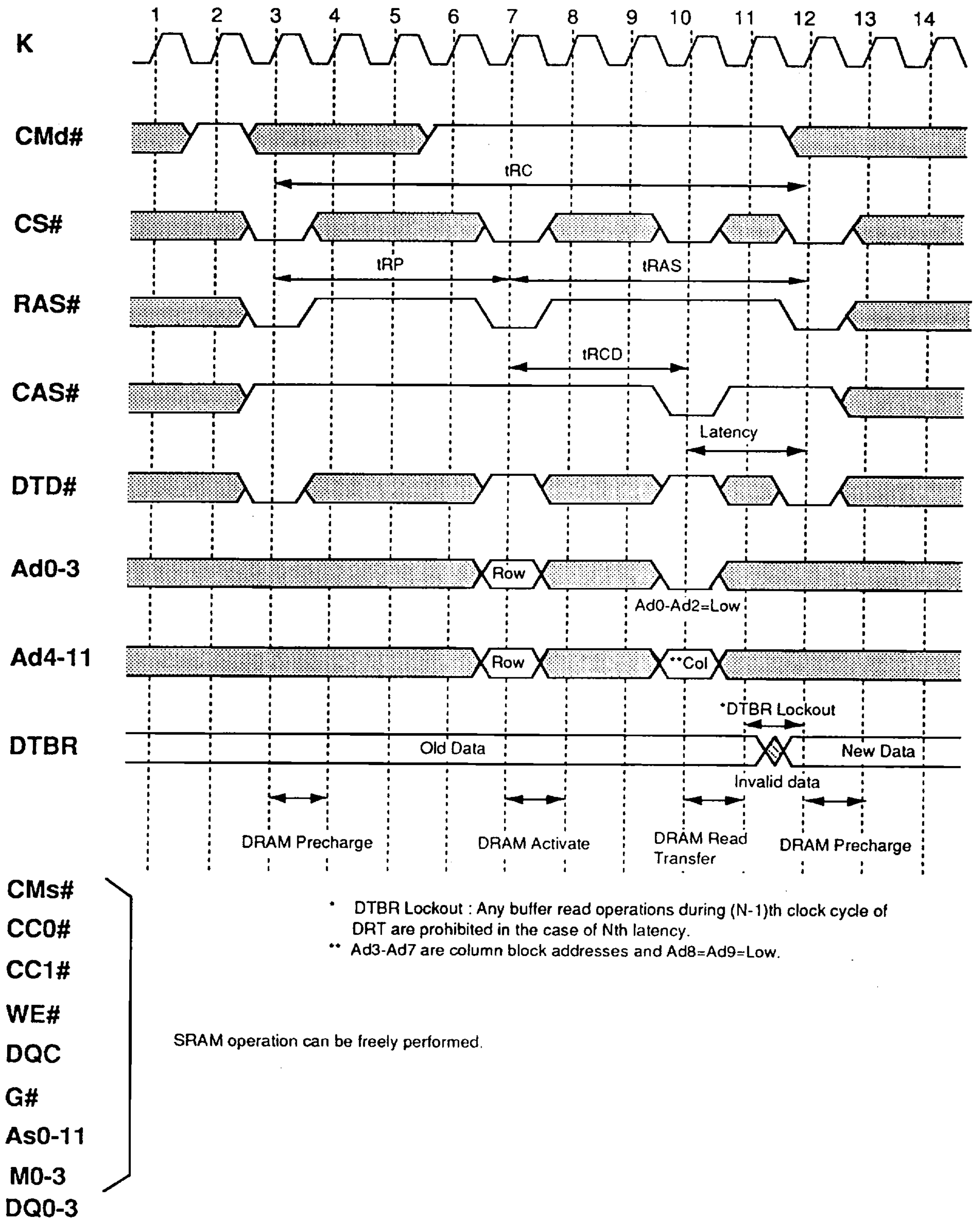



NO-Operation Mode

## No-Operation (NOP)

| | |
|---|---|
| NOP | If CS#=High at rising edge of K device enters No-Operation mode and all input signals are disabled . |

## DRAM Read Transfer




* DTBR Lockout : Any buffer read operations during (N-1)th clock cycle of DRT are prohibited in the case of Nth latency.

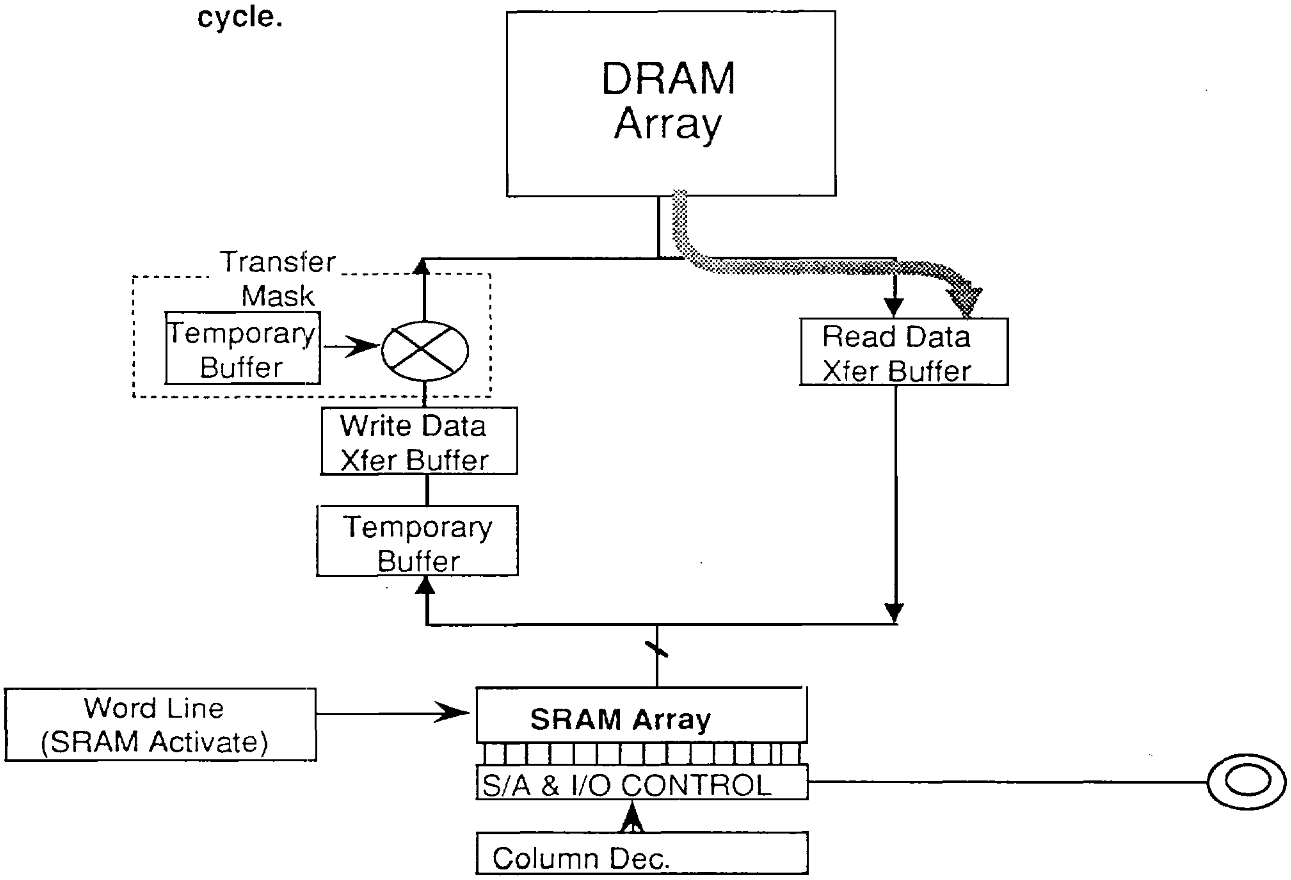
** Ad3-Ad7 are column block addresses and Ad8=Ad9=Low.

# DRAM Read Transfer

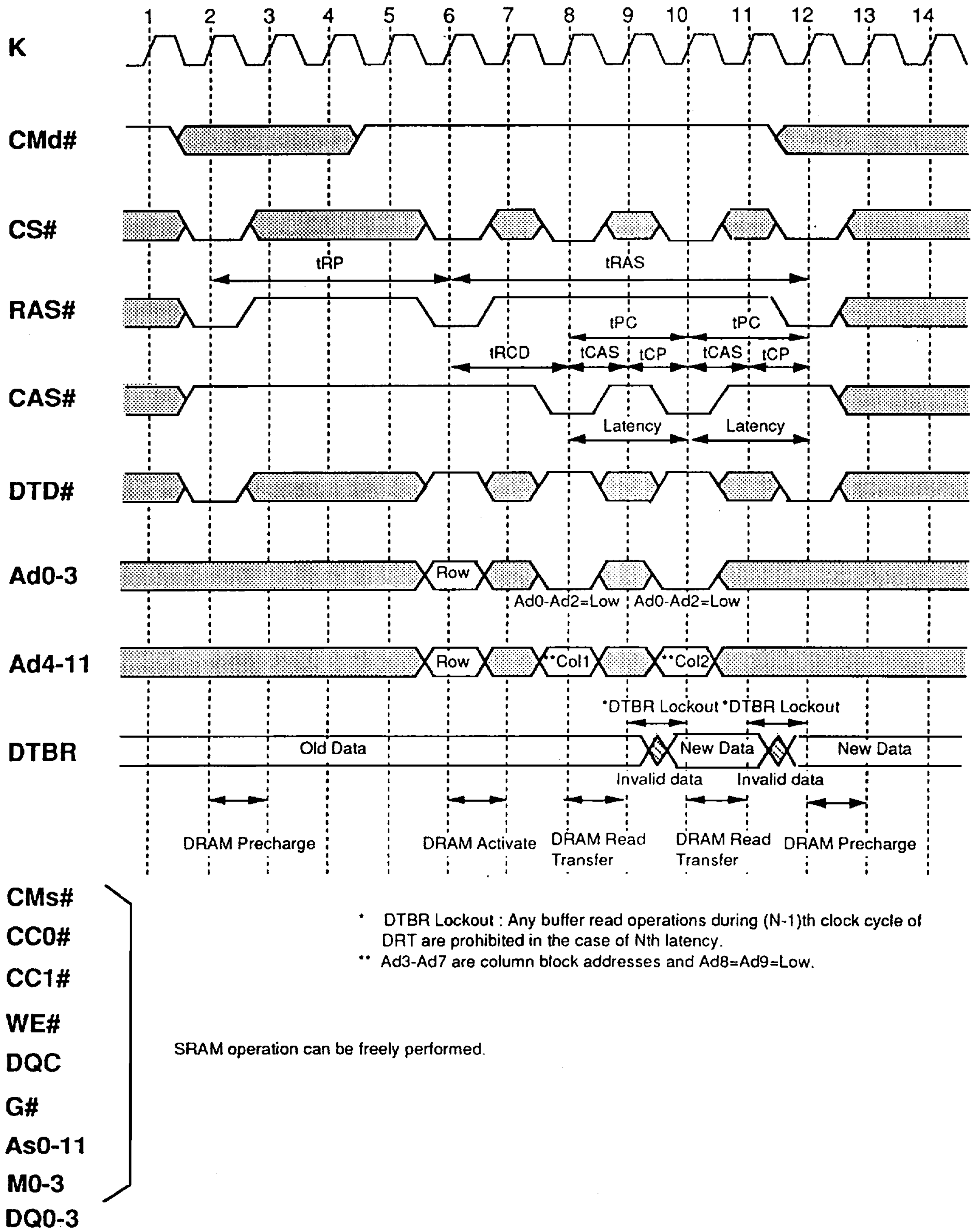
**DRAM Precharge** If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle.

**DRAM Activate** If CMd#=High at the rising edge of K, and CS#=RAS#=Low and CAS#=DTD#=High at the rising edge of K of the following cycle, the DRAM enters active mode. Addresses are latched from the Ad0-Ad9 inputs by the same rising edge of K. Internally, a DRAM row is selected. A DRAM precharge cycle must separate all DRAM Activate cycles (when a new DRAM row is accessed).

**DRAM Read Transfer** **If CMd#=High at the rising edge of K and RAS#=DTD#=High and CS#=CAS#=Low and at the rising edge of K of the following cycle (following a DRAM Activate cycle), a DRAM Read Transfer is performed. A Block of Data is transferred from the DRAM to the DTBR as specified by Addresses Ad4-Ad9 (Latched @ CAS#=L, K=rising edge). Addresses Ad0-Ad3 and Ad10-Ad11 must be set to Low. No other operations involving the DTBR are allowed during the (n-1)th K-clock cycle following the initiation of the DRAM Read Transfer (CAS#=L @ K-rising edge), where "n" is the latency defined during the "Set Command Register" cycle.**



## DRAM Read Transfer(Page Mode)

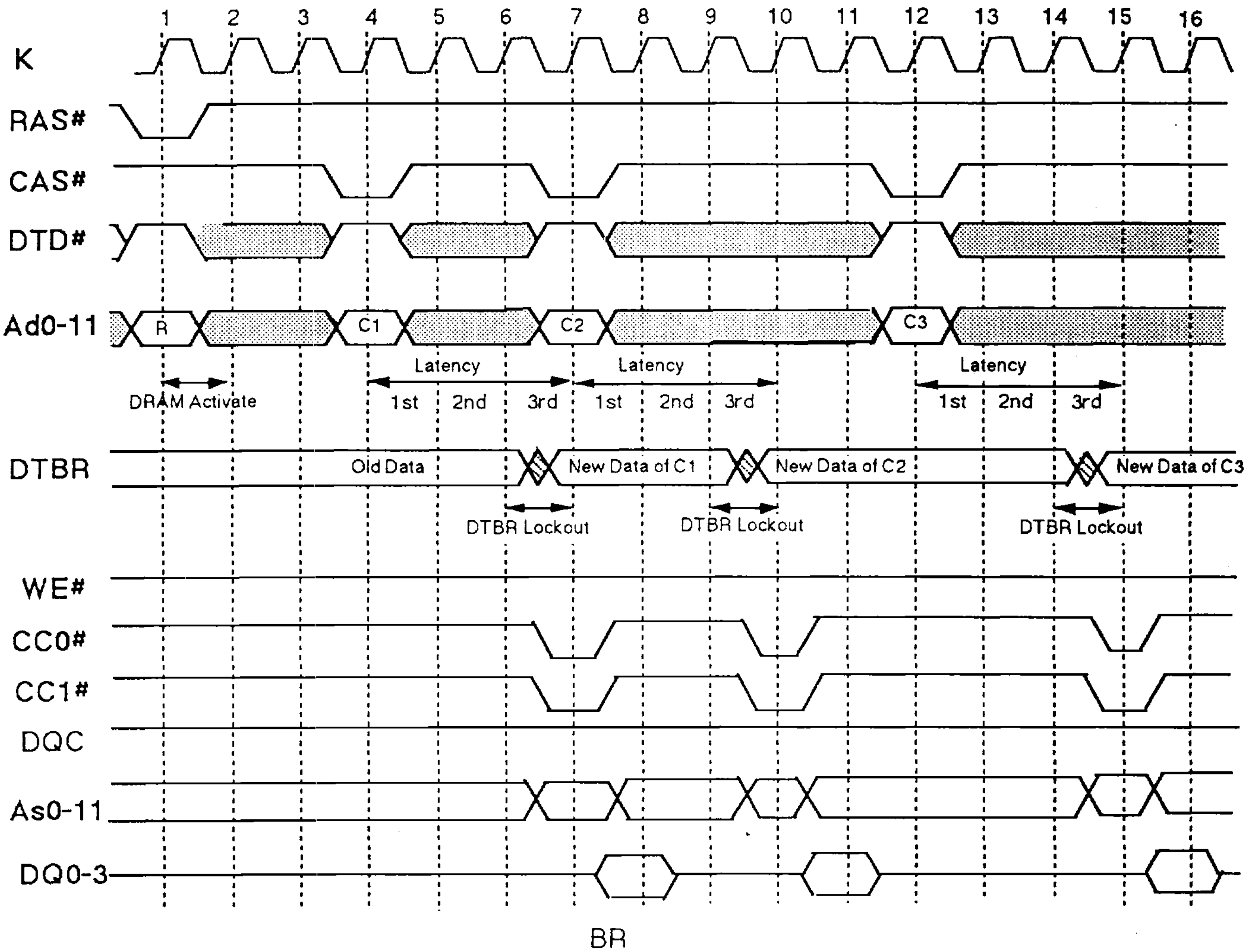



* DTBR Lockout : Any buffer read operations during (N-1)th clock cycle of DRT are prohibited in the case of Nth latency.

** Ad3-Ad7 are column block addresses and Ad8=Ad9=Low.

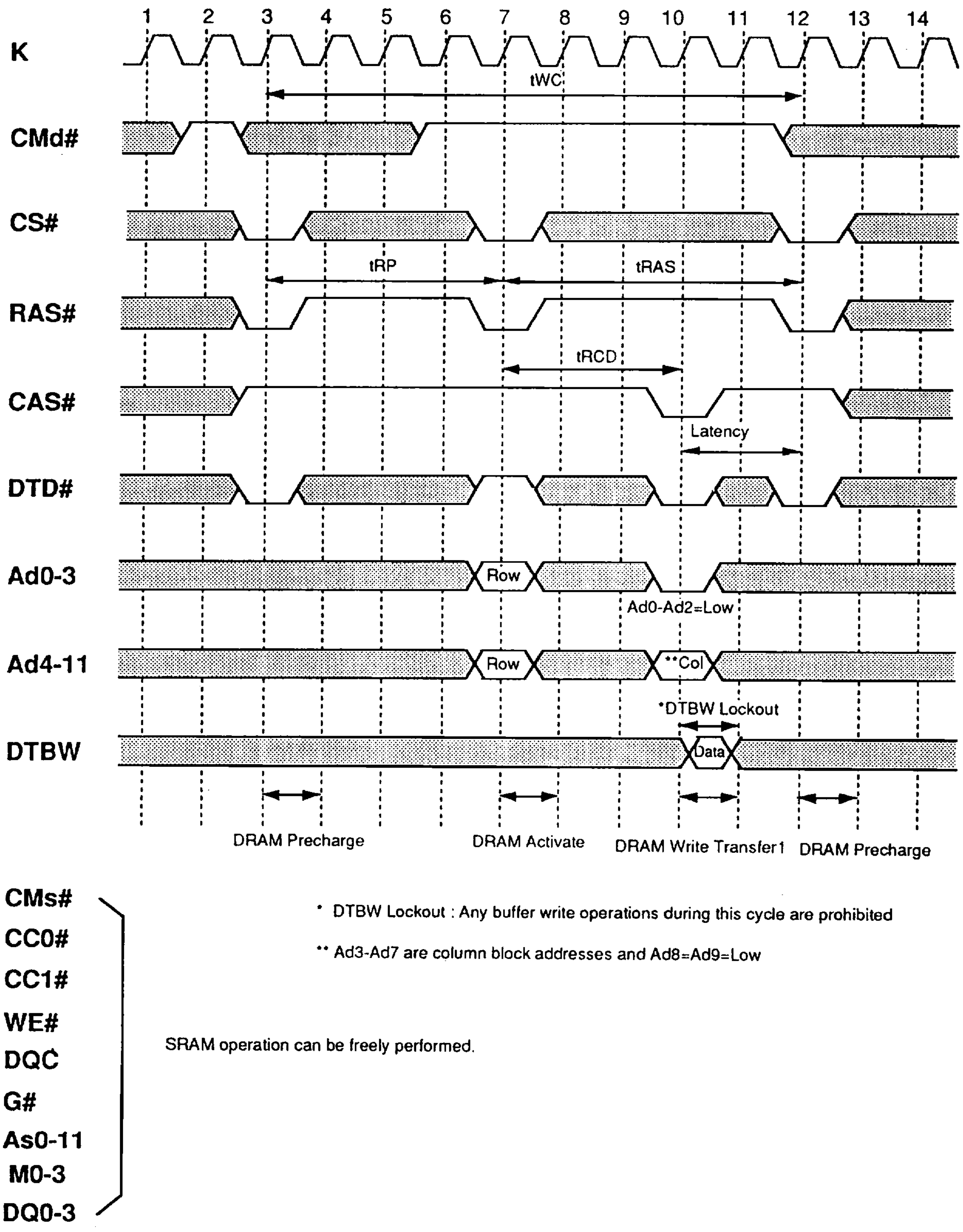
Detailed DRAM Read Transfer description

After row addresses are asserted by DRAM Activate command (ACT) and the selected row is activated in time of tRCD later, column blocks are ready to be transferred from DRAM to DTBR(Data Transfer Buffer <Read>) by DRAM Raed Transfer command (DRT). Data is transferred synchronously to K of N cycle later where N is the page_latency. The page_latency must be programmed in Set Command Register cycle(SCR). The border of old data and new data in DTBR is described as below.




The Latency means the number of the clocks where the new data can be transferred from DTBR to SRAM and/or DQ pins,which is similar to Access time of DRAM.
It is prohibited to transfer from DTBR to SRAM or DQ pins(BRT/BRTR/BR) during (N-1)th clock cycle of DRT, where N is the Latency.

## DRAM Write Transfer 1




* DTBW Lockout : Any buffer write operations during this cycle are prohibited

** Ad3-Ad7 are column block addresses and Ad8=Ad9=Low

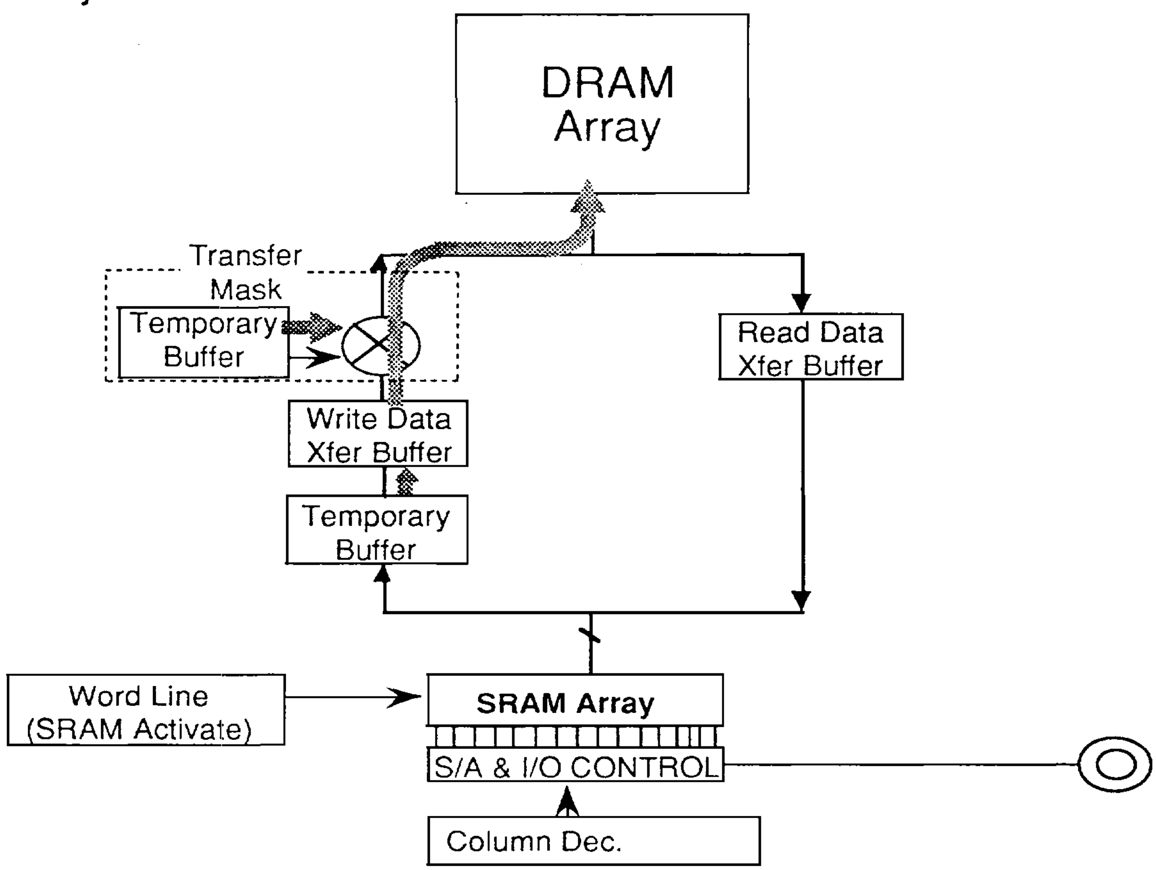
SRAM operation can be freely performed.

# DRAM Write Transfer 1

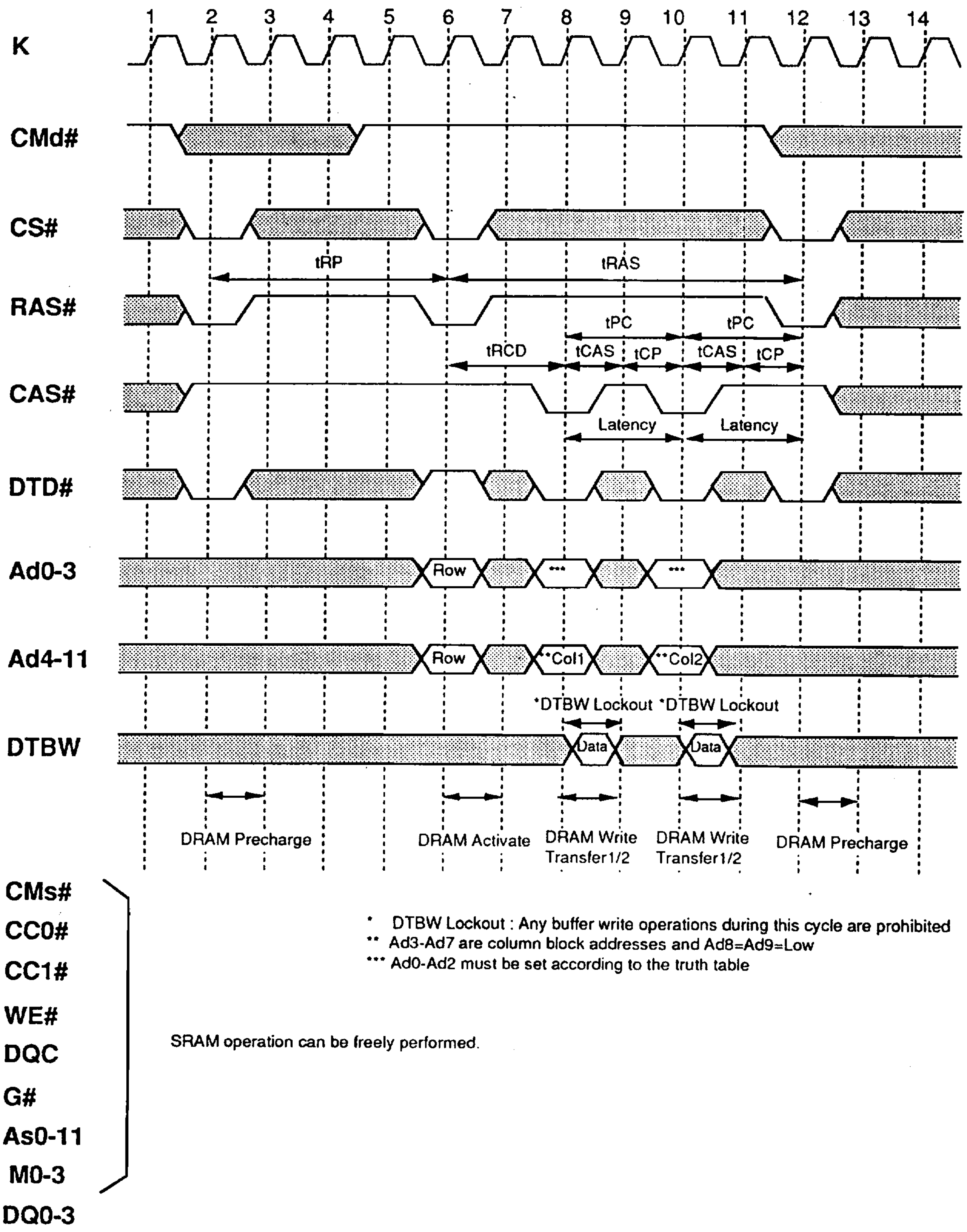
DRAM Precharge — If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle.

DRAM Activate — If CMd#=High at the rising edge of K, and CS#=RAS#=Low and CAS#=DTD#=High at the rising edge of K of the following cycle, the DRAM enters active mode. Addresses are latched from the Ad0-Ad11 inputs by the same rising edge of K. Internally, a DRAM row is selected. A DRAM precharge cycle must separate all DRAM Activate cycles (when a new DRAM row is accessed).

**DRAM Write Transfer1** — **If CMd#=High at rising edge of K and CS#=CAS#=DTD#=Low and RAS#=High at the rising edge of K of the following cycle (following a DRAM Activated cycle), a DRAM Write Transfer1 (DWT1) is performed. A Block (16 X 4 Bits) of Data is transferred from the Write Data Transfer Buffer (DTBW) to the DRAM as specified by Addresses Ad4-Ad9 (Latched @ CAS#=Low, K= rising edge time). Addresses Ad0-Ad3 and Ad10-Ad11 must be set to Low. During DWT1 cycle data of Temporary Buffer are transferred to DTBW and masked data of Temporary Buffer are loaded to the Transfer Mask and finally all the masked data are transferred to DRAM Array in N latency. The data path are opened during DWT1 cycle and are closed before the next cycle begins. No other operations involving the DTBW are allowed during the single master clock cycle in which the Write Transfer was initiated.**



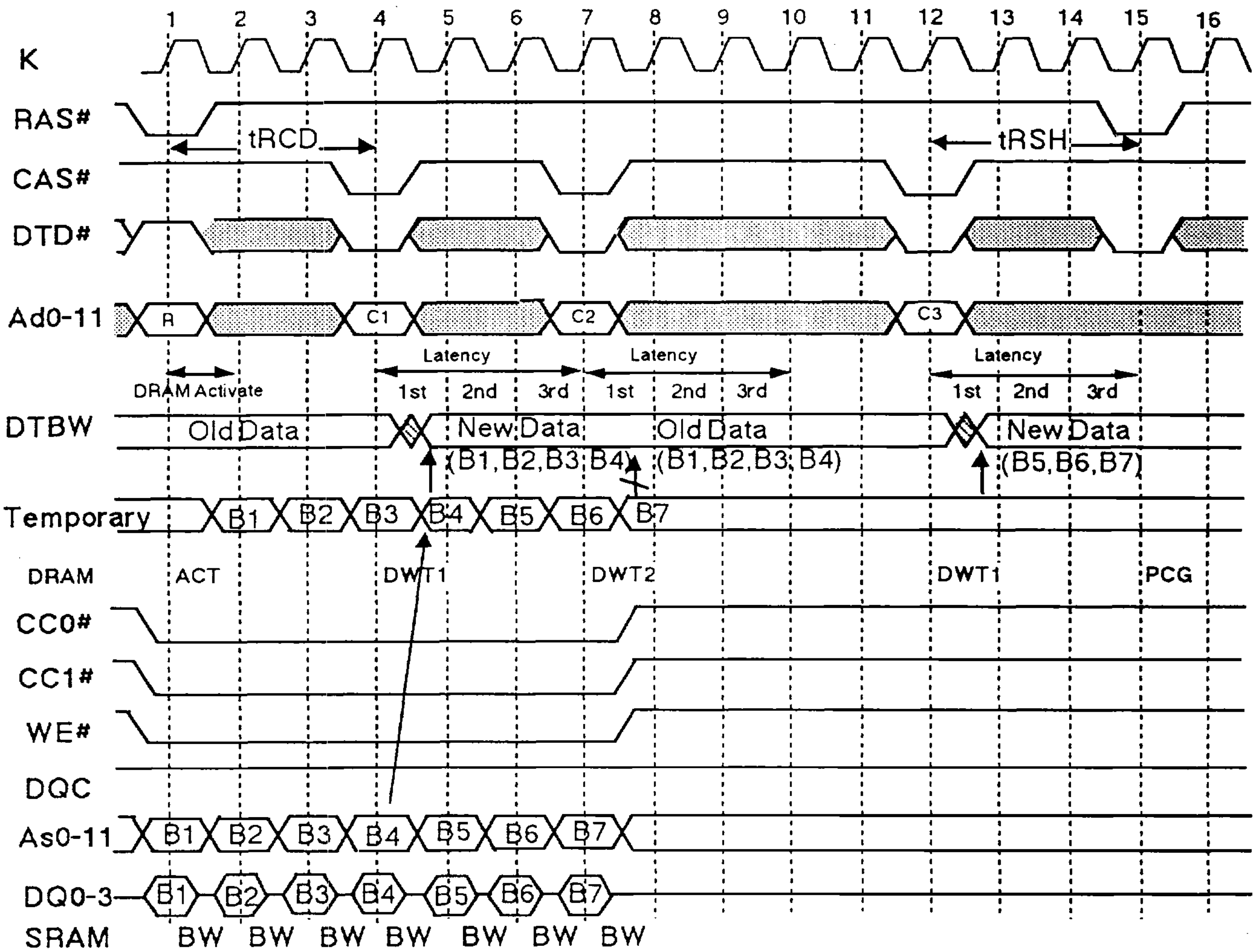
## DRAM Write Transfer1/2(Page Mode)




* DTBW Lockout : Any buffer write operations during this cycle are prohibited
** Ad3-Ad7 are column block addresses and Ad8=Ad9=Low
*** Ad0-Ad2 must be set according to the truth table

# Detailed DRAM Write Transfer description

As in the case of DRT cycle, after row addresses are asserted by DRAM Activate command (ACT) and the selected row is activated in time of tRCD later, column blocks are ready to be transferred from DTBW(Data Transfer Buffer <Write>) to DRAM by DRAM Write Transfer command (DWT).
Data is transferred synchronously to K during N cycles where N is the latency.
The latency must be programmed in Set Command Register cycle(SCR).

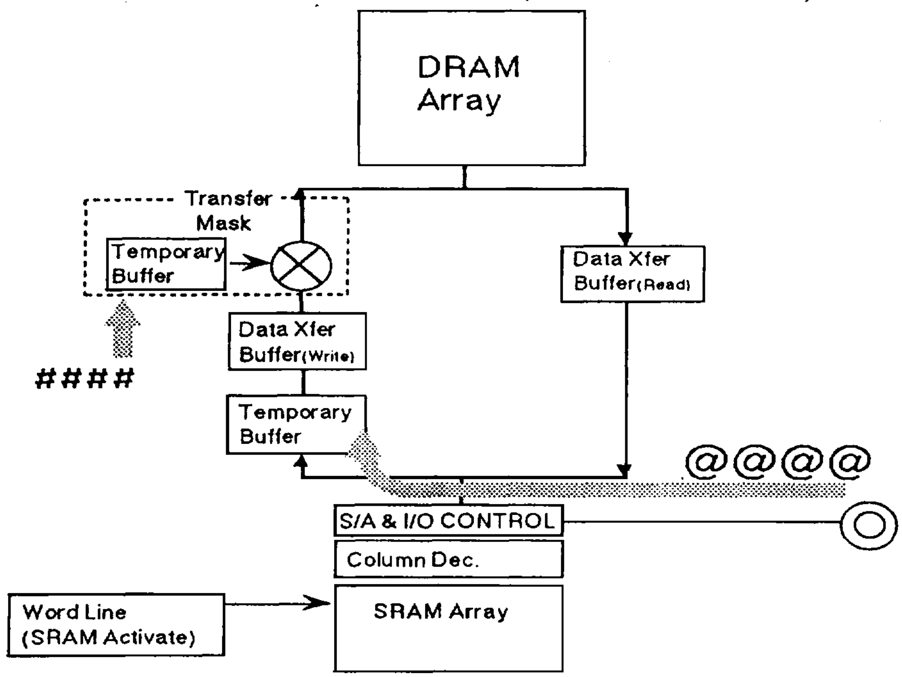



Each DTBW has a temporary buffer in between DTBw and data lines to realize pipe-lined operation and /or independent operation of DWT cycle from SRAM operation.
DWT1 opens the gate of data path and mask data between the temporary buffer and DTBw at the first DWT1 cycle and shut it before the second cycle begins.
After the second cycle of DWT1, new data can be written into the temporary buffer for the next DRAM Write Transfer cycle.
DWT2 does not open the gate of the data and mask. And it keeps the previous data and mask to fill DRAM with the same data , which is useful for graphic application.
DWT has options of DWT1R and DWT2R for cashe application. New block data of DRAM are transferred to DTBR simultaneously in those cycles.

# Buffer Write and DRAM Write Transfer cycle

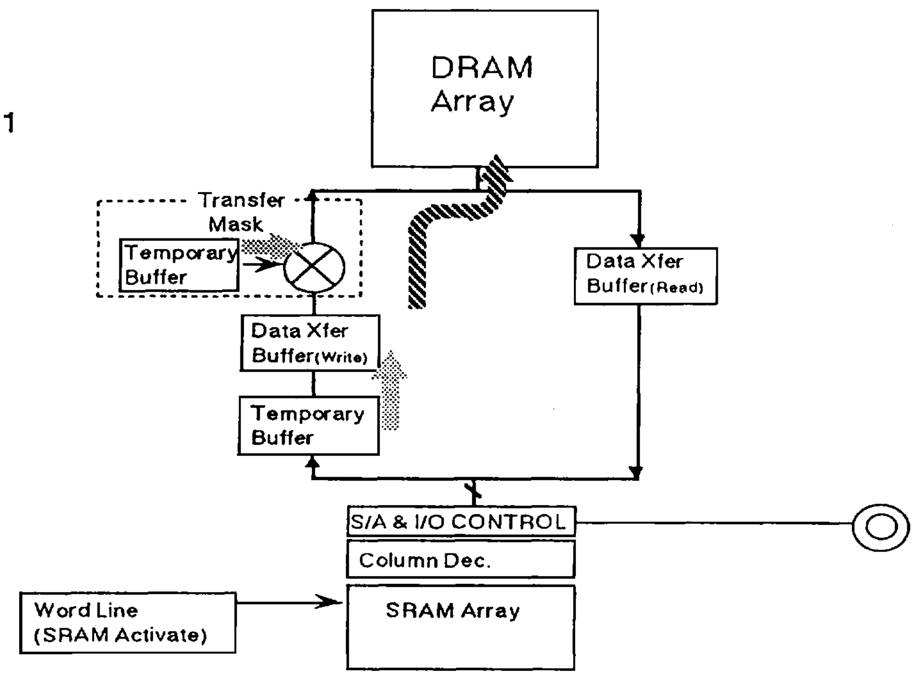
Buffer Write

When Buffer Write cycle is initiated, data of DQ pins is written to one of the selected temporary buffer(as indicated @@@@) and mask data of the selected bit is set(as indicated ####).



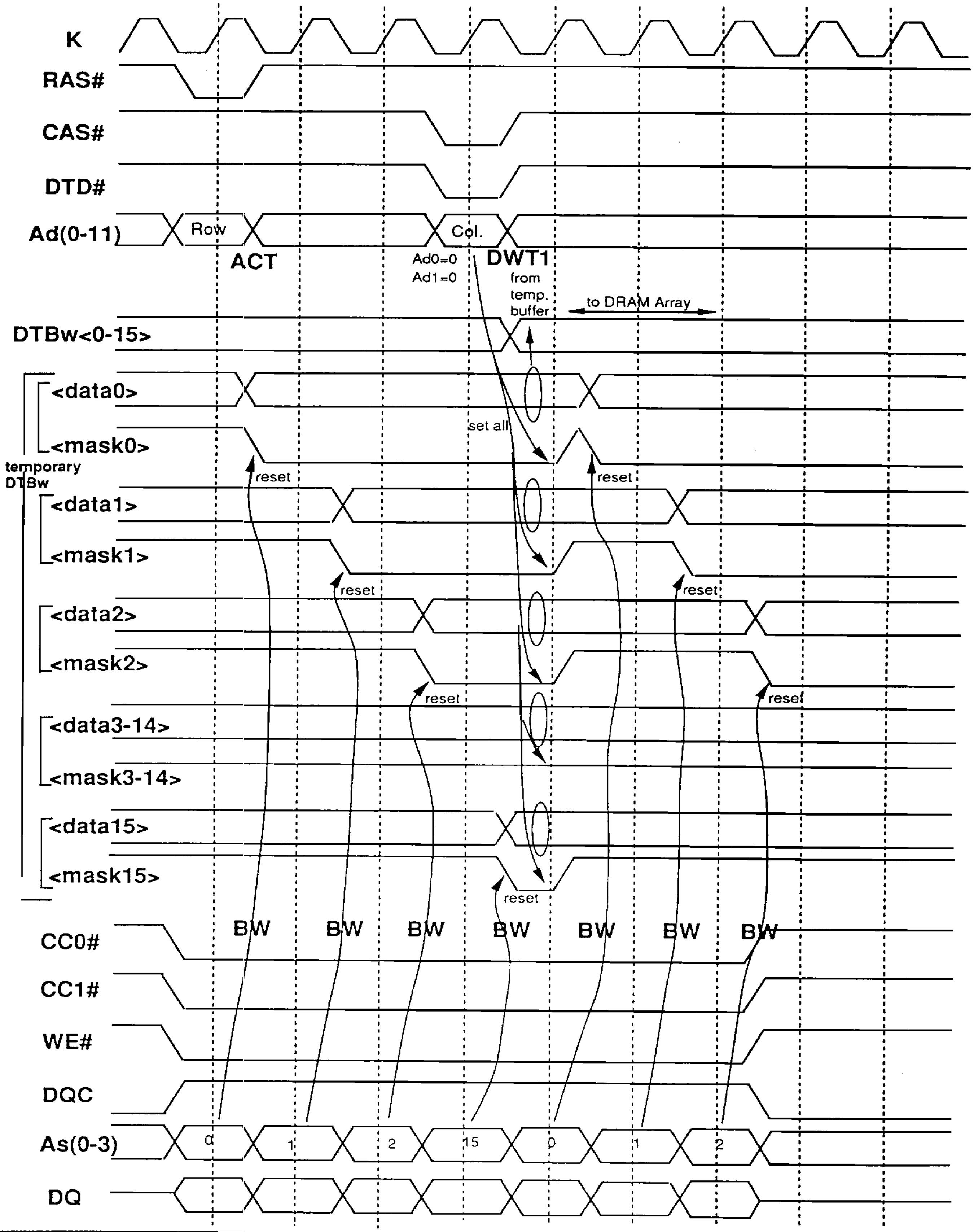

DRAM Write Transfer1

When DRAM Write Transfer cycle1 is initiated, data of temporary buffer is transferred to data Xfer Buffer<write> and mask data of temporary buffer is transferred to mask register at the first cycle of DWT1 .
Temporary masks are all set at this first cycle and new Buffer Write cycle of SRAM part can be set from the second cycle of DWT1.



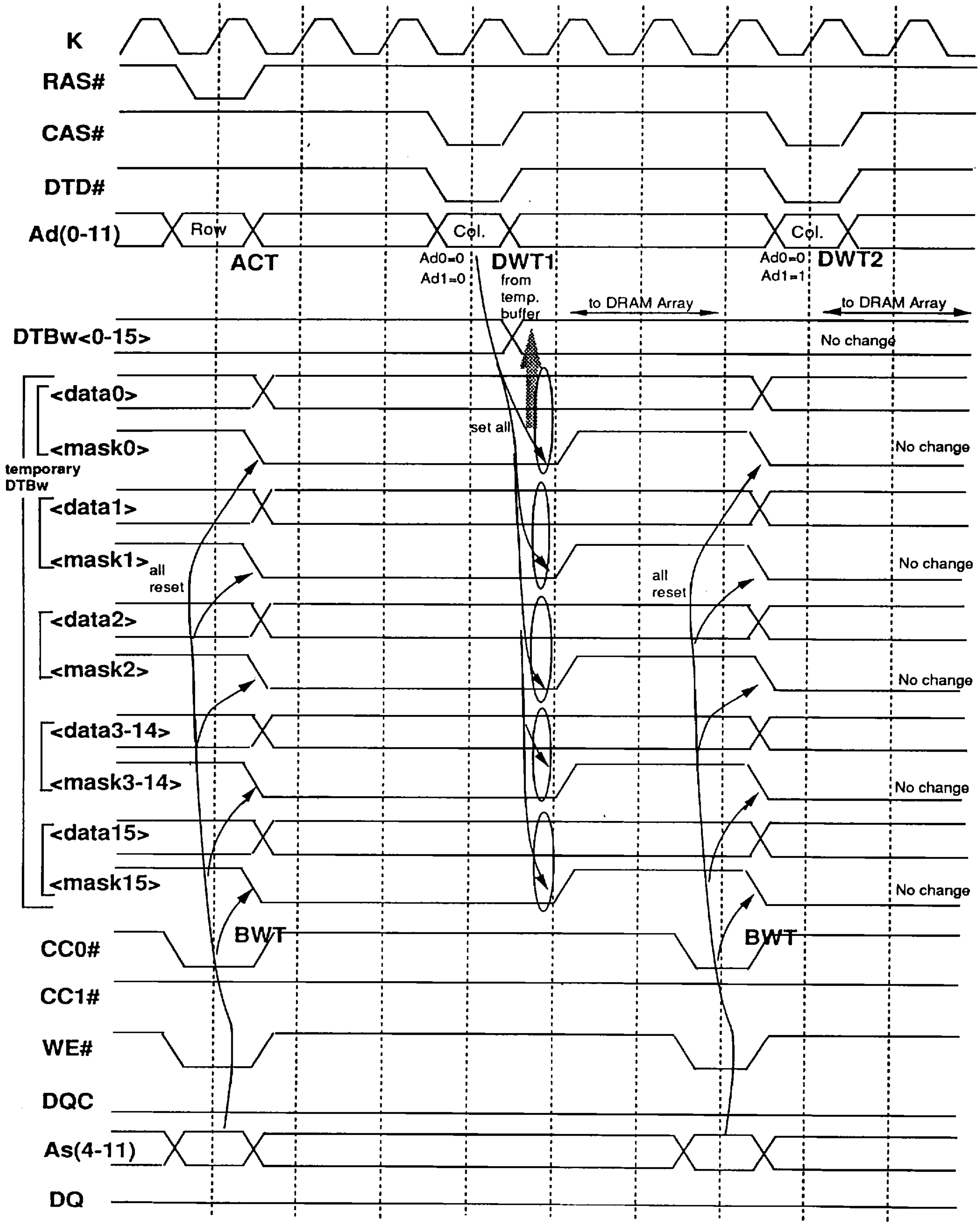

Then masked data is transferred to DRAM Array during the latency cycles.

## Mask Set and Reset — BW&DWT1

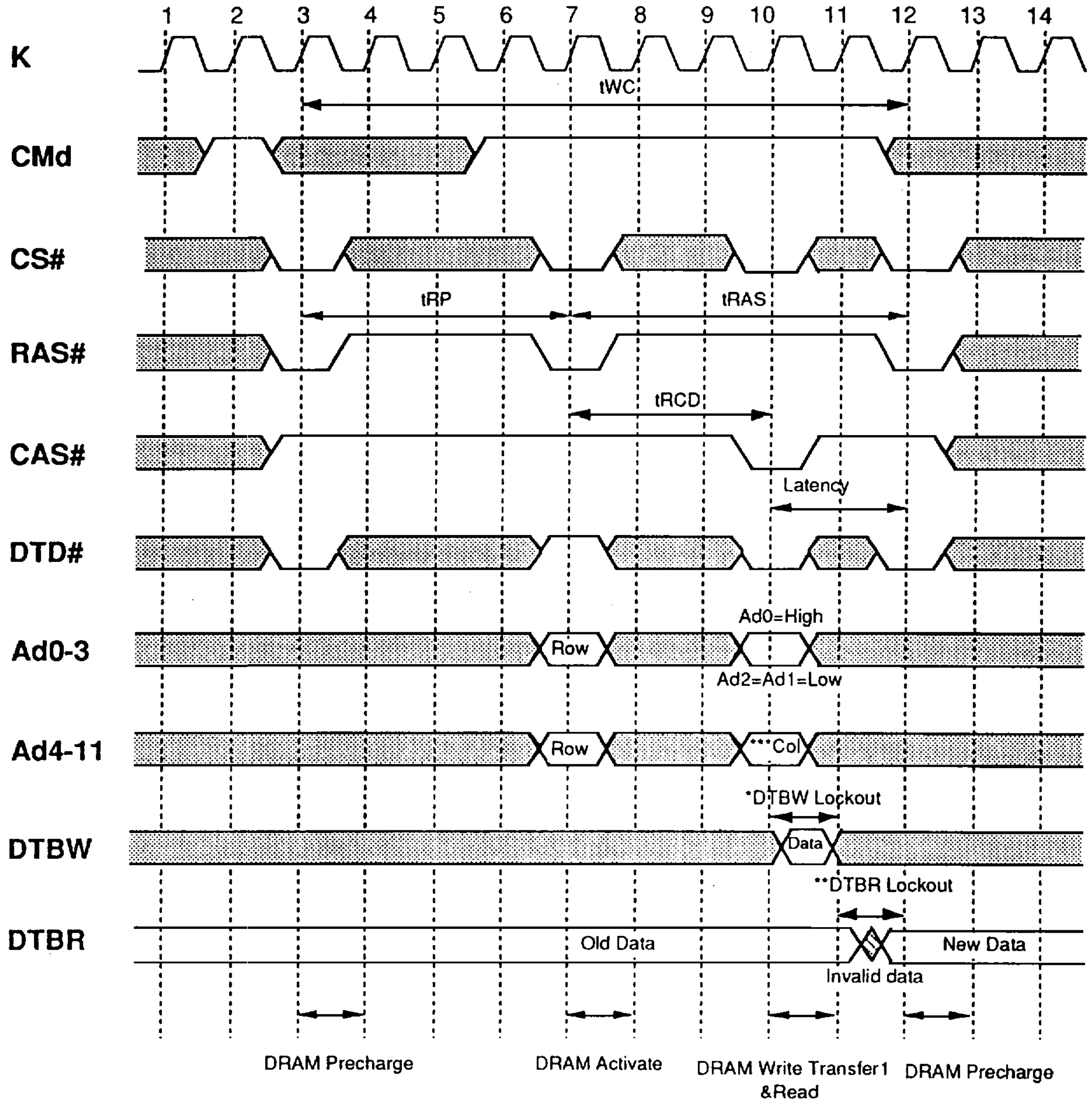


## Mask Set and Reset

BW&DWT1,SWT2



## DRAM Write Transfer 1 & Read




CMs#
CC0#
CC1#
WE#
DQC
G#
As0-11
M0-3
DQ0-3

* DTBW Lockout : Any buffer write operations during the occurrence of the first cycle of DWT1&R are prohibited .

** DTBR Lockout : Any buffer read operations during (N-1)th clock cycle of DWT1&R are prohibited in the case of Nth latency.

***Ad3-Ad7 are column block addresses and Ad8=Ad9=Low

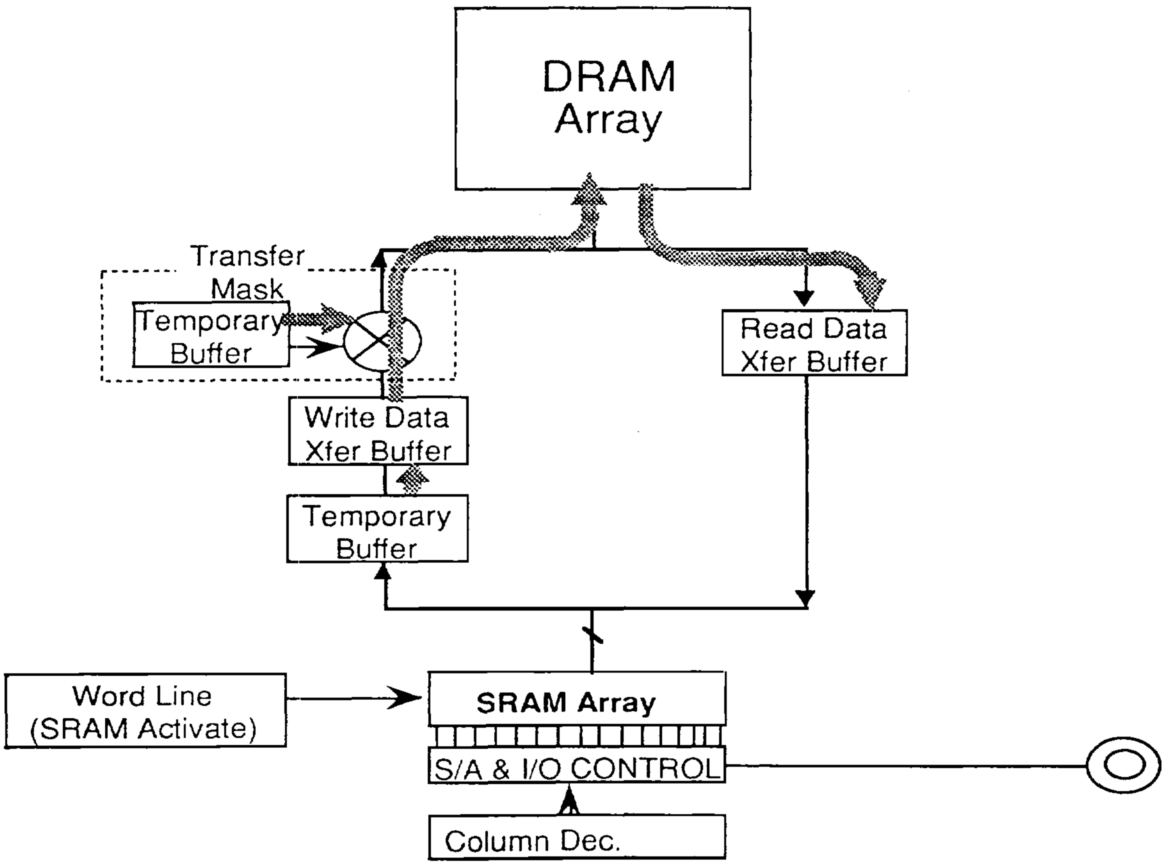
SRAM operation can be freely performed.

# DRAM Write Transfer 1 & Read

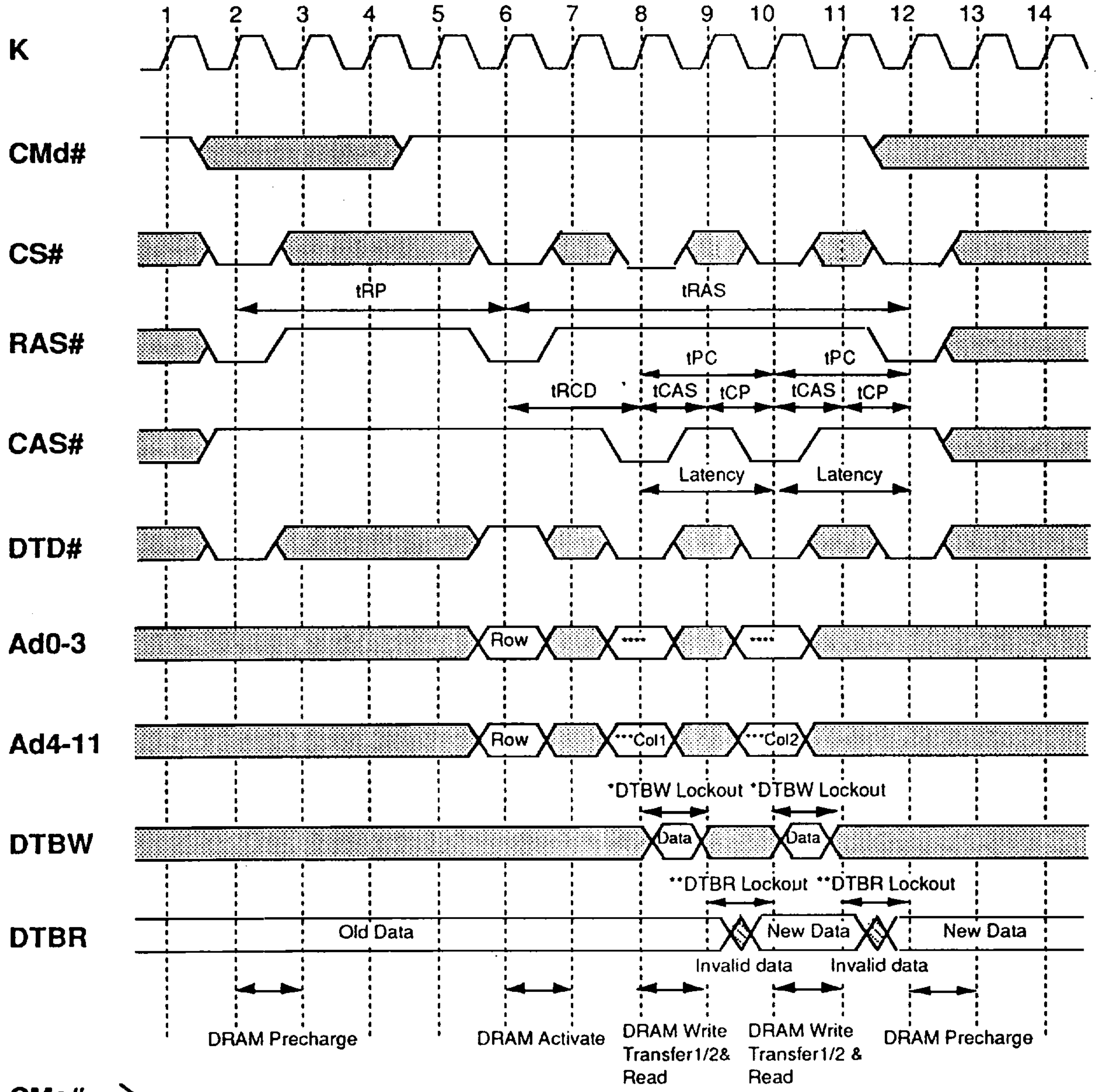
**DRAM Precharge** If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle.

**DRAM Activate** If CMd#=High at the rising edge of K, and CS#=RAS#=Low and CAS#=DTD#=High at the rising edge of K of the following cycle, the DRAM enters active mode. Addresses are latched from the Ad0-Ad11 inputs by the same rising edge of K. Internally, a DRAM row is selected. A DRAM precharge cycle must separate all DRAM Activate cycles (when a new DRAM row is accessed).

**DRAM Write Transfer1& Read** **If CMd#=High at rising edge of K and CS#=CAS#=DTD#=Low and RAS#=High at the rising edge of K of the following cycle (following a DRAM Activated cycle), a DRAM Write Transfer1&Read (DWT1&R) is performed. A Block (16 X 4 Bits) of Data is transferred from the DTBW to the DRAM as specified by Addresses Ad4-Ad11(Latched @ CAS#=Low, K= rising edge time). Addresses Ad1-Ad3 and Ad10-Ad11 must be set to Low while Ad0=High. During DWT1&R cycle data of Temporary Buffer are transferred to Write Data Xfer Buffer(DTBW) and masked data of Temporary Buffer are loaded to the Transfer Mask and finally all the masked data are transferred to DRAM Array at the same time a new block of data from DRAM Array is also transferred to Read Data Transfer Buffer (DTBR). The data path are opened during DWT1&R cycle and are closed before the next cycle begins.**



## DRAM Write Transfer1/2 & Read(Page Mode)




CMs#
CC0#
CC1#
WE#
DQC
G#
As0-11
M0-3
DQ0-3

SRAM operation can be freely performed.

* DTBW Lockout : Any buffer write operations during the occurrence of the first cycle of DWT1&R are prohibited .

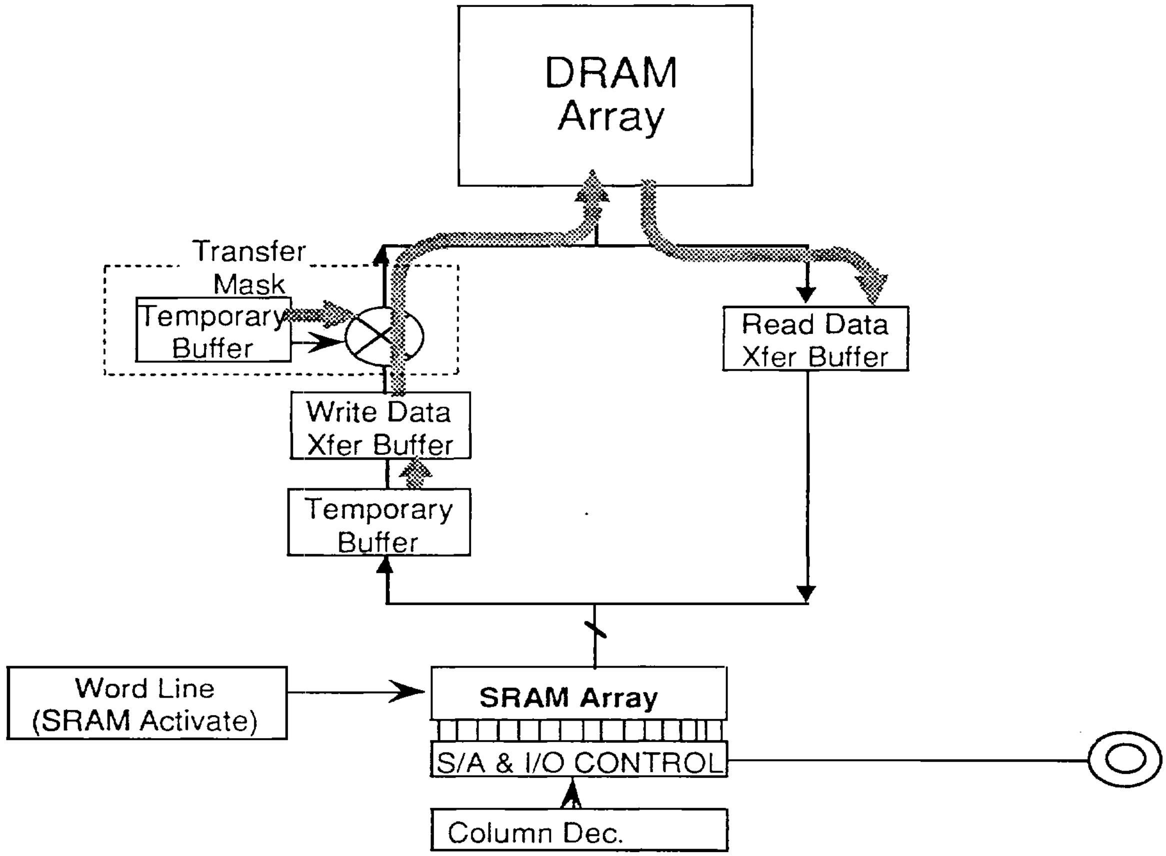
** DTBR Lockout : Any buffer read operations during (N-1)th clock cycle of DWT1&R are prohibited in the case of Nth latency.

*** Ad3-Ad7 are column block addresses and Ad8=Ad9=Low .

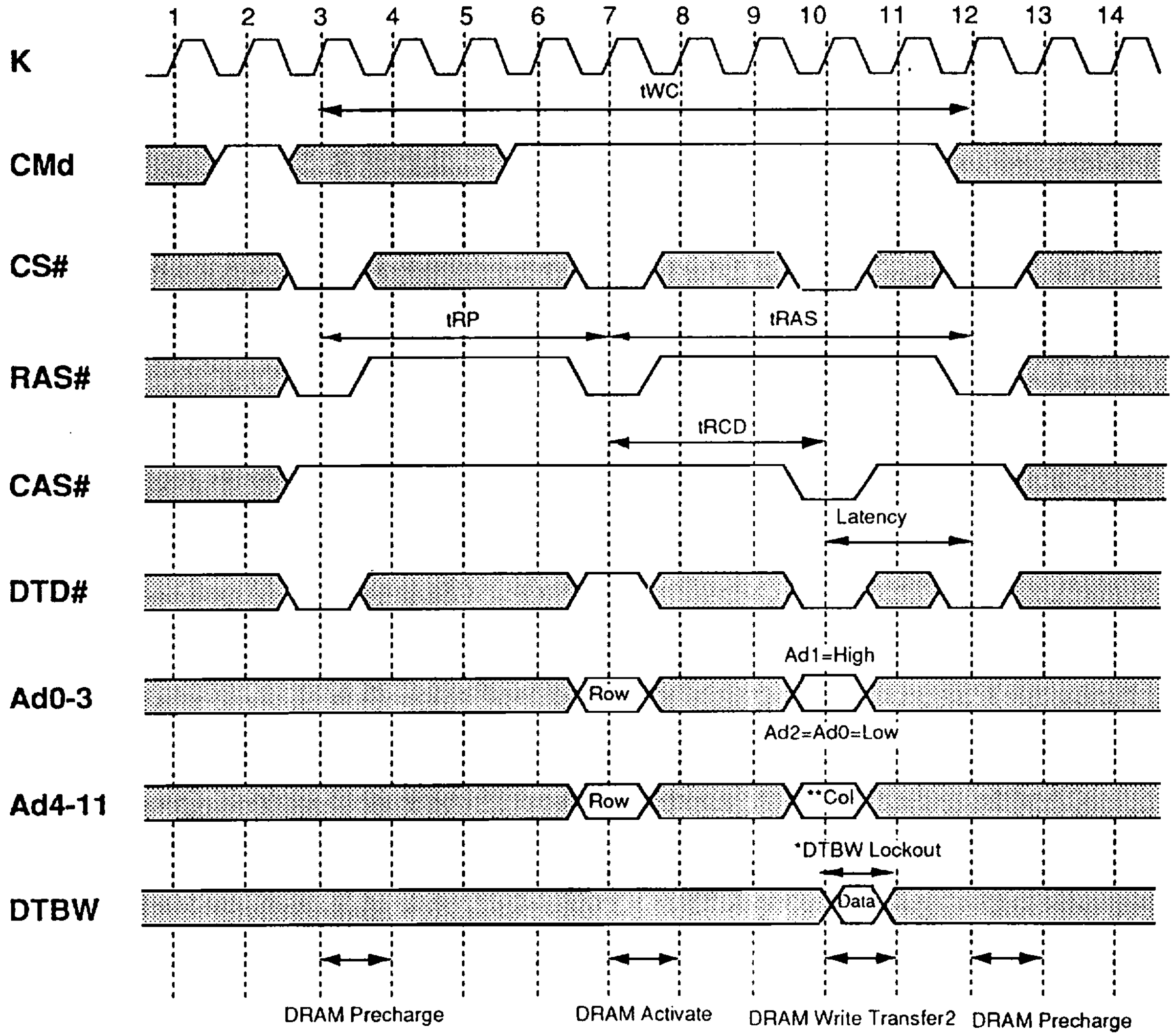
****Ad0-Ad2 must be set according to the truth table.

# DRAM Write Transfer 1 & Read

| | |
|---|---|
| DRAM Precharge | If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle. |
| DRAM Activate | If CMd#=High at the rising edge of K, and CS#=RAS#=Low and CAS#=DTD#=High at the rising edge of K of the following cycle, the DRAM enters active mode. Addresses are latched from the Ad0-Ad11 inputs by the same rising edge of K. Internally, a DRAM row is selected. A DRAM precharge cycle must separate all DRAM Activate cycles (when a new DRAM row is accessed). |
| **DRAM Write Transfer1& Read** | **If CMd#=High at rising edge of K and CS#=CAS#=DTD#=Low and RAS#=High at the rising edge of K of the following cycle (following a DRAM Activated cycle), a DRAM Write Transfer1&Read (DWT1&R) is performed. A Block (16 X 4 Bits) of Data is transferred from the DTBW to the DRAM as specified by Addresses Ad4-Ad11(Latched @ CAS#=Low, K= rising edge time). Addresses Ad1-Ad3 and Ad10-Ad11 must be set to Low while Ad0=High. During DWT1&R cycle data of Temporary Buffer are transferred to Write Data Xfer Buffer(DTBW) and masked data of Temporary Buffer are loaded to the Transfer Mask and finally all the masked data are transferred to DRAM Array at the same time a new block of data from DRAM Array is also transferred to Read Data Transfer Buffer (DTBR). The data path are opened during DWT1&R cycle and are closed before the next cycle begins.** |



## DRAM Write Transfer 2




* DTBW Lockout : Any buffer write operations during occurrence of the first cycle of DWT2 are prohibited.

** Ad3-Ad7 are column block addresses (Ad8=Ad9=Low)

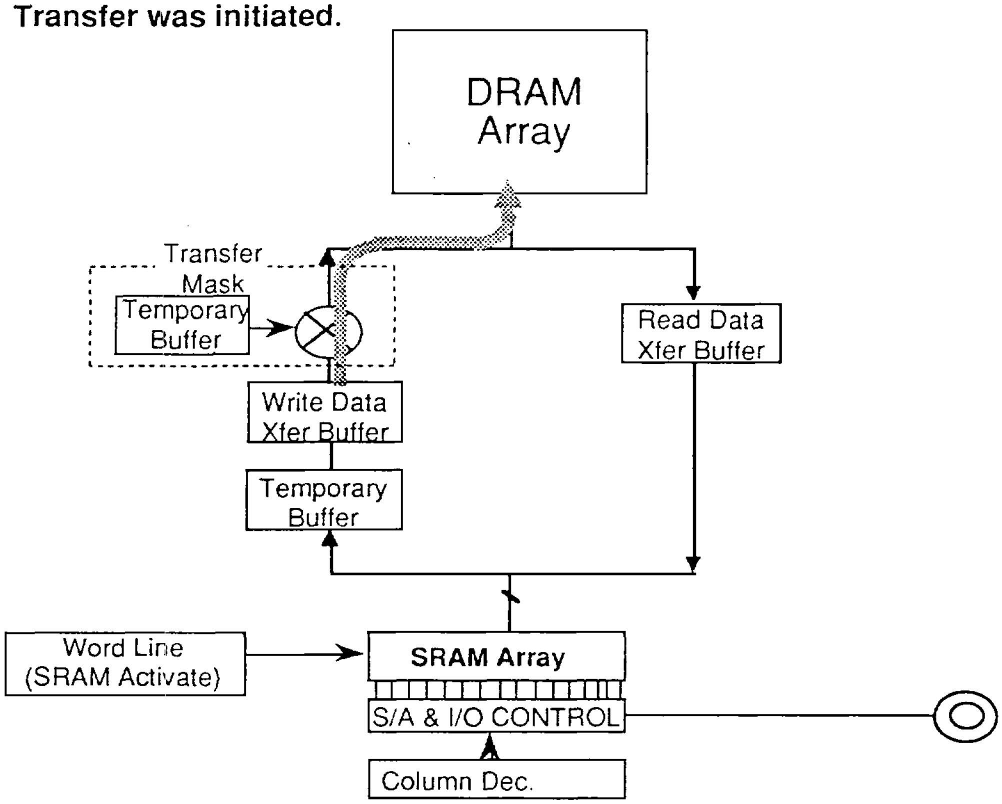
SRAM operation can be freely performed.

# DRAM Write Transfer 2

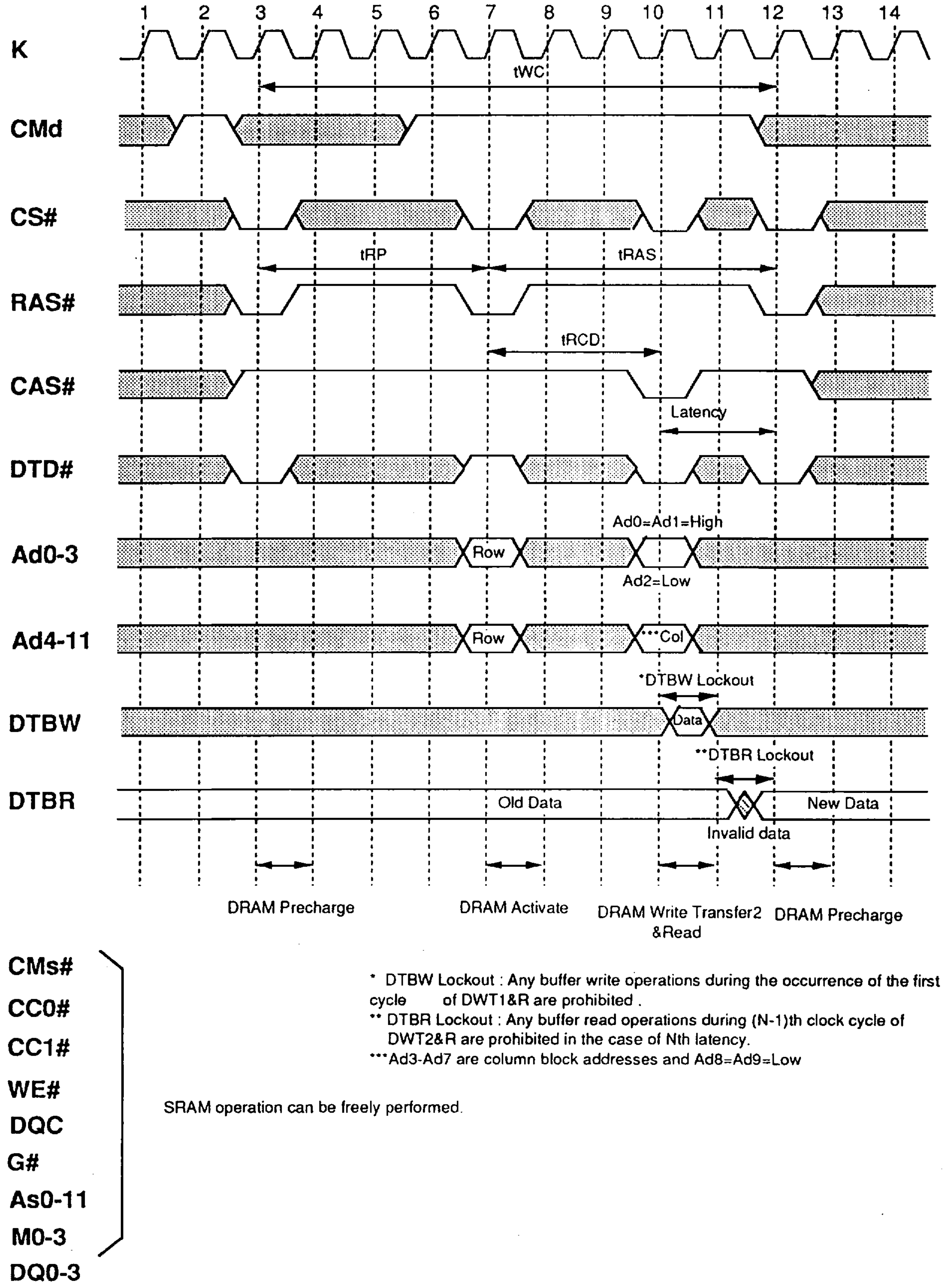
**DRAM Precharge**
If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle.

**DRAM Activate**
If CMd#=High at the rising edge of K, and CS#=RAS#=Low and CAS#=DTD#=High at the rising edge of K of the following cycle, the DRAM enters active mode. Addresses are latched from the Ad0-Ad9 inputs by the same rising edge of K. Internally, a DRAM row is selected. A DRAM precharge cycle must separate all DRAM Activate cycles (when a new DRAM row is accessed).

**DRAM Write Transfer2**
**If CMd#=High at rising edge of K and CS#=CAS#=DTD#=Low and RAS#=High at the rising edge of K of the following cycle (following a DRAM Activated cycle), a DRAM Write Transfer2(DWT2) is performed. A Block (16 X 4 Bits) of Data is transferred from the Write Data Transfer Buffer (DTBW) to the DRAM as specified by Addresses Ad4-Ad9(Latched @ CAS#=Low, K= rising edge time). Addresses Ad0, Ad2,Ad3 and Ad10-Ad11must be set to Low while Ad1=High. During DWT2 cycle no new data are transferred between Temporary Buffer and DTBW so that , the old data are transferred to DRAM Array without Mask Register set and no other operations involving the DTBW are allowed during the single master clock cycle in which the Write Transfer was initiated.**



## DRAM Write Transfer 2 & Read




* DTBW Lockout : Any buffer write operations during the occurrence of the first cycle of DWT1&R are prohibited .
** DTBR Lockout : Any buffer read operations during (N-1)th clock cycle of DWT2&R are prohibited in the case of Nth latency.
***Ad3-Ad7 are column block addresses and Ad8=Ad9=Low

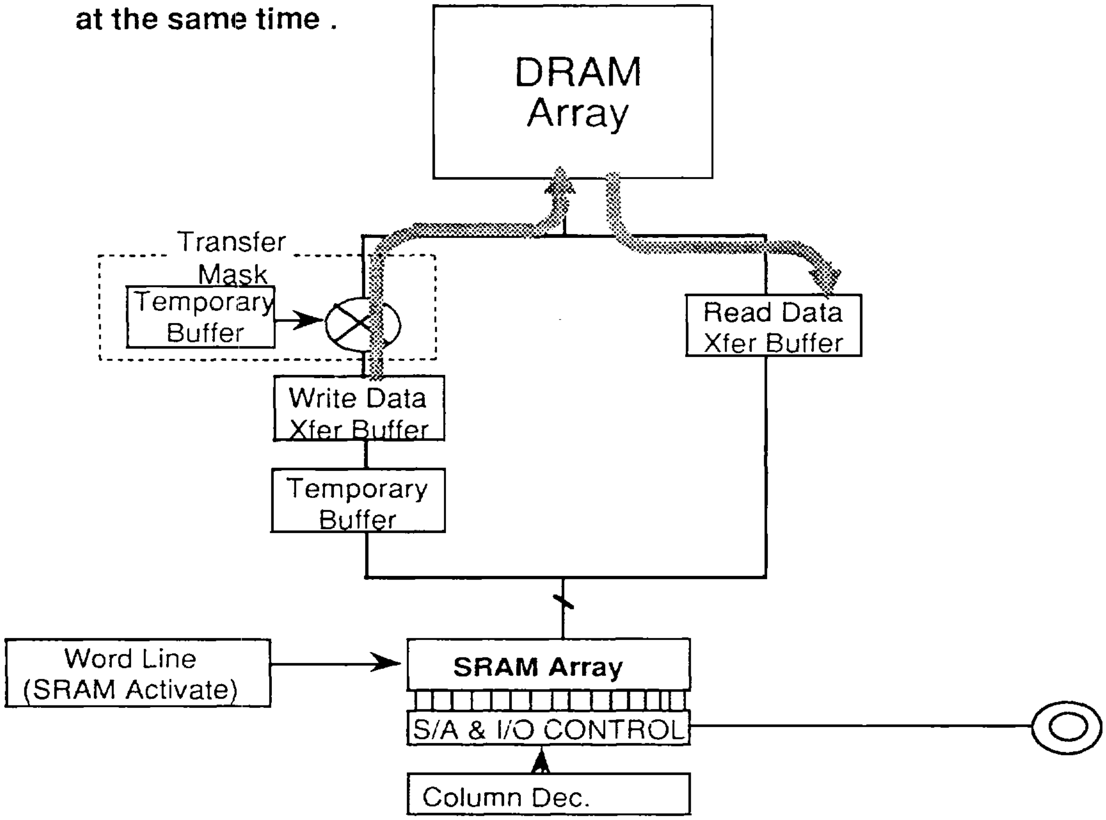
SRAM operation can be freely performed.

# DRAM Write Transfer 2 & Read

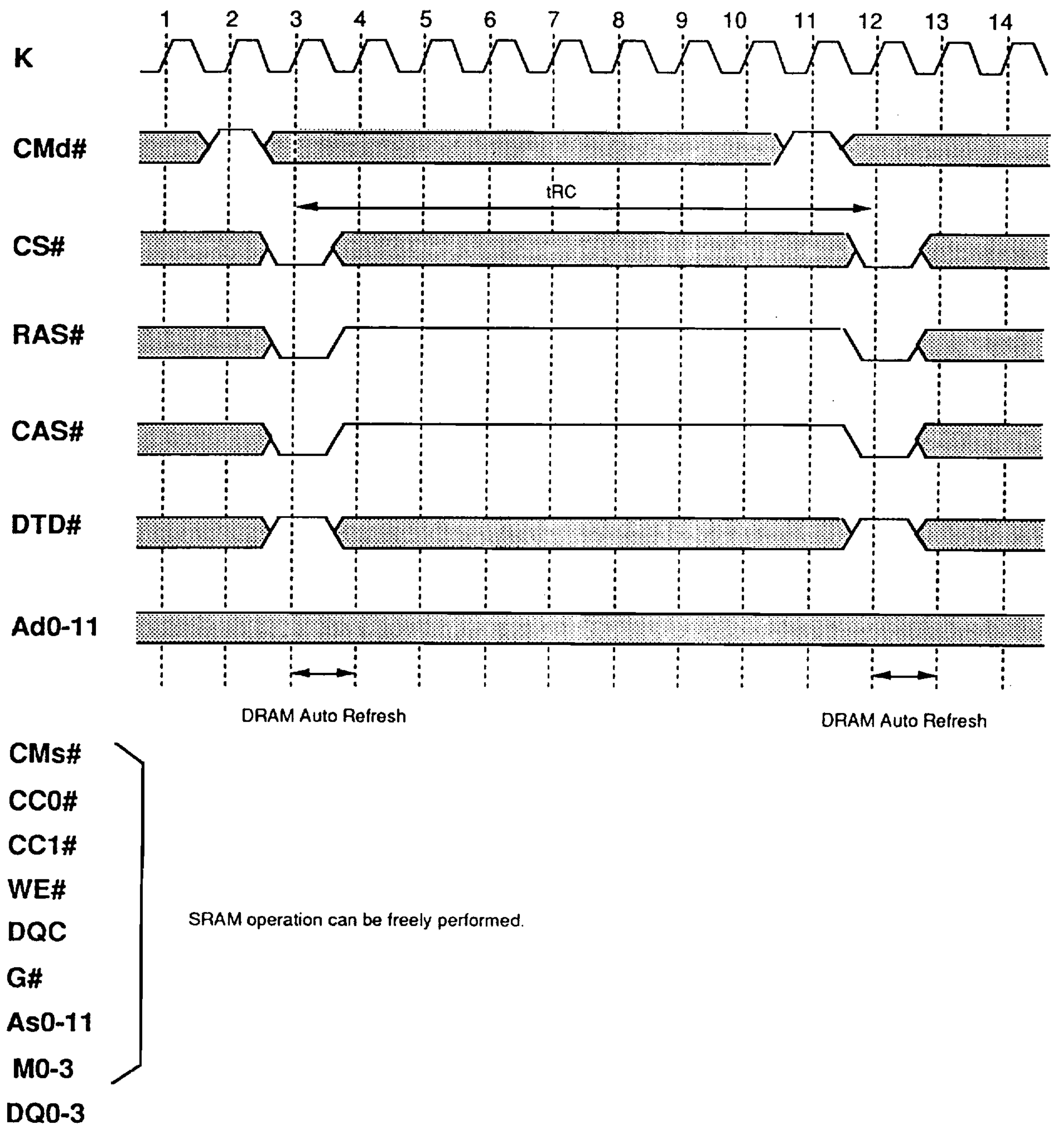
**DRAM Precharge** If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle.

**DRAM Activate** If CMd#=High at the rising edge of K, and CS#=RAS#=Low and CAS#=DTD#=High at the rising edge of K of the following cycle, the DRAM enters active mode. Addresses are latched from the Ad0-Ad9 inputs by the same rising edge of K. Internally, a DRAM row is selected. A DRAM precharge cycle must separate all DRAM Activate cycles (when a new DRAM row is accessed).

**DRAM Write Transfer2& Read** **If CMd#=High at rising edge of K and CS#=CAS#=DTD#=Low and RAS#=High at the rising edge of K of the following cycle (following a DRAM Activated cycle), a DRAM Write Transfer2 & Read(DWT2&R) is performed. A Block (16X 4Bits) of Data is transferred from the Write Data Transfer Buffer (DTBW) to the DRAM as specified by Addresses Ad4-Ad9(Latched @ CAS#=Low, K= rising edge time). Addresses Ad0-Ad1 is set to High and Ad2,Ad3,Ad10-Ad11 must be set to Low. During DWT2&R cycle no new data are transferred between Temporary Buffer and DTBW so that , the old data are transferred to DRAM Array without Mask Register set and no other operations involving the DTBW are allowed during the single master clock cycle in which the Write Transfer was initiated. A new block of data is also transferred to DTBR at the same time .**



## DRAM Auto Refresh



# DRAM Auto Refresh

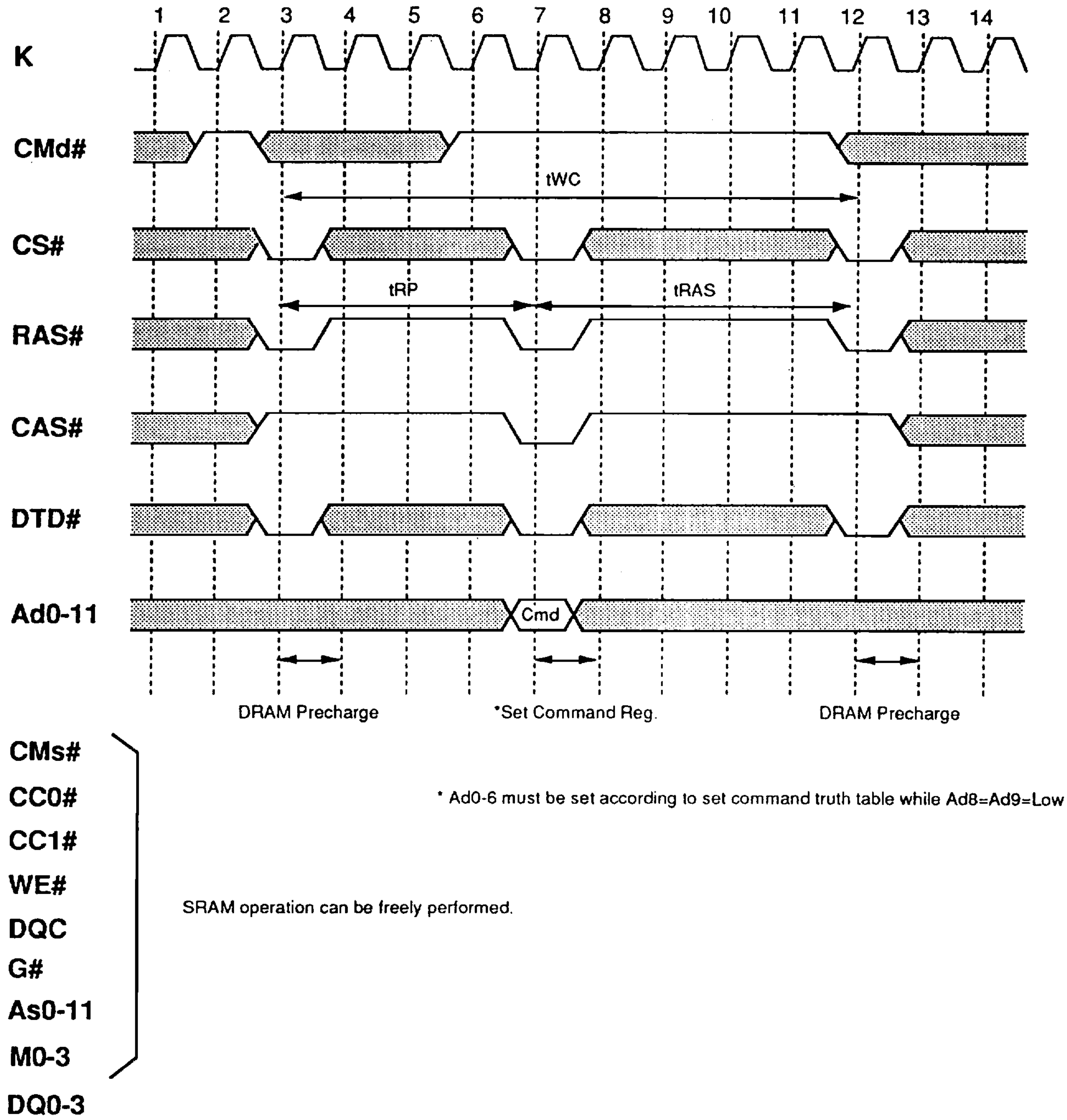
**DRAM Auto-Refresh**

**If CMd#=High at the rising edge of K, and CS#=RAS#=CAS#=Low and DTD#=High at the rising edge of K of the following cycle, the DRAM enters Auto-Refresh Mode. Internally, a row is selected and refreshed. The Auto refresh cycle must be followed by a DRAM precharge cycle before another DRAM Activate cycle can take place. The mode is similar to a CAS-Before-RAS (CBR) mode in standard DRAMs.**

DRAM Precharge

If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle.

## Set Command Register



# Set Command Register

**DRAM Precharge**

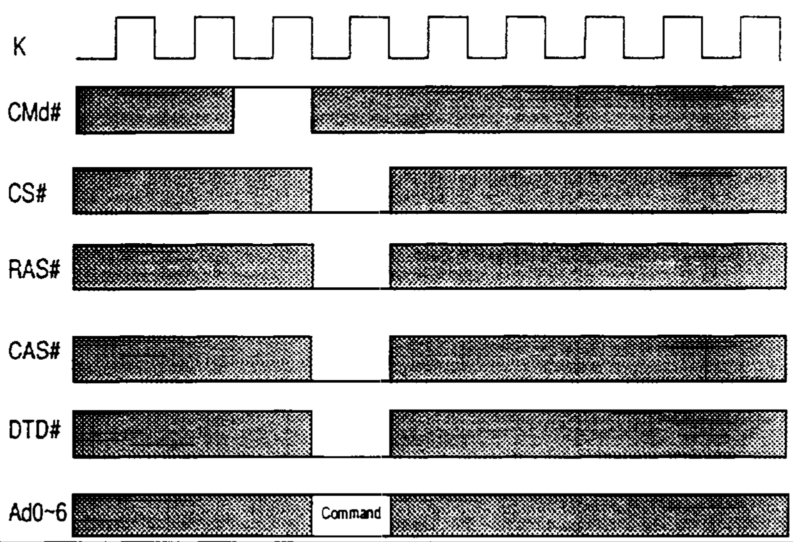
If CMd#=High at the rising edge of K, and CS#=RAS#=DTD#=Low and CAS#=High at the rising edge of K of the following cycle, the DRAM enters precharge mode. Internally, the active row is deselected (completing the refresh process), page-mode is disabled, and the DRAM prepares for another DRAM Activate cycle.

**Set Command Register**

**If CMd#=High at the rising edge of K, and CS#=RAS#=CAS#=DTD#=Low at the rising edge of K of the following cycle, the DRAM enters Set Command Register mode. The address present on the Ad0-Ad6 pins determines the DRAM Read/Write Transfer Latency, the Output Mode (transparent / latched / registered), and Mask Register Mode (set / no operation). The unused addresses must be set to Low.**

## SET COMMAND REGISTER (SCR)
### Detailed Truth Table for SCR

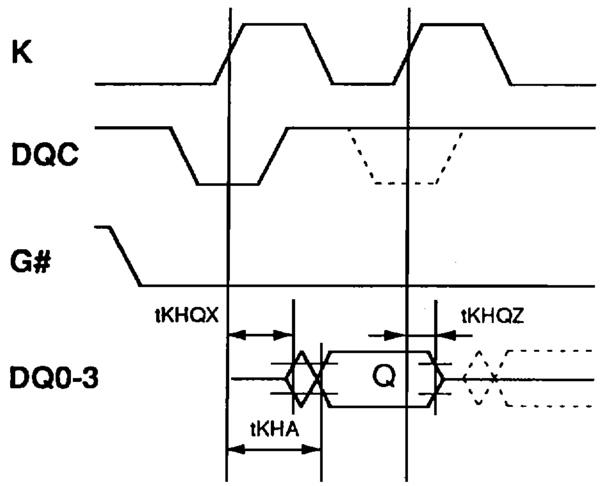
| Operation Code | | | * Latency | | | Output Mode | | Reserved | Set Mask Register | Command |
|---|---|---|---|---|---|---|---|---|---|---|
| Ad9 | Ad8 | Ad7 | Ad6 | Ad5 | Ad4 | Ad3 | Ad2 | Ad1 | Ad0 | |
| L | L | L | L | L | L | X | X | L | X | Latency 1 |
| L | L | L | L | L | H | X | X | L | X | 2 |
| L | L | L | L | H | L | X | X | L | X | 3 |
| L | L | L | L | H | H | X | X | L | X | 4 |
| L | L | L | X | X | X | L | L | L | X | Output Mode Transparent |
| L | L | L | X | X | X | L | H | L | X | Latched |
| L | L | L | X | X | X | H | L | L | X | Registered |
| L | L | L | X | X | X | X | X | L | L | No Operation of Mask |
| L | L | L | X | X | X | X | X | L | H | Set All Masks |

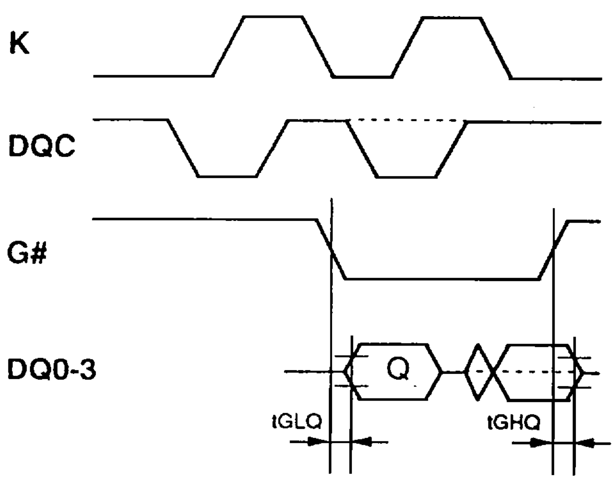



* Latency is the number of the clock cycle take the new data is transferred from DTBR to SRAM and/or DQ pins. Therefore, it can be adjusted to the clock frequency of the system.

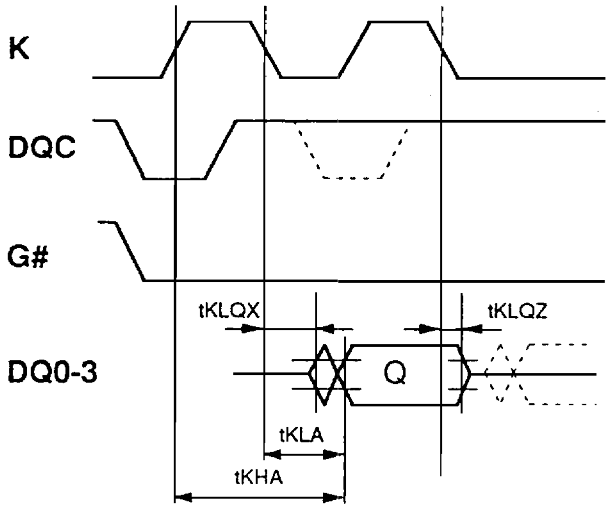
## Output Operations

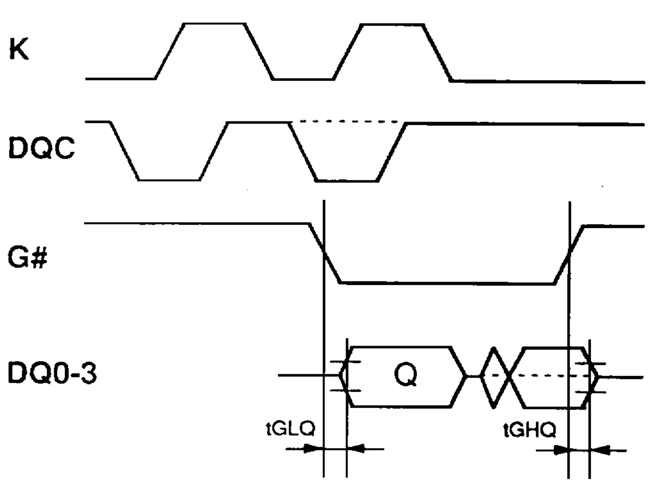
### Transparent



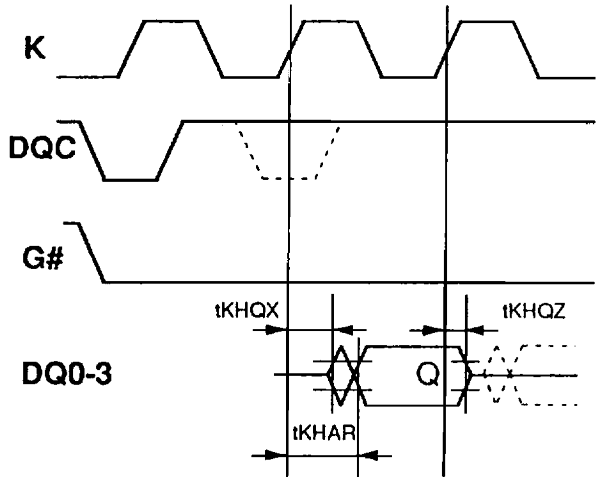



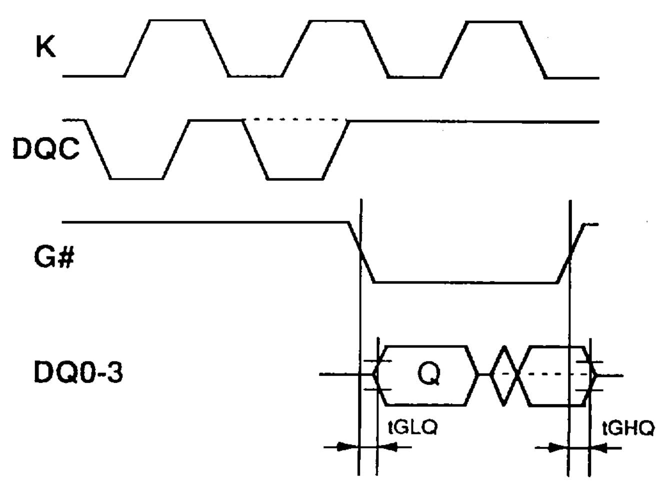
**Latched**

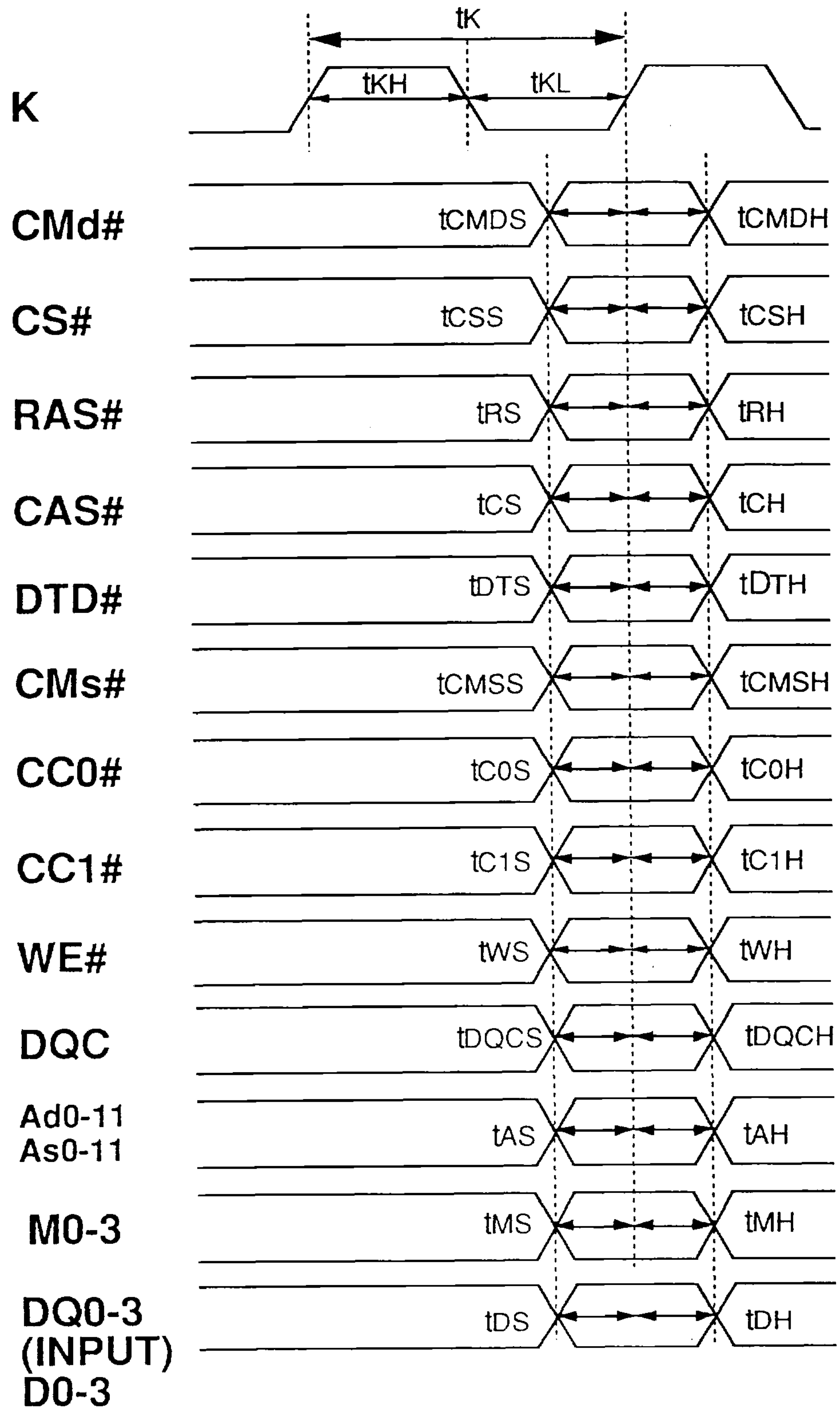


**Registered**




tK
tKH
tKL
K
CMd#
tCMDS
tCMDH
CS#
tCSS
tCSH
RAS#
tRS
tRH
CAS#
tCS
tCH
DTD#
tDTS
tDTH
CMs#
tCMSS
tCMSH
CC0#
tC0S
tC0H
CC1#
tC1S
tC1H
WE#
tWS
tWH
DQC
tDQCS
tDQCH
Ad0-11
As0-11
tAS
tAH
M0-3
tMS
tMH
DQ0-3
(INPUT)
D0-3
tDS
tDH

## ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Vcc | Supply Voltage | With respect to Vss | -0.5 ~ 4.6 | V |
| VI | Input Voltage | | -0.5 ~ 4.6 | V |
| VO | Output Voltage | | -0.5 ~ 4.6 | V |
| IO | Output Current | | 50 | mA |
| Pd | Power Dissipation | | 1000 | mW |
| Topr | Operating Temperature | | 0 ~ 70 | ℃ |
| Tstg | Storage Temperature | | -65 ~ 150 | ℃ |
| | | | | |

## RECOMMENDED OPERATING CONDITIONS

(Ta=0~70℃, unless otherwise noted)

| Symbol | Parameter | Limits | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Vcc | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| Vss | Supply Voltage | 0 | 0 | 0 | V |
| VIH | High-level Input Voltage all inputs | 2.0 | | Vcc+0.3 | V |
| VIL | Low-level Input Voltage all inputs | -0.3 | | 0.8 | V |
| | | | | | |
| | | | | | |

## CAPACITANCE

(Ta=0~70℃, Vcc=3.3±0.3V, Vss=0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits (MAX) | Unit |
|---|---|---|---|---|
| CI(A) | Input Capacitance, Address pin | VI=Vss | 5 | pF |
| CI(C) | Input Capacitance, Clock pin | f=1MHz | 7 | pF |
| CI/O | Input Capacitance, I/O pin | VI=25mVrms | 7 | pF |

## AVERAGE SUPPLY CURRENT from Vcc

(Ta=0~70˚C, Vcc=VccQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

| Symbol | Condition | Limits (MAX) | | | | Unit |
|---|---|---|---|---|---|---|
| | output open | -8 | -10 | -12 | -15 | |
| IccAS | Average supply current of SRAM tK=min | | | | | |
| IccAD | Average supply current of DRAM tK=min | | | | | |
| IccSTN | LVTTL standby,tK=min,CMd#=CMs#=H | | | | | |
| IccSCN | CMOS standby,tK=min,CMd#=CMs#=H | | T.B.D. | | | |
| IccSX | standby,CMd#=CMs#=L | | | | | |
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**TIMING REQUIREMENTS -1** (CLK pulse, input signals setup / hold time to CLK edge)
(Ta=0~70˚C, Vcc=VccQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)
Input Pulse Levels: 0 to 3.0V
Input Timing Measurement Reference Level: 1.5V
Input Rise/Fall Time: 2ns

| Symbol | Parameter | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -8 | | -10 | | -12 | | -15 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| tK | Clock Cycle Time | 8 | 1000 | 10 | 1000 | 12 | 1000 | 15 | 1000 | ns |
| tKH | Clock High PulseWidth | 3 | | 4 | | 5 | | 6 | | ns |
| tKL | Clock Low PulseWidth | 3 | | 4 | | 5 | | 6 | | ns |
| tCMDS | Setup Time for CMd | 3 | | 3 | | 3 | | 3 | | ns |
| tCMDH | Hold Time for CMd | 2 | | 2 | | 2 | | 2 | | ns |
| tRS | Setup Time for RAS# | 3 | | 3 | | 3 | | 3 | | ns |
| tRH | Hold Time for RAS# | 2 | | 2 | | 2 | | 2 | | ns |
| tCS | Setup Time for CAS# | 3 | | 3 | | 3 | | 3 | | ns |
| tCH | Hold Time for CAS# | 2 | | 2 | | 2 | | 2 | | ns |
| tDTS | Setup Time for DTD# | 3 | | 3 | | 3 | | 3 | | ns |
| tDTH | Hold Time for DTD# | 2 | | 2 | | 2 | | 2 | | ns |
| tCMSS | Setup Time for CMs | 3 | | 3 | | 3 | | 3 | | ns |
| tCMSH | Hold Time for CMs | 2 | | 2 | | 2 | | 2 | | ns |
| tES | Setup Time for E# | 3 | | 3 | | 3 | | 3 | | ns |
| tEH | Hold Time for E# | 2 | | 2 | | 2 | | 2 | | ns |
| tWS | Setup Time for WE# | 3 | | 3 | | 3 | | 3 | | ns |
| tWH | Hold Time for WE# | 2 | | 2 | | 2 | | 2 | | ns |
| tC1S | Setup Time for CC1 | 3 | | 3 | | 3 | | 3 | | ns |
| tC1H | Hold Time for CC1 | 2 | | 2 | | 2 | | 2 | | ns |
| tC2S | Setup Time for CC2 | 3 | | 3 | | 3 | | 3 | | ns |
| tC2H | Hold Time for CC2 | 2 | | 2 | | 2 | | 2 | | ns |
| tAS | Setup Time for Address | 3 | | 3 | | 3 | | 3 | | ns |
| tAH | Hold Time for Address | 2 | | 2 | | 2 | | 2 | | ns |
| tMS | Setup Time for Mask | 3 | | 3 | | 3 | | 3 | | ns |
| tMH | Hold Time for Mask | 2 | | 2 | | 2 | | 2 | | ns |
| tDS | Setup Time for Din | 3 | | 3 | | 3 | | 3 | | ns |
| tDH | Hold Time for Din | 2 | | 2 | | 2 | | 2 | | ns |
| tCSS | Setup Time for CS# | 8 | | 8 | | 8 | | 8 | | ns |
| tCSH | Hold Time for CS# | 2 | | 2 | | 2 | | 3 | | ns |

# M5M4V16409ATP-8,-10,-12,-15

Oct 26,1992

**16MCDRAM:16M (4194304 - WORD BY 4 - BIT) Cache DRAM with 16k (4096-WORD BY4 -BIT) SRAM**

## TIMING REQUIREMENTS -2 (Read, Write, Refresh)

(Ta=0~70°C, Vcc=VccQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

Input Pulse Levels: 0 to 3.0V

Input Timing Measurement Reference Level: 1.5V

Input Rise/Fall Time: 2ns

| Symbol | Parameter | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | -8 | | -10 | | -12 | | -15 | | |
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| tRAC | | 60 | | 60 | | 70 | | 80 | | ns |
| tCAC | | 30 | | 30 | | 35 | | 40 | | ns |
| tREF | Refresh Cycle Time | | 64 | | 64 | | 64 | | 64 | ms |
| tRP | Precharge Time | 40 | | 40 | | 50 | | 60 | | ns |
| tRCD | Delay Time, Add Strb. Row to Col. | 20 | | 20 | | 25 | | 30 | | ns |
| tCCD | Delay Time, Add Strb. Col. to Col. | 20 | | 20 | | 25 | | 30 | | ns |
| tRC | Read Transfer Cycle Time | 100 | | 100 | | 120 | | 140 | | ns |
| tWC | Write Transfer Cycle Time | 100 | | 100 | | 120 | | 140 | | ns |
| tPC | Page Cycle Time | 20 | | 20 | | 25 | | 30 | | ns |
| tRAS | Active Time | 60 | 200000 | 60 | 200000 | 70 | 200000 | 80 | 200000 | ns |
| tWRP | Write to Precharge Recovery Time | 20 | | 20 | | 25 | | 30 | | ns |
| tWRR | Write to Read Recovery Time | 20 | | 20 | | 25 | | 30 | | ns |
| | | | | | | | | | | |
| | | | | | | | | | | |

**TIMING PARAMETER - CLK TABLE**

| Version | -8 | | -10 | | -12 | | -15 | |
|---|---|---|---|---|---|---|---|---|
| Freq. | 125 | 80 | 100 | 66.6 | 80 | 50 | 66.6 | 33.3 |
| (MHz) | Min Max | Min Max | Min Max | Min Max | MinMax | Min Max | Min Max | Min Max |
| tREF | 8.0M | 5.1M | 6.4M | 4.26M | 5.12M | 3.2M | 4.26M | 2.1M |
| tRP | 5 | 4 | 4 | 4 | 4 | 3 | 4 | 2 |
| tRCD | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 1 |
| tCCD | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 1 |
| tRC | 13 | 9 | 10 | 7 | 10 | 6 | 10 | 5 |
| tWC | 13 | 9 | 10 | 7 | 10 | 6 | 10 | 5 |
| tPC | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 1 |
| tRAS | 8 25000 | 5 16000 | 6 20000 | 4 13333 | 616000 | 4 10000 | 6 13333 | 3 6666 |
| tWRP | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 1 |
| tWRR | 3 | 2 | 2 | 2 | 2 | 2 | 2 | 1 |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |
| | | | | | | | | |

Number of CLK can be calculated as integeε(timing parameter / tCLK) in any clock frequency.

## SWITCHING CHARACTERISTICS

(Ta=0~70°C, Vcc=VccQ=3.3±0.3V, Vss=VssQ=0V, unless otherwise noted)

| Symbol | Parameter | Limits | | | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | -10 | | -12 | | -15 | | | |
| | | Min | Max | Min | Max | Min | Max | | | |
| tRAC | Access Time from /RAS | | 60 | | 60 | | 70 | | 80 | ns |
| tCAC | Access Time from /CAS | | 30 | | 30 | | 35 | | 40 | ns |
| tKHA | Access Time from CLK 'H' Edge | | 8 | | 6 | | 7 | | 8 | ns |
| tKHQX | Output Active from CLK 'H' Edge | 2 | | 2 | | 2 | | 2 | | ns |
| tKHQZ | Output Disable from CLK 'H' Edge | 2 | 4 | 2 | 5 | 2 | 6 | 2 | 7 | ns |
| tKLA | Access Time from CLK 'L' Edge | | 6 | | 8 | | 10 | | 12 | ns |
| tKLQX | Output Active from CLK 'L' Edge | 2 | | 2 | | 2 | | 2 | | ns |
| tKLQZ | Output Disable from CLK 'L' Edge | 2 | 4 | 2 | 5 | 2 | 6 | 2 | 7 | ns |
| tKHAR | Access Time from CLK 'H' Edge | | 6 | | 8 | | 10 | | 12 | ns |
| tGLQ | Access Time from G# 'L' Edge | | 6 | | 8 | | 10 | | 12 | ns |
| tGHQ | Output Disable from G# 'H' Edge | 2 | 4 | 2 | 5 | 2 | 6 | 2 | 7 | ns |

Note1: tKHZ defines the time at which the output achieves the low impedance state (Iout>10uA).
2: tOFF defines the time at which the output achieves the high impedance state (Iout≦10uA).

Access Latency Minimum

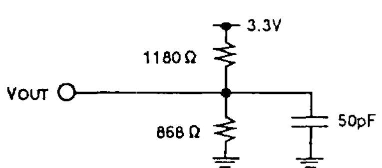
| Freq.(MHz) | | 125 | 100 | 80 | 66.6 | 54 | 50 | 33.3 | 27 |
|---|---|---|---|---|---|---|---|---|---|
| -8 | tRAC | 7 | 6 | 5 | 4 | 4 | 3 | 2 | 2 |
| | tCAC | 4 | 3 | 2 | 2 | 2 | 2 | 1 | 1 |
| -10 | tRAC | 6 | 5 | 4 | 4 | 3 | 3 | 2 | 2 |
| | tCAC | 3 | 3 | 2 | 2 | 2 | 2 | 1 | 1 |
| -12 | tRAC | - | 6 | 5 | 4 | 4 | 3 | 3 | 2 |
| | tCAC | - | 4 | 3 | 2 | 2 | 2 | 2 | 1 |
| -15 | tRAC | - | - | 6 | 5 | 4 | 4 | 3 | 3 |
| | tCAC | - | - | 3 | 3 | 2 | 2 | 2 | 2 |

## AC OPERATING CONDITIONS AND CHARACTERISTICS

(Ta=0~70°C, Vcc=VccQ=3.3±0.3V, Vss=0V, unless otherwise noted)

| Symbol | Parameter | Test Condition | Limits | | Unit |
|---|---|---|---|---|---|
| | | | Min | Max | |
| VOH(DC)* | High-level Output Voltage (DC) | IOH=-2mA | 2.4 | - | V |
| VOL(DC)* | Low-level Output Voltage (DC) | IOL= 2mA | - | 0.4 | V |
| VOH(AC)* | High-level Output Voltage (AC) | CL=50pF, IOH=-2mA | 2.0 | - | V |
| VOL(AC)* | Low-level Output Voltage (AC) | CL=50pF, IOL= 2mA | - | 0.8 | V |
| IOZ | Off-state Output Current | Q floating VO=0~VccQ | -10 | 10 | uA |
| II | Input Current | VIH=0~Vcc+0.3V | -10 | 10 | uA |

* VOH(AC) and VOL(AC) are the reference level for AC measurement.
VOH(DC) and VOL(DC) are the final level the output reaches.



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