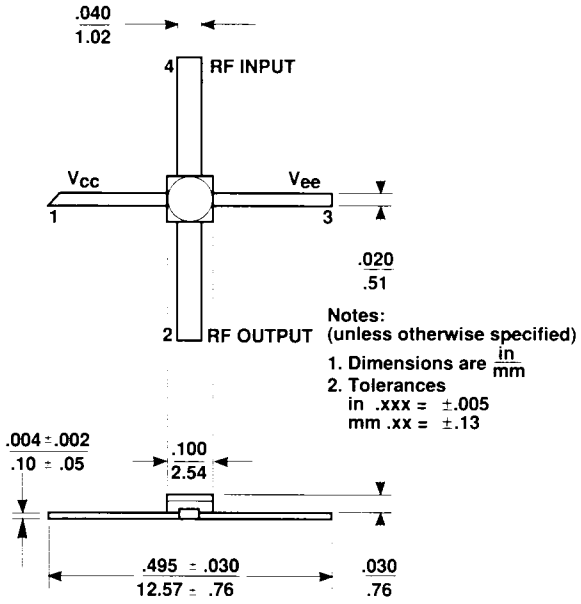
AVANTEK

IFD-50010
MagIC™ Silicon Bipolar MMIC
5 GHz Divide-by-4 Static Prescaler
September, 1989

Features

- **Wide Operating Frequency Range: 0.05 to 5 GHz typical**
- **Low Phase Noise: -140 dBc/Hz, 1 KHz offset**
- **High Input Sensitivity: -30 dBm at 1 GHz typical**
- **Low Output Level: -13 dBm typical**
- **Single Supply Voltage: V_{cc} = 5 V**
- **Low Power Dissipation: 125 mW typical**
- **Hermetic Gold-Ceramic Surface Mount Package**

Avantek 100 mil Package

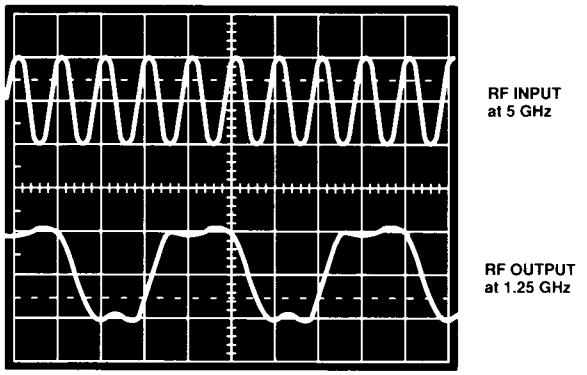


Description

Avantek's IFD-50010 is a low-phase-noise silicon bipolar static digital frequency divider using two scaled Emitter-Coupled-Logic (ECL) master-slave D flip-flops and sensitive buffer amplifiers. It is housed in a hermetic, high reliability ceramic package suitable for commercial, industrial and military applications. Typical applications include stabilized or digitally controlled local oscillators for GPS, TVRO, DBS, cellular radio and military communications receivers, and frequency synthesizers and counters in instrumentation systems.

The IFD series of digital frequency dividers is fabricated using Avantek's 15 GHz f_T, 20 GHz f_{MAX} ISOSAT™-I silicon bipolar process which uses nitride self-alignment, submicrometer lithography, trench isolation, ion implantation, gold metallization and polyimide inter-metal dielectric and scratch protection to achieve excellent performance, uniformity and reliability.

Typical Output Response With 5 GHz Input



Electrical Specifications[1], T_A = 25°C

Symbol	Parameters and Test Conditions: V_{cc} - V_{ee} = 5 V, Z_O = 50 Ω		Units	Min.	Typ.	Max.
F_{MAX}	Maximum Clock Frequency	P_{in} = −10 dBm (200 mVpp)	GHz	4.5	5.0	
F_{MIN}	Minimum Clock Frequency	P_{in} = −10 dBm (200 mVpp)	GHz		0.05	
IS	Input Sensitivity	f = 1 GHz	dBm		−30	
			mVpp		20	
OL	Output Level	f = 0.05 to 5 GHz	dBm		−13	
			mVpp		140	
SL_{MAX}	Highest Nonharmonic Spurious Level	f = 0.05 to 5 GHz	dBm		−35	
VSWR	Input VSWR	f = 0.05 to 5 GHz			1.5:1	
	Output VSWR	f = 0.05 to 5 GHz			2.0:1	
PN	SSB Phase Noise	f = 2 GHz, 1 kHz offset f = 4 GHz, 1 kHz offset	dBc/Hz		−140 −135	
T_r	Output Rise Time	f = 5 GHz	psec		100	
T_f	Output Fall Time	f = 5 GHz	psec		100	
I_{cc}	Supply Current		mA	20	25	35

Note: 1. The recommended operating voltage range for this device is 4.5 to 5.5 V.

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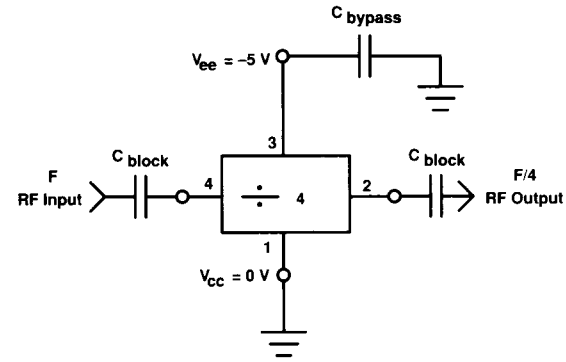
Absolute Maximum Ratings

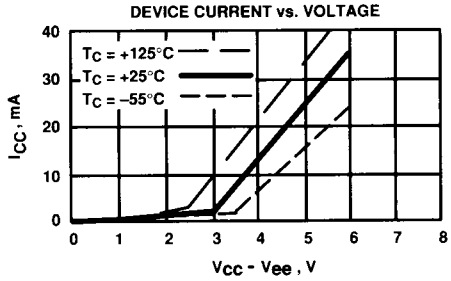
Parameter	Absolute Maximum[1]
Device Voltage	6 V
Power Dissipation[2,3]	250 mW
RF Input Power	+10 dBm
Junction Temperature	200°C
Storage Temperature	–65°C to 200°C
Thermal Resistance[2]: θ_{jc} = 95°C/W	

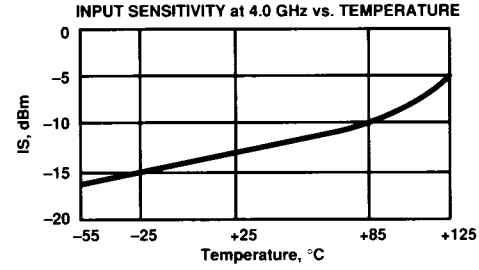
Notes:
1. Permanent damage may occur if any of these limits are exceeded.
2. T_{CASE} = 25°C
3. Derate at 10.5 mW/°C for T_C >176°C

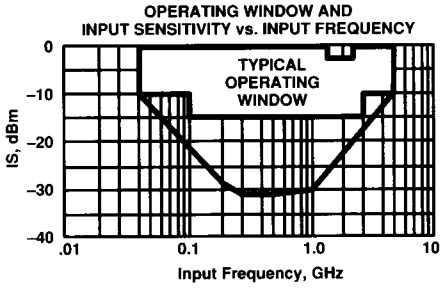
Typical Biasing Configuration

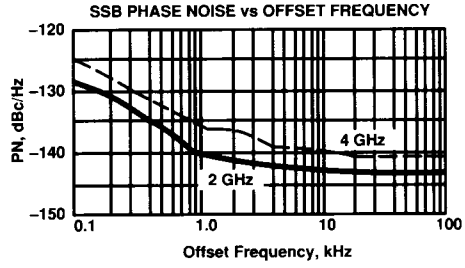


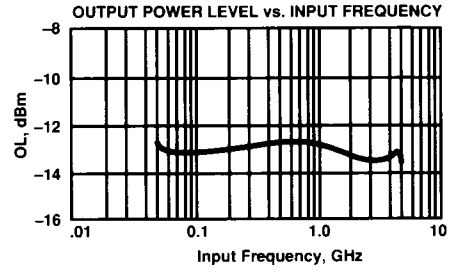
Typical Performance, T_A = 25°C
P_{in} = –10 dBm
(unless otherwise noted)



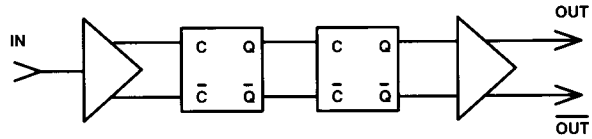




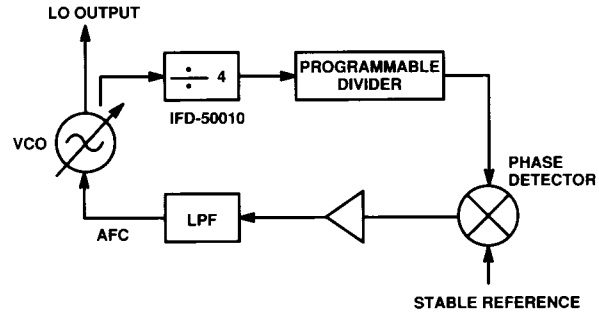




Chip Block Diagram



Typical Stabilized LO Configuration



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