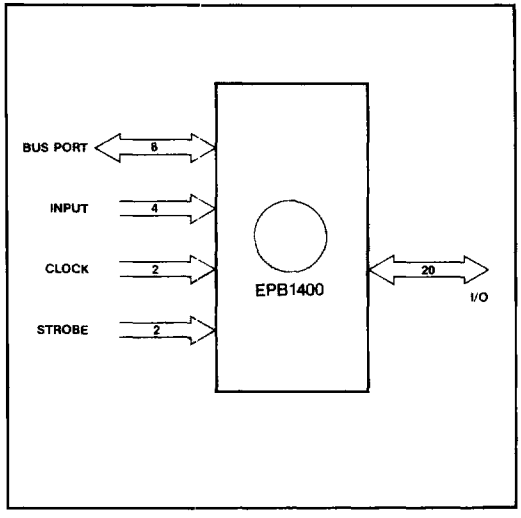
EPB1400 PROGRAMMABLE BUS PERIPHERAL

FEATURES

- Bus I/O—Register Intensive (Buster) EPLD
- Erasable, User-Configurable Logic Device for Customized Microprocessor Peripheral Functions.
- Byte-Wide Microprocessor Bus Port with Programmable Control.
- Dual Byte-Wide Input and Output Register's for Fully-Buffered Microprocessor Interfacing.
- 20 General-Purpose Macrocells for User-Defined Peripheral/Logic Functions Featuring:
  - Programmable Flip-Flop Type (D/T/JK/SR)
  - Synchronous or Asynchronous Clocking
  - 8 Product Terms per Macrocell
  - Individual OE Control per Macrocell
  - Independent Pin/Macrocell Feedback
- Over 1400 Equivalent 2-Input NAND Gates.
- Efficient Design Entry using TTL SSI and MSI Macrofunctions with Altera's A+PLUS Design System and LogiCaps Schematic Capture.
- Speed Equivalent to 74LS TTL for 25MHz Operation
- Low-Power CMOS Technology.
- 100% Generically Testable Insures 100% Programming Yield
- Packaged in 40 Pin Dual-In-Line (Plastic/ Cerdip) as well as 44 Lead JLCC or PLCC Chip Carriers.

LOGICAL PINOUT



GENERAL DESCRIPTION

The EPB1400 (Buster) EPLD from Altera represents the first Microprocessor Peripheral User-Configurable at the Silicon level. The device consists of a dedicated Byte-wide Bus-Interface Port and Input/Output Buffer Registers arranged around a universal Programmable Logic Device (PLD) core. The microprocessor interface is configurable by the user to match any required microprocessor bus, even when special or non-standard control interfaces are required by a specific application. On-chip buffering in the form of the Input and Output Registers allows the implementation of functions in the device which are loosely coupled to the controlling microprocessor. The universal PLD core may implement user-defined mixes of combinatorial and sequential logic. The result is a highly-integrated, programmable solution for customized peripheral functions without the attendant delays of a conventional custom or semi-custom solution.

The bidirectional, generic slave interface of the EPB1400 Bus Port fits virtually any microprocessor. Control interface is user-defined for the target processor using programmable logic structures. Integrating control and peripheral functions on a single chip insures zero wait-state operation with even 25MHz processors. Multiple devices may be operated in parallel to allow interfacing with 16- or 32-bit processors for more complex functions.

The Byte-wide Input Registers on Buster may be configured to operate in either a flow-through or edge-triggered mode. Synchronous strobe signals from designated pins allow high-speed control of transfers to and from the processor. Programmable logic control allows on-chip address decoding of the Register select lines.

High I/O count allows easy interfacing into any system. Dual feedback structures guarantee maximum utility from each pin: buried functions may be implemented while associated macrocell pins are used as inputs. Eight dedicated inputs, a Byte-wide Bus Port and 20 User-Configurable I/O pins give a high degree of interface flexibility.

ADVANCED INFORMATION

SPECIFICATIONS SUBJECT TO CHANGE

REV. 1.0

Output Latches (used to report device state back to the processor). The RELDINT output provides a reliable interrupt handshake with the processor, insuring timely reload of the input buffer register.

The central portion of the schematic shows two 74191 counter macrofunctions connected to form a loadable, 8 bit down counter. This counter is clocked at the system clock frequency, and on reaching zero generates a clock pulse to the parallel-serial converter. In addition, the initial count is automatically reloaded from the 74377 buffer register into the counter, assuring continuous bit rate division without external intervention. Two 74194 shift register macrofunctions implement the actual 8 bit serializer functions, and the other 74377 reigster acts as input data buffer register. Two 74373 output latches provide a mechanism for processor access to current bit rate count values or current shift register contents.

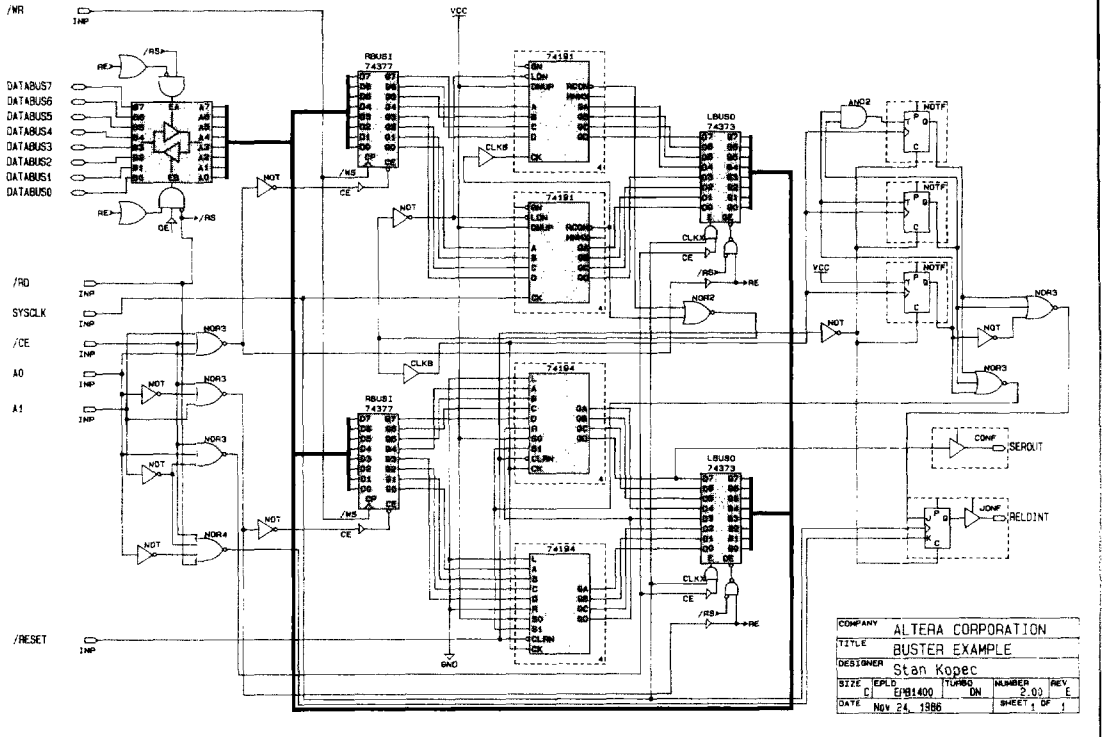
The upper right corner of the schematic shows a controlling state machine which generates interrupts to the CPU to initiate input buffer reload, as well as generating serializer load signals after each octet of data is sent. Finally, in the lower left is shown control and address decoding logic which controls processor access to the I/O registers on the chip. /RD,/WR,/CE, A0 and A1 are decoded as shown by the schematic, but are completely user-definable.

The possibilities are almost endless. Customized peripherals are as easy as Macrofunction schematic entry using familiar symbols.

Once the design entry is complete, the A+Plus software automatically expands the logic macros, minimizes the source logic and fits it to the device. Partially utilized TTL macros are compacted to eliminate "wasted" logic and pins. A JEDEC output map provides standard input for programming the device on an Altera programming unit or other third-part programmer. The entire cycle is performed within the uniform development environment of A+Plus with no translation, conversion or interface worries.

Simulation capability is available in the PLFSIM functional simulator offered by Altera. A user-friendly human interface allows multiple input and output formats so input vectors may be easily generated and simulation output results evaluated. High throughput is obtained by virtue of the functional nature of the simulator, thus allowing a larger range of input patterns to be simulated in a given amount of time.

EPB1400 TYPICAL APPLICATION—BUFFERED SERIALIZER WITH BIT RATE SCALER



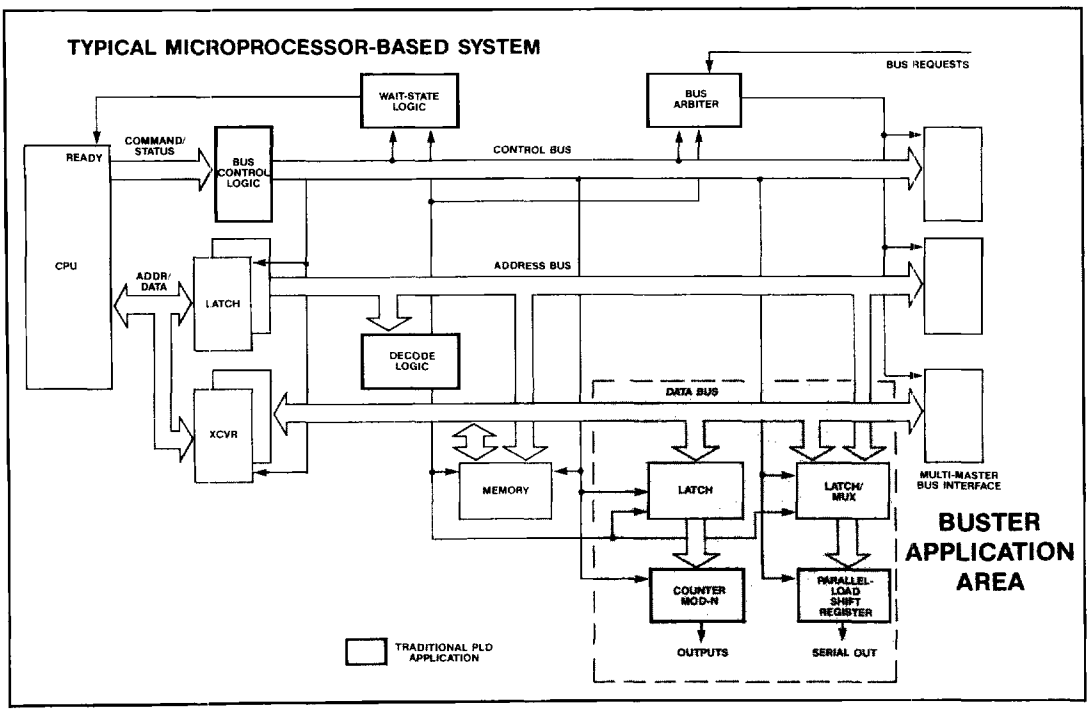
The 20 general-purpose logic macrocells feature programmable flip-flops, asynchronous or synchronous clocking, 8 product terms per macrocell, and other features shared with other Altera EPLDs. The full range of TTL functions available in Altera's LogiCaps Macrofunction library are available for implementation in Buster in any user-defined configuration.

The EPB1400 utilizes a sub-2 micron CMOS EPROM technology employing EPROM transistors to configure the internal logic array and device architecture. User-defined logic functions are constructed by selectively programming EPROM cells within the device. The EPROM technology also allows 100% generic testing at the factory. Cerdip devices may be erased by ultraviolet light, and design changes are therefore no longer costly or time-consuming. Design development, optimization and debug is thus an efficient process. For volume manufacturing, plastic One-Time-Programmable (OTP) versions of the device are available.

DESIGN DEVELOPMENT: APPLICATION EXAMPLE

The development software for Altera's User-Configurable Peripheral Logic Devices allows design at an efficient, Macrofunction level. In the LogiCaps schematic editor, specialized primitive symbols model the bus-interface logic of the devices. User-defined peripheral logic may be built behind this microprocessor interface using additional TTL Macrofunction elements. These elements may be invoked at either the SSI or MSI level: for example, individual 7474 elements may be used in design entry, or 74374 octal equivalents used where appropriate. Programmable flip-flop type (D,T, JK,SR), independent synchronous or asynchronous clocking of the Macrocells, flexible I/O and other standard Altera EPLD features are made available to the user in familiar terms.

An example is shown below which illustrates some of the capability available in the EPB1400. This example shows a medium-scale peripheral function to be interfaced to an 8088 microprocessor bus. The device logic implements a buffered serializer application with integral bit rate scaler. Address and control decoding, microprocessor programmable 8-bit rate scaler, 8-bit parallel-serial converter, data input buffering register and reload interrupt logic are all contained in a single device. The device is actually capable of operating at a 25MHz system clock rate, far beyond most available processor clock rates. In the upper left corner of the schematic is shown the bus transceiver primitive which models in LogiCaps the EPB1400 Bus Port circuitry. DATABUS (0-7) represents the 8086 microprocessor Address/Data Bus connections. To the right of the transceiver primitive is shown the device's internal bus structure which connects the various registers and logic cells on the device. Two 74377 Input Registers are shown connected to the internal bus, as well as two 74373



EPB1400 BLOCK DIAGRAM