ADE-XXX-XXX

HD49410FS
PIP Controller (PAL Suited)
(with Built-In A/D, D/a Converters)

HITACHI

Rev. 2
Sep. 1993

The HD49410FS is a memory controller for PAL suited PIP (picture-in-picture) systems and incorporates a 1-channel 6-bit A/D converter, a 2-channel 6-bit D/A converter, a 3-channel multiplexer, a 4 f_{SC} PLL circuit, and oscillators for memory read/write operations.
By combining this IC with four additional ICs (the HA118088, HA11567, HA11535, and HM53461), it is possible to construct a five-chip PIP system.

Functions

- PIP system memory controller
- 3-channel multiplexer with clamping function
- 1-channel, 6-bit 2.4 Msps A/D converter
- 2-channel, 6-bit 17 Msps D/A converter
- 4 f_{SC} (17 MHz) PLL
- Memory read oscillator, memory write oscillator

Features

- A PAL Suited PIP system can be constructed by combining this IC with four other ICs (HA118088, HA11567, HA11535, and HM53461).
- The size of the sub picture can be set to 1/3 or 1/4 the size of the main picture.
- The sub picture can be frozen (Still mode).
- The IC can process S signals (Y/C 2-signal processing).

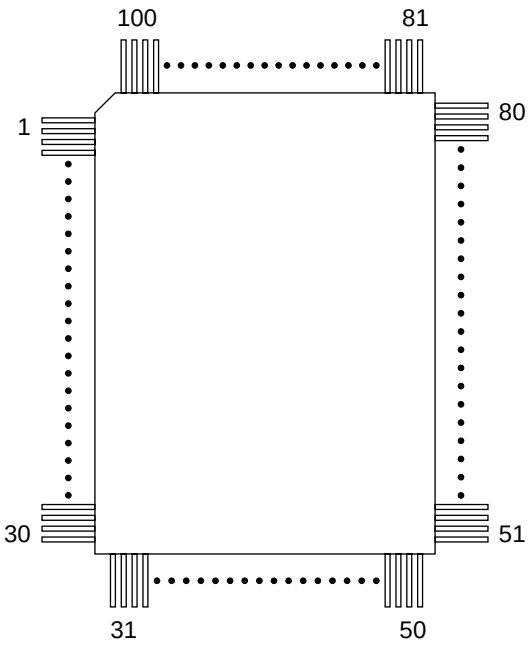
Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating	Unit
Supply voltage	V_{DDMax}	7	V
Power dissipation	P_T	434	mW
Digital input voltage	V_{ID}	-0.3 to V_{DD}+0.3	V
Analog input voltage	V_{IA}	-0.3 to V_{DD}+0.3	V
Operating temperature	Topr	-10 to +75	°C
Storage temperature	Tstg	-55 to +125	°C

Electrical Characteristics (V_{DD}=5V, Ta=25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Operating supply voltage	V_{DD}	4.75	5.00	5.25	V	
Current drawn	I_{DD}	-	60	-	mA	
Input current	I_{ID}	-10	-	10	µA	Digital input (CMOS, TTL)
Input V_{TH} (CMOS)	V_{THC}	1.5	-	3.5	V	CMOS input
Input V_{TH} (TTL)	V_{THT}	0.8	-	2.4	V	TTL input
Output voltage (H)	V_{OHC}	3.5	-	V_{DD}	V	CMOS output
Output voltage (L)	V_{OLC}	-	-	1.5	V	
ADC resolution		6	6	6	bit	
DAC resolution		6	6	6	bit	
PLL pull-in range (H)		4.87	-	-	MHz	
PLL pull-in range (L)		-	-	3.99	MHz	
R oscillation frequency	f_{ROSC}	-	16.2	-	MHz	
W oscillation frequency	f_{WOSC}	-	14.3	-	MHz	

Pin Arrangement



(Top View)

Pin Functions

Pin Function Table

Pin No.	Symbol	Function	I/O System (I/O Level)	I/O or Impedance	Active Level
1	PIP	PIP mode input	Schmitt	I	Hi
2	CY	Y signal clamping filter	Analog	(15 k)	
3	CRY	R-Y signal clamping filter	Analog	(2 k)	
4	CBY	B-Y signal clamping filter	Analog	(2 k)	
5	MPXO	Test-use pin			Note: Leave this pin open
6	PADJ1	Sub picture output timing control (1)	CMOS	I	Hi/Lo
7	ADGND	Analog system ground			
8	VRT	ADC reference voltage high level input	Analog		

Pin Function Table (cont)

Pin No.	Symbol	Function	I/O System (I/O Level)	I/O or Impedance	Active Level
9	VB	ADC comparator bias voltage	Analog	Open drain	
10	CSW	Main picture on/off signal input	Schmitt	I	Lo: Main picture off
11	ADVDD	Analog system V_{DD}			
12	Y	Y signal input	Analog	I: Gate input	
13	BS	Test-use pin	CMOS	I	Note: Fix to Hi
14	RY	R-Y signal input	Analog	I: Gate input	
15	TN	Test-use pin	CMOS	I	Note: Fix to Hi
16	BY	B-Y signal input	Analog	I: Gate input	
17	ALLR	Test-use pin	CMOS	I	Note: Fix to Lo
18	VRM	ADC reference voltage intermediate tap	Analog		
19	VRB	ADC reference voltage Lo level input	Analog		
20	DGND	Digital system ground			
21	DGND	Digital system ground			
22	SIFTC	Sub picture position shift	Schmitt	I	Shifts in a clockwise rotation each time a Lo/Hi pulse is input
23	DGND	Digital system ground			
24	DGND	Digital system ground			
25	VODD	Oscillator V_{DD}			
26	RCI	Read clock feedback signal	CMOS	O	Hi/Lo
27	RC	Read clock signal input	CMOS	I	Hi/Lo
28	PADJ2	Sub picture output timing control (2)	CMOS	I	Hi/Lo
29	MCP	Pedestal clamp timing signal	CMOS	O	Hi
30	OUTC	Sub picture output timing signal	CMOS	O	Hi: Sub picture display period

Pin Function Table (cont)

Pin No.	Symbol	Function	I/O System (I/O Level)	I/O or Impedance	Active Level
31	CLIP	Sub picture noise clip timing signal	CMOS	O	Hi: Clipping period
32	WAKU	Sub picture frame output timing signal	CMOS	O	Hi: Frame output period
33	DACK	DAC clock	CMOS	I	Hi/Lo
34	DA1	Digital signal input	CMOS	I	Hi/Lo
35	DA2				
36	DA3				
37	DA4				
38	DA5				
39	PALP	Main picture R-Y phase switching control	CMOS	I	Hi: Reverse phase Lo: Normal phase
40	REXY	DAC external resistor connection (1)	Analog		7.2 kΩ external resistor connected to V_{DD}
41	CBLY	DAC bypass capacitor connection (1)	Analog		
42	VREFY	DAC reference voltage input (1)	Analog	I: Gate input	
43	YO	Y signal output	Analog	O	150 Ω external resistor connected to V_{DD}
44	DAVDD	DAC V_{DD}			
45	REXC	DAC external resistor connection (2)	Analog		7.2 kΩ external resistor connected to V_{DD}
46	VREFC	DAC reference voltage input (2)	Analog	I: Gate input	
47	CBLC	DAC bypass capacitor connection (2)	Analog		
48	CO	C signal output	Analog	O	150 Ω external resistor connected to V_{DD}
49	DAGND	GND			
50	TS1	Test-use pin	CMOS	I	Note: Fix to Hi

Pin Function Table (cont)

Pin No.	Symbol	Function	I/O System (I/O Level)	I/O or Impedance	Active Level
51	TS2	Test-use pin	CMOS	I	Note: Fix ro Hi
52	(NC)	No connection			
53	TS3	Test-use pin	CMOS	I	Note: Fix to Hi
54	TS4				
55	TS5				
56	DA6	Digital signal input	CMOS	I	Hi/Lo
57	DA7				
58	DA8				
59	DACONT	Test-use pin	CMOS	I	Note: Fix to Hi
60	SUB VDD	Substrate V_{DD}			
61	CP	PLL phase comparator filter	Analog	(80 k)	
62	PLLGND	PLL ground			
63	FSCI	Main picture burst lock f_{SC} input	Analog	I	
64	PLLVDD	PLL V_{DD}			
65	DVDD	Digital system V_{DD}			
66	SO2	Memory read data input	TTL	I	Hi/Lo
67	SO3				
68	SO1				
69	SO4				
70	SC	Serial read clock output	CMOS	O	Hi/Lo
71	A7 (MSB)	Memory address data output	CMOS	O	Hi/Lo
72	A4				
73	A3				
74	A5				
75	A2				

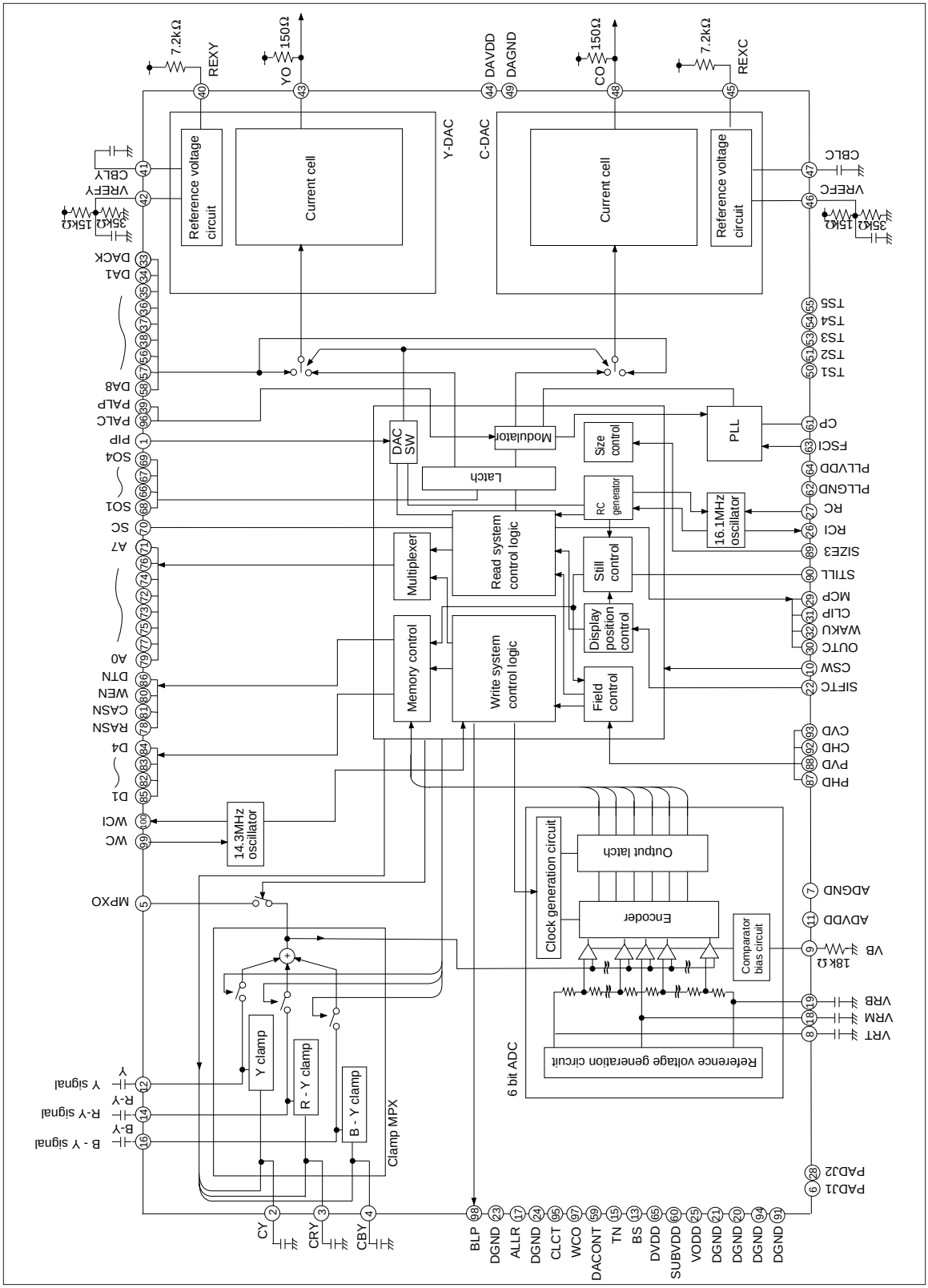
Pin Function Table (cont)

Pin No.	Symbol	Function	I/O System (I/O Level)	I/O or Impedance	Active Level
76	A6	Memory address data output	CMOS	O	Hi/Lo
77	A1				
78	RASN	Memory row address assigned output	CMOS	O	When Hi changes to Lo
79	A0 (LSB)	Memory address data output	CMOS	O	Hi/Lo
80	WEN	Sub picture data write control output	CMOS	O	Hi: Write inhibited
81	CASN	Memory column address assigned output	CMOS	O	When Hi changes to Lo
82	D2	Memory write data output	CMOS	O	Hi/Lo
83	D3				
84	D4				
85	D1				
86	DTN	Memory data transmission mode/ read mode control output	CMOS	O	Lo: Data transmission mode Hi: Read mode
87	PHD	Main picture horizontal sync signal input	Schmitt	I	Hi
88	PVD	Main picture vertical sync signal input	Schmitt	I	Hi
89	SIZE3	Sub picture size control	CMOS	I	Hi: 1/3 mode Lo: 1/4 mode
90	STILL	Sub picture still mode control	CMOS	I	Hi
91	DGND	Digital system ground			
92	CHD	Sub picture horizontal sync signal input	Schmitt	I	Hi
93	CVD	Sub picture vertical sync signal input	Schmitt	I	Hi
94	DGND	Digital system ground			

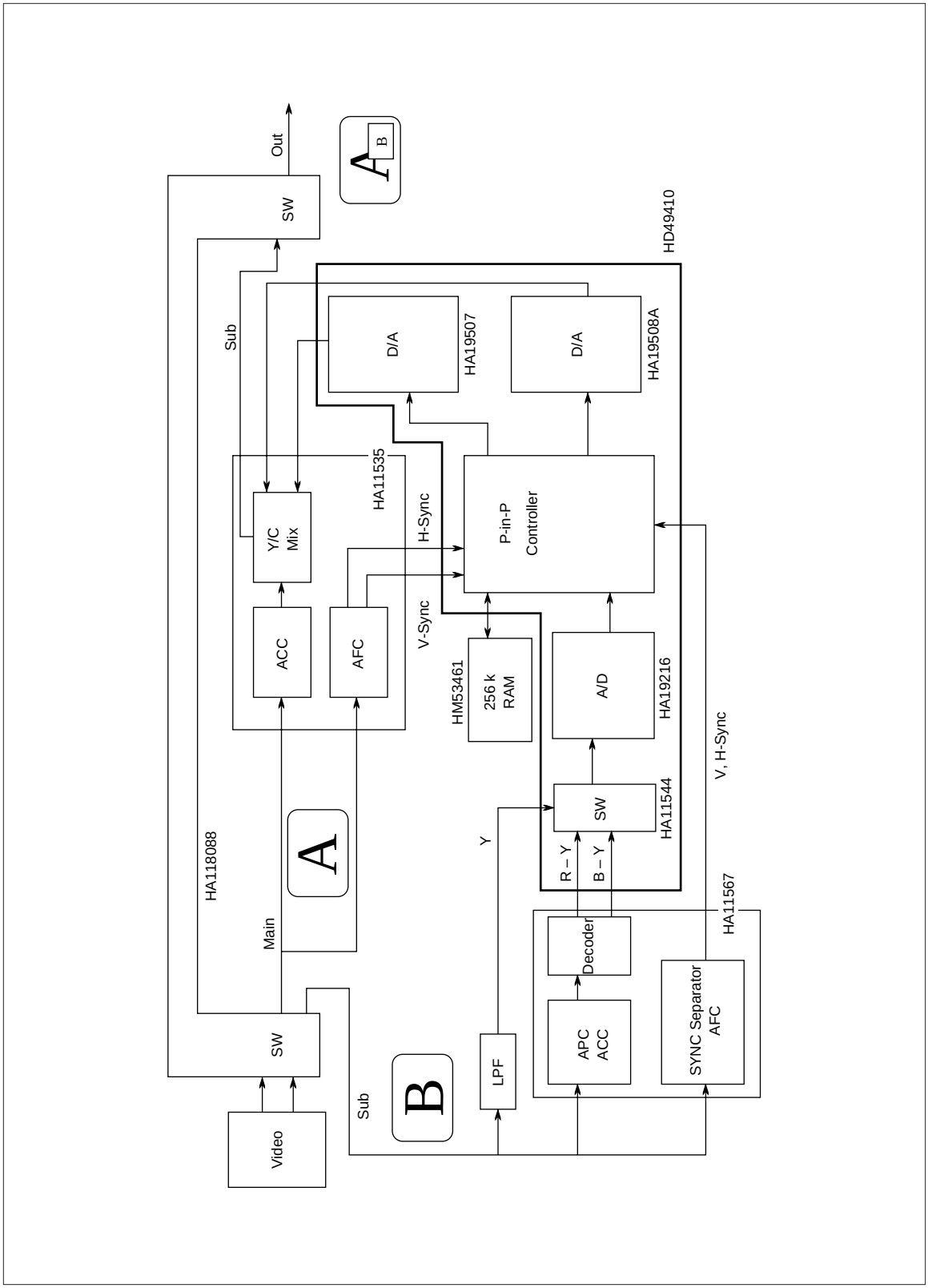
Pin Function Table (cont)

Pin No.	Symbol	Function	I/O System (I/O Level)	I/O or Impedance	Active Level
95	CLCT	Test-use pin	CMOS	I	Note: Fix to Hi
96	PALC	Sub picture R-Y phase switching control	CMOS	I	Hi: Reverse phase Lo: Normal phase
97	WCO	Test-use pin	CMOS	I/O	Note: Fix to Lo
98	BLP	Blanking pulse output	CMOS	O	Hi
99	WC	Write clock signal input	CMOS	I	Hi/Lo
100	WCI	Write clock feedback signal	CMOS	O	Hi/Lo

Block Diagram



PIP System Block Diagram



Package Dimensions

Unit : mm