042148

SHARP

LH52255

Data Sheet

64K x 4 CMOS Static RAM

Functional Description

The LH52255 is a high speed 262,144 bit static RAM organized as 64K x 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. Speed is enhanced by internally beginning read cycles after address transitions, resulting in fast Chip Select ($\overline{S}$) access times.

This RAM is fully static in operation. Cycles begin once addresses are stable.

Write cycles occur when both Chip Select ($\overline{S}$) and Write Enable ($\overline{W}$) are low. Data is transferred from the DQ pins and is written into the memory cells specified by the 16 address lines. Write cycles can begin once addresses are stable, given t_{SW} and t_{WP} are met.

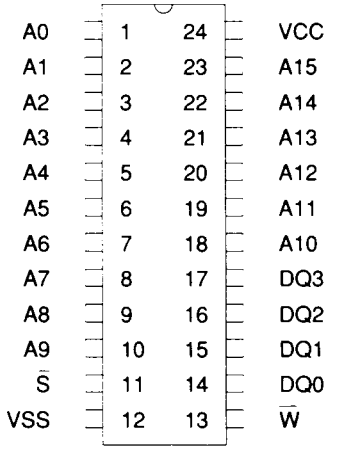
Read cycles occur when $\overline{S}$ is low and $\overline{W}$ is high. A read cycle will begin upon an address transition or on a rising edge of $\overline{W}$. The falling edge of $\overline{S}$ may occur up to t_{SA} before the end of the cycle without delaying valid data.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desireable. Series termination of the inputs should be considered when transmission line effects occur.

Features

- Fast Address Access Times - 25/30/35/45ns
- Fast Chip Select Access Times - 15/20/20/25/30ns
- 64K x 4 Organization
- TTL Compatible Inputs and Outputs
- 5V ±10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count
- 300-Mil, 24-Pin DIP
- JEDEC Standard Pinout

Pin Diagram



Truth Table

$\overline{S}$	$\overline{W}$	Mode	DQ	Icc
H	X	Not Selected	High Z	Active
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

Pin Identification

A_0-A_{15} . . . . . Address Inputs
DQ_0-DQ_3 . . . . . Data Inputs/Outputs
$\overline{S}$ . . . . . Chip Select Input
$\overline{W}$ . . . . . Write Enable Input
V_{CC} . . . . . Positive Power Supply
V_{SS} . . . . . Ground

Absolute Maximum Ratings [1]

Supply Voltage to Ground Potential	-0.5V to 7V
Input Voltage Range	-0.5V to V_{CC}+0.5V
DC Output Current [2]	± 40 mA
Storage Temperature Range	-65°C to 150°C
Power Dissipation (Package Limit) [2]	1.0W

Operating Ranges

Symbol	Parameter	Min	Typ	Max	Unit
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [3]	-0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC}+0.5	V

DC Electrical Characteristics - Over Operating Range

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
I_{CC1}	Operating Current [4,5]	Outputs open, t_{RC}=25ns			150	mA
I_{CC1}	Operating Current [4]	Outputs open, t_{RC}=30ns			135	mA
I_{CC1}	Operating Current [4]	Outputs open, t_{RC}=35ns			120	mA
I_{CC1}	Operating Current [4]	Outputs open, t_{RC}=45ns			100	mA
I_{CC1}	Operating Current [4]	Outputs open, t_{RC}=55ns			85	mA
$_{CC1}$	Operating Current [4]	Outputs open, t_{RC}=100ns			45	mA
I_{LI}	Input Leakage Current	V_{CC}=5.5V, V_{in}=0V to V_{CC}	-2		+2	µA
I_{LO}	I/O Leakage Current	V_{CC}=5.5V, V_{in}=0V to V_{CC}	-10		+10	µA
V_{OH}	Output High Voltage	I_{OH}=-4.0mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL}=8.0mA			0.4	V

See notes following "Switching Characteristics"

Switching Characteristics - Over Operating Range [6]

Symbol	Description	-25 [5] Min	-25 [5] Max	-30 Min	-30 Max	-35 Min	-35 Max	-45 Min	-45 Max	Units
Read Cycle										
t_{RC}	Read Cycle Time	25		30		35		45		ns
t_{AA}	Address Access Time		25		30		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		3		ns
t_{SA}	$\overline{S}$ Low to Valid Data		15		20		20		25	ns
t_{SLZ}	$\overline{S}$ Low to Output Active [7,8]	3		3		3		3		ns
t_{SHZ}	$\overline{S}$ High to Output High Z [7,8]		15		15		15		20	ns
Write Cycle										
t_{WC}	Write Cycle Time	25		30		35		45		ns
t_{SW}	$\overline{S}$ Low to End of Write	20		25		25		40		ns
t_{AW}	Address Valid to End of Write	20		25		25		45		ns
t_{AS}	Address Setup	0		0		0		0		ns
t_{AH}	Address Hold from $\overline{W}$ High	3		3		3		3		ns
t_{WP}	$\overline{W}$ Pulse Width	20		25		25		40		ns
t_{DW}	Input Data Setup Time	10		15		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		0		ns
t_{WLZ}	$\overline{W}$ High to Output Active [7,8]	0		0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High Z [7,8]		10		10		10		15	ns

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of up to 3.0V in amplitude are permitted once per cycle.
4. I_{CC} is dependent upon actual output loading and cycle rates. Specified values are with outputs open, operating at minimum cycle times.
5. -25 specifications are preliminary.
6. Switching Characteristics measurements performed at "AC Test Condition" levels.
7. Active output to High Z and Output High Z to Active tests specified for a 200mV transition from steady state voltage levels into the test load.
8. Sample tested only.
9. Capacitances are maximum values at VCC = 5.0 Volts, $T_A = 25^{\circ}C$, measured at 1.0 MHz with V_{in}=0V.

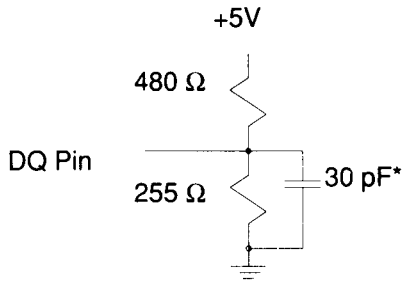
AC Test Conditions

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	5ns
Input and Output Timing Ref. Levels	1.5V
Output Load, Timing Tests	See Figure Below

Capacitance [8,9]

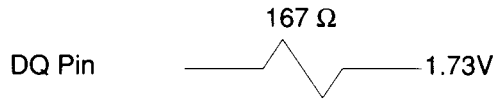
C_{IN} (Input Capacitance)	5pF
C_{DQ} (Input/Output Capacitance)	7pF

Equivalent Test Load



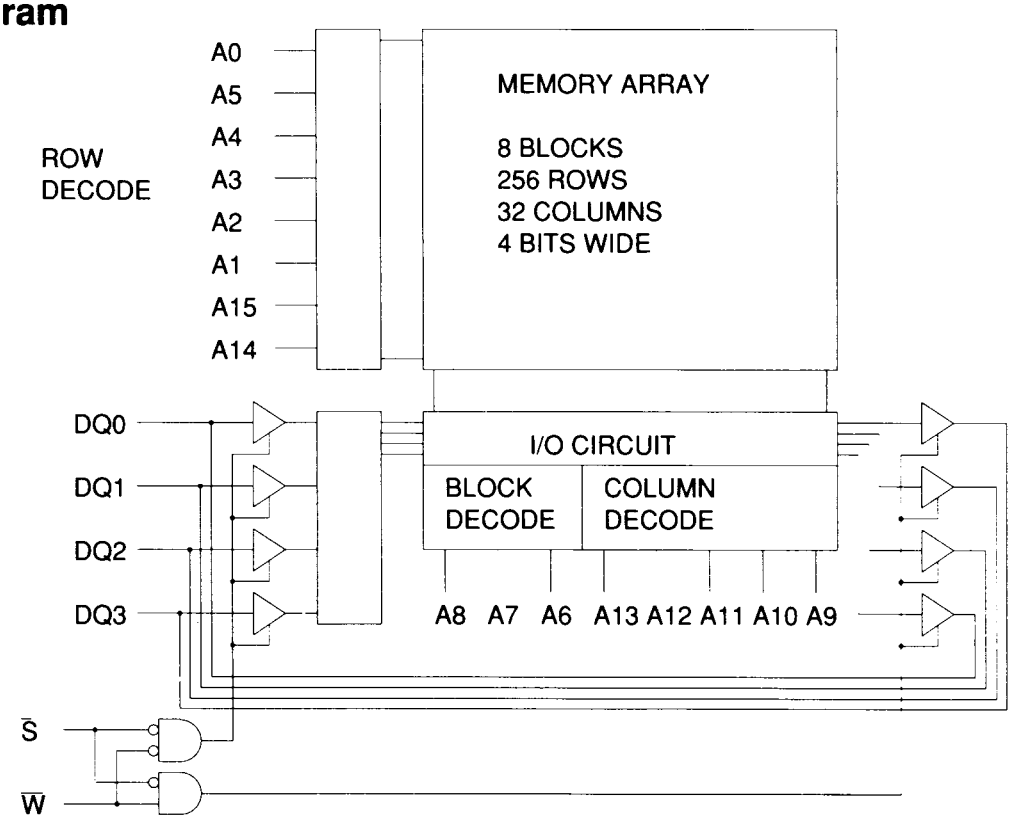
* Includes scope and jig capacitance.

Actual Test Load



Test fixture has an intrensic 30 pF (min)

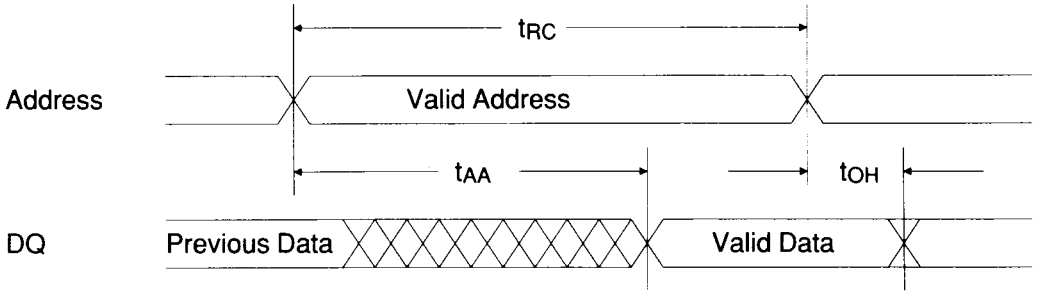
Block Diagram



Switching Waveforms - Read Cycle

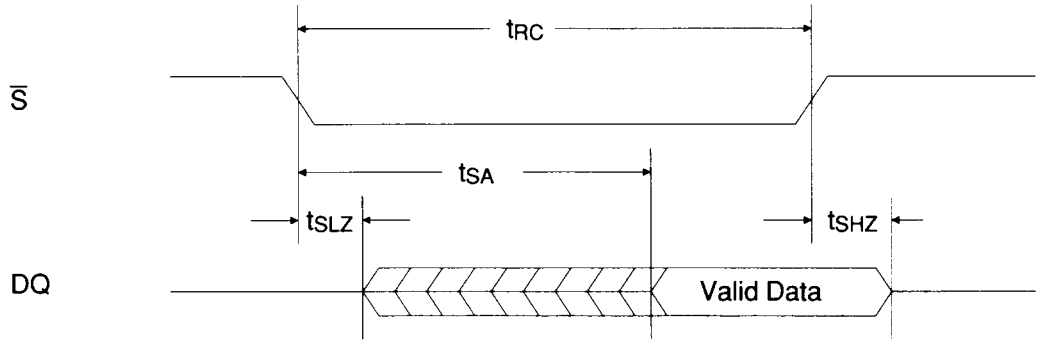
Read Cycle No. 1

Chip is in the Read Mode: $\overline{W}$ is HIGH and $\overline{S}$ is LOW. Read Cycle timing is referenced from when all addresses are stable until the next address transition. Crosshatched portion of DQ implies that data lines are in the low Z state and the data may not be valid.



Read Cycle No. 2

Chip is in the Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case where addresses are valid t_{AA} before valid data is required. Data Out is not specified to be valid until t_{SA}, but may become valid as soon as t_{SLZ}. Outputs will transition directly from high Z to valid Data Out.

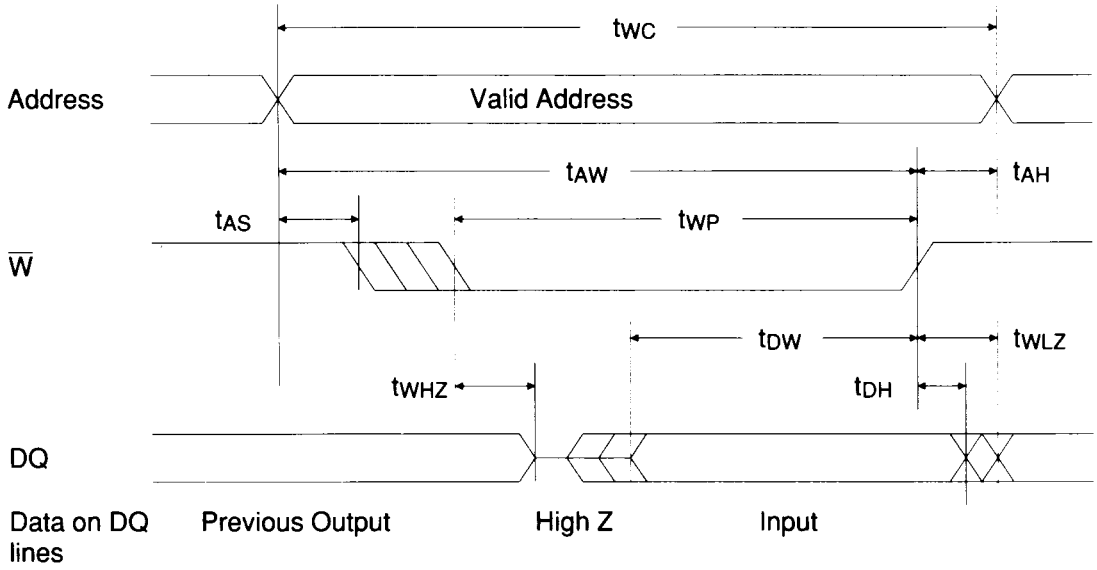


Switching Waveforms - Write Cycle

Addresses must be stable during Write Cycles. $\overline{S}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the high Z state if $\overline{W}$ is LOW when $\overline{S}$ goes LOW. Care should be taken so that the output drivers on the LH52255 are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

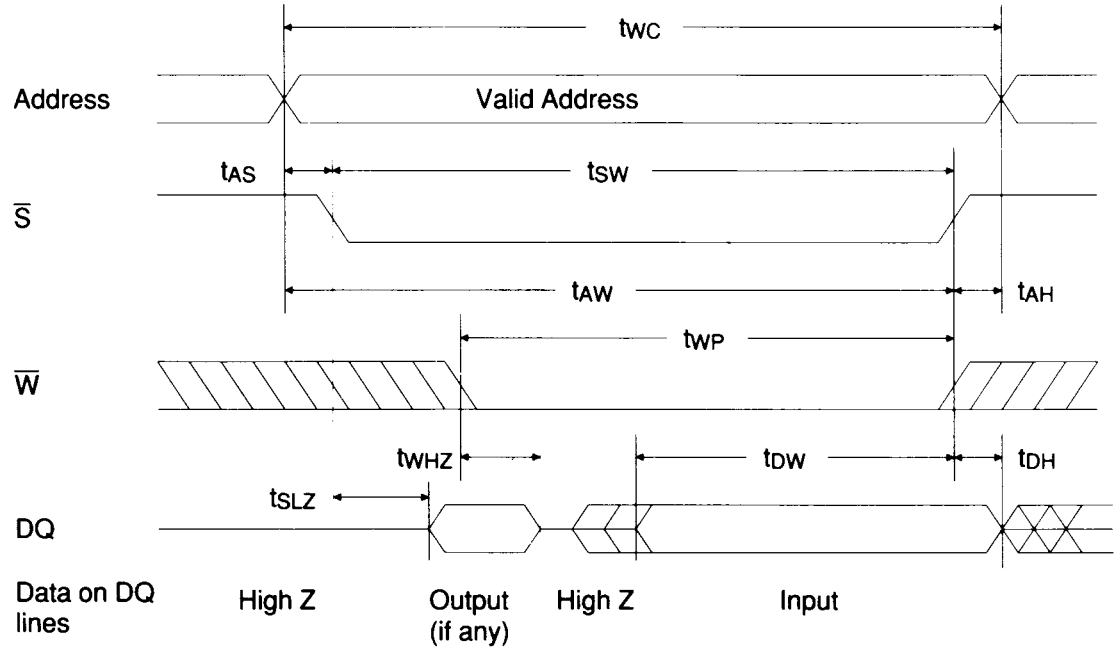
Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{S}$ is LOW. Using only $\overline{W}$ to control Write Cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

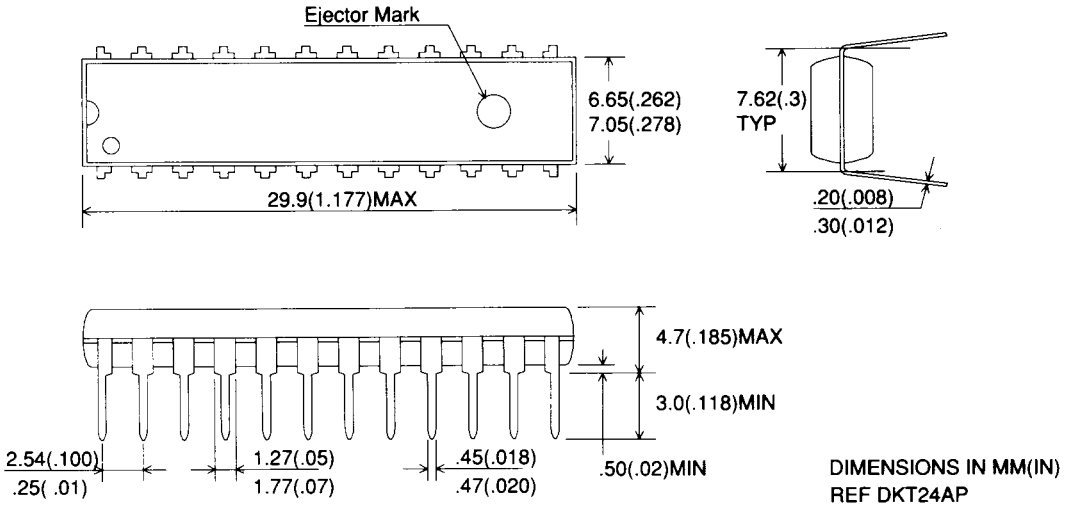


Write Cycle No. 2 ($\overline{S}$ Controlled)

DQ lines may transition to low Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{S}$.



Package Diagram - 24 pin plastic DIP



Ordering Information

Ordering Code	Speed	Package Type
LH52255-25 [5]	25ns	Plastic DIP
LH52255-30	30ns	Plastic DIP
LH52255-35	35ns	Plastic DIP
LH52255-45	45ns	Plastic DIP
LH52255-55	55ns	Plastic DIP

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