CD4504BMS

CMOS Hex Voltage Level Shifter for TTL-to-CMOS or CMOS-to-CMOS Operation

December 1992

Features

- **High Voltage Type (20V Rating)**
- **Independence of Power Supply Sequence Considerations**
  - **VCC can Exceed VDD**
  - **Input Signals can Exceed Both VCC and VDD**
- **Up and Down Level Shifting Capability**
- **Shiftable Input Threshold for Either CMOS or TTL Compatibility**
- **100% Tested for Quiescent Current at 20V**
- **5V, 10V and 15V Parametric Ratings**
- **Standardized Symmetrical Output Characteristics**
- **Maximum Input Current of 1μA at 18V Over Full Package Temperature Range; 100nA at 18V and +25°C**
- **Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"**

Description

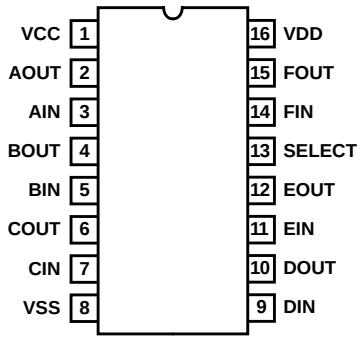
CD4504BMS hex voltage level shifter consists of six circuits which shift input signals from the VCC logic level to the VDD logic level. To shift TTL signals to CMOS logic levels, the SELECT input is at the VCC HIGH logic state. When the SELECT input is at a LOW logic state, each circuit translates signals from one CMOS level to another.

The CD4504BMS is supplied in these 16-lead outline packages:

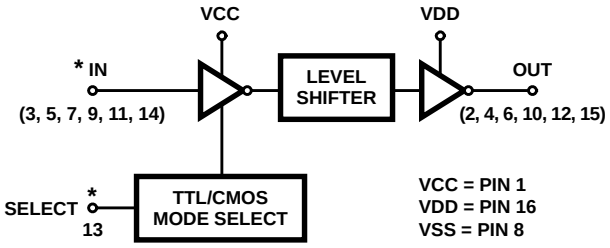
Frit Seal DIP	H1F
Ceramic Flatpack	H6W

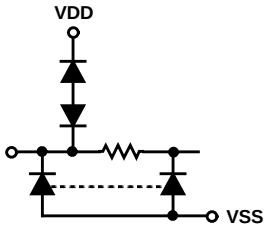
Pinout

CD4504BMS
TOP VIEW



Functional Diagram





* ALL INPUTS ARE PROTECTED BY CMOS PROTECTION NETWORK

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

File Number **3336**

Absolute Maximum Ratings

DC Supply Voltage Range, (VDD) . . . . . -0.5V to +20V
(Voltage Referenced to VSS Terminals)
Input Voltage Range, All Inputs . . . . . -0.5V to VDD +0.5V
DC Input Current, Any One Input . . . . . ±10mA
Operating Temperature Range . . . . . -55°C to +125°C
Package Types D, F, K, H
Storage Temperature Range (TSTG) . . . . . -65°C to +150°C
Lead Temperature (During Soldering) . . . . . +265°C
At Distance 1/16 ± 1/32 Inch (1.59mm ± 0.79mm) from case for 10s Maximum

Reliability Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP and FRIT Package	80°C/W	20°C/W
Flatpack Package	70°C/W	20°C/W

Maximum Package Power Dissipation (PD) at +125°C
For TA = -55°C to +100°C (Package Type D, F, K) 500mW
For TA = +100°C to +125°C (Package Type D, F, K) . . . . . Derate Linearity at 12mW/°C to 200mW
Device Dissipation per Output Transistor 100mW
For TA = Full Package Temperature Range (All Package Types)
Junction Temperature . . . . . +175°C

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)		GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 20V, VIN = VDD or GND		1	+25°C	-	2	µA
				2	+125°C	-	200	µA
		VDD = 18V, VIN = VDD or GND		3	-55°C	-	2	µA
Input Leakage Current	IIL	VIN = VDD or GND	VDD = 20	1	+25°C	-100	-	nA
				2	+125°C	-1000	-	nA
			VDD = 18V	3	-55°C	-100	-	nA
Input Leakage Current	IIH	VIN = VDD or GND	VDD = 20	1	+25°C	-	100	nA
				2	+125°C	-	1000	nA
			VDD = 18V	3	-55°C	-	100	nA
Output Voltage	VOL15	VDD = 15V, No Load		1, 2, 3	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH15	VDD = 15V, No Load (Note 3)		1, 2, 3	+25°C, +125°C, -55°C	14.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V		1	+25°C	0.53	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V		1	+25°C	1.4	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V		1	+25°C	3.5	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V		1	+25°C	-	-0.53	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V		1	+25°C	-	-1.8	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V		1	+25°C	-	-1.4	mA
Output Current (Source)	IOH15	VDD = 15V, VOUT = 13.5V		1	+25°C	-	-3.5	mA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA		1	+25°C	-2.8	-0.7	V
P Threshold Voltage	VPTH	VSS = 0V, IDD = 10µA		1	+25°C	0.7	2.8	V
Functional	F	VDD = 4.5V, VCC = 2.8, VIN = VDD or GND		7	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 4.5V, VCC = 3.0, VIN = VDD or GND		8B	-55°C			
		VDD = 18V, VCC = 18V, VIN = GND or VCC		8A	+125°C			
		VDD = 18V, VCC = 4.5V, VIN = VCC or GND		8A	+125°C			
		VDD = 4.5V, VCC = 18V, VIN = VCC or GND		8A	+125°C			
		VDD = 20V, VCC = 20V, VIN = GND or VCC		7	+25°C			
		VDD = 20V, VCC = 4.5V, VIN = VCC or GND		7	+25°C			
		VDD = 4.5V, VCC = 20V, VIN = VCC or GND		7	+25°C			

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS (NOTE 1)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Voltage Low (Note 2) TTL-CMOS	VIL	VDD = 15V, VOH > 13.5V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	-	0.8	V
Input Voltage High (Note 2) TTL-CMOS	VIH	VDD = 15V, VOH > 13.5V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	2	-	V
Input Voltage Low (Note 2) CMOS-CMOS	VIL	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High (Note 2)CMOS-CMOS	VIH	VDD = 10V, VOH > 9V, VOL < 1V VCC = 5V	1, 2, 3	+25°C, +125°C, -55°C	3.5	-	V
Input Voltage Low (Note 2) CMOS-CMOS	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V	1, 2, 3	+25°C, +125°C, -55°C	-	3	V
Input Voltage High (Note 2) CMOS-CMOS	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 10V	1, 2, 3	+25°C, +125°C, -55°C	7	-	V

NOTES:
1. All voltages referenced to device GND, 100% testing being implemented.
2. Go/No Go test with limits applied to inputs.
3. For accuracy, voltage is measured differentially to VDD. Limit is 0.050V max.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS (NOTE 1, 2)	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay TTL to CMOS VDD > VCC	TPHL1	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Propagation Delay CMOS to CMOS VDD > VCC	TPHL2	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	240	ns
			10, 11	+125°C, -55°C	-	324	ns
Propagation Delay CMOS to CMOS VCC > VDD	TPHL3	VDD = 5V, VIN = VCC or GND VCC = 10V	9	+25°C	-	550	ns
			10, 11	+125°C, -55°C	-	743	ns
Propagation Delay TTL to CMOS VDD > VCC	TPLH1	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	280	ns
			10, 11	+125°C, -55°C	-	378	ns
Propagation Delay CMOS to CMOS VDD > VCC	TPLH2	VDD = 10V, VIN = VCC or GND VCC = 5V	9	+25°C	-	240	ns
			10, 11	+125°C, -55°C	-	324	ns
Propagation Delay CMOS to CMOS VCC > VDD	TPLH3	VDD = 5V, VIN = VCC or GND VCC = 10V	9	+25°C	-	400	ns
			10, 11	+125°C, -55°C	-	540	ns
Transition Time	TTHL TTLH	All Modes	9	+25°C	-	200	ns
			10, 11	+125°C, -55°C	-	270	ns

NOTES:
1. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
2. -55°C and +125°C limits guaranteed, 100% testing being implemented.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	IDD	VDD = 5V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	1	µA
				+125°C	-	30	µA
		VDD = 10V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	60	µA
		VDD = 15V, VIN = VDD or GND	1, 2	-55°C, +25°C	-	2	µA
				+125°C	-	120	µA
Output Voltage	VOL	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOL	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	-	50	mV
Output Voltage	VOH	VDD = 5V, No Load	1, 2	+25°C, +125°C, -55°C	4.95	-	V
Output Voltage	VOH	VDD = 10V, No Load	1, 2	+25°C, +125°C, -55°C	9.95	-	V
Output Current (Sink)	IOL5	VDD = 5V, VOUT = 0.4V	1, 2	+125°C	0.36	-	mA
				-55°C	0.64	-	mA
Output Current (Sink)	IOL10	VDD = 10V, VOUT = 0.5V	1, 2	+125°C	0.9	-	mA
				-55°C	1.6	-	mA
Output Current (Sink)	IOL15	VDD = 15V, VOUT = 1.5V	1, 2	+125°C	2.4	-	mA
				-55°C	4.2	-	mA
Output Current (Source)	IOH5A	VDD = 5V, VOUT = 4.6V	1, 2	+125°C	-	-0.36	mA
				-55°C	-	-0.64	mA
Output Current (Source)	IOH5B	VDD = 5V, VOUT = 2.5V	1, 2	+125°C	-	-1.15	mA
				-55°C	-	-2.0	mA
Output Current (Source)	IOH10	VDD = 10V, VOUT = 9.5V	1, 2	+125°C	-	-0.9	mA
				-55°C	-	-1.6	mA
Output Current (Source)	IOH15	VDD =15V, VOUT = 13.5V	1, 2	+125°C	-	-2.4	mA
				-55°C	-	-4.2	mA
Input Voltage Low TTL - CMOS	VIL	VDD = 10V, VOH > 9V, VOL < 1V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	-	0.8	V
Input Voltage High TTL - CMOS	VIH	VDD = 10V, VOH > 9V, VOL < 1V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	2	-	V
Input Voltage Low CMOS - CMOS	VIL	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	-	1.5	V
Input Voltage High CMOS - CMOS	VIH	VDD = 15V, VOH > 13.5V, VOL < 1.5V, VCC = 5V	1, 2	+25°C, +125°C, -55°C	3.5	-	V
Propagation Delay TTL - CMOS, VDD > VCC	TPHL1	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	280	ns
Propagation Delay CMOS - CMOS, VDD > VCC	TPHL2	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25°C	-	140	ns
Propagation Delay CMOS - CMOS, VCC > VDD	TPHL3	VDD = 5V, VCC = 15V	1, 2, 3	+25°C	-	550	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25°C	-	140	ns
Propagation Delay TTL - CMOS, VDD > VCC	TPLH1	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	280	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay CMOS - CMOS, VDD > VCC	TPLH2	VDD = 15V, VCC = 5V	1, 2, 3	+25°C	-	240	ns
		VDD = 15V, VCC = 10V	1, 2, 3	+25°C	-	140	ns
Propagation Delay CMOS - CMOS VCC > VDD	TPLH3	VDD = 5V, VCC = 15V	1, 2, 3	+25°C	-	400	ns
		VDD = 10V, VCC = 15V	1, 2, 3	+25°C	-	120	ns
Transition Time	TTHL TTLH	VDD = 10V	1, 2, 3	+25°C	-	100	ns
		VDD = 15V	1, 2, 3	+25°C	-	80	ns
Input Capacitance	CIN	Any Input	1, 2	+25°C	-	7.5	pF

NOTES:

1. All voltages referenced to device GND.
2. The parameters listed on Table 3 are controlled via design or process and are not directly tested. These parameters are characterized on initial design release and upon design changes which would affect these characteristics.
3. CL = 50pF, RL = 200K, Input TR, TF < 20ns.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Supply Current	IDD	VDD = 20V, VIN = VDD or GND	1, 4	+25°C	-	7.5	µA
N Threshold Voltage	VNTH	VDD = 10V, ISS = -10µA	1, 4	+25°C	-2.8	-0.2	V
N Threshold Voltage Delta	ΔVTN	VDD = 10V, ISS = -10µA	1, 4	+25°C	-	±1	V
P Threshold Voltage	VTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	0.2	2.8	V
P Threshold Voltage Delta	ΔVTP	VSS = 0V, IDD = 10µA	1, 4	+25°C	-	±1	V
Functional	F	VDD = 18V, VIN = VDD or GND	1	+25°C	VOH > VDD/2	VOL < VDD/2	V
		VDD = 3V, VIN = VDD or GND					
Propagation Delay Time	TPHL TPLH	VDD = 5V	1, 2, 3, 4	+25°C	-	1.35 x +25°C Limit	ns

NOTES: 1. All voltages referenced to device GND.
2. CL = 50pF, RL = 200K, Input TR, TF < 20ns.
3. See Table 2 for +25°C limit.
4. Read and Record

TABLE 5. BURN-IN AND LIFE TEST DELTA PARAMETERS +25°C

PARAMETER	SYMBOL	DELTA LIMIT
Supply Current - MSI-1	IDD	± 0.2µA
Output Current (Sink)	IOL5	± 20% x Pre-Test Reading
Output Current (Source)	IOH5A	± 20% x Pre-Test Reading

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 1 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
Interim Test 2 (Post Burn-In)	100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)	100% 5004	1, 7, 9, Deltas	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP		MIL-STD-883 METHOD	GROUP A SUBGROUPS	READ AND RECORD
Interim Test 3 (Post Burn-In)		100% 5004	1, 7, 9	IDD, IOL5, IOH5A
PDA (Note 1)		100% 5004	1, 7, 9, Deltas	
Final Test		100% 5004	2, 3, 8A, 8B, 10, 11	
Group A		Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group B	Subgroup B-5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Deltas	Subgroups 1, 2, 3, 9, 10, 11
	Subgroup B-6	Sample 5005	1, 7, 9	
Group D		Sample 5005	1, 2, 3, 8A, 8B, 9	Subgroups 1, 2 3

NOTE: 1. 5% Parameteric, 3% Functional; Cumulative for Static 1 and 2.

TABLE 7. TOTAL DOSE IRRADIATION

CONFORMANCE GROUPS	MIL-STD-883 METHOD	TEST		READ AND RECORD	
		PRE-IRRAD	POST-IRRAD	PRE-IRRAD	POST-IRRAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 9	Table 4

TABLE 8. BURN-IN AND IRRADIATION TEST CONNECTIONS

FUNCTION	OPEN	GROUND	VDD	9V ± -0.5V	OSCILLATOR	
					50kHz	25kHz
Static Burn-In 1 (Note 1)	2, 4, 6, 10, 12, 15	3, 5, 7-9, 11, 14	16	1, 13		
Static Burn-In 2 (Note 1)	2, 4, 6, 10, 12, 15	8	16	1, 3, 5, 7, 9, 11, 13, 14		
Dynamic Burn-In (Note 1, 3)	-	8	16	1, 2, 4, 6, 10, 12, 15	3, 5, 7, 9, 11, 14	
Irradiation (Note 2)	2, 4, 6, 10, 12, 15	8	1, 3, 5, 7, 9, 11, 13, 14, 16			

NOTES:

1. Each pin except VCC, VDD and GND will have a series resistor of 10K ± 5%, VDD = 18V ± 0.5V
2. Each pin except VCC, VDD and GND will have a series resistor of 47K ± 5%; Group E, Subgroup 2, sample size is 4 dice/wafer, 0 failures, VDD = 10V ± 0.5V
3. Oscillator output to be VDD/2.

Typical Performance Characteristics

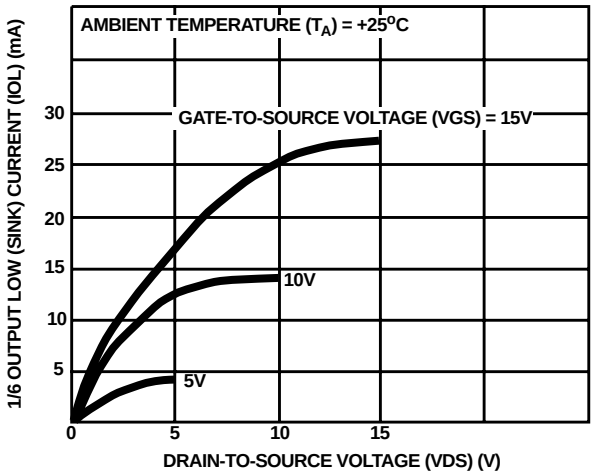


FIGURE 1. TYPICAL OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

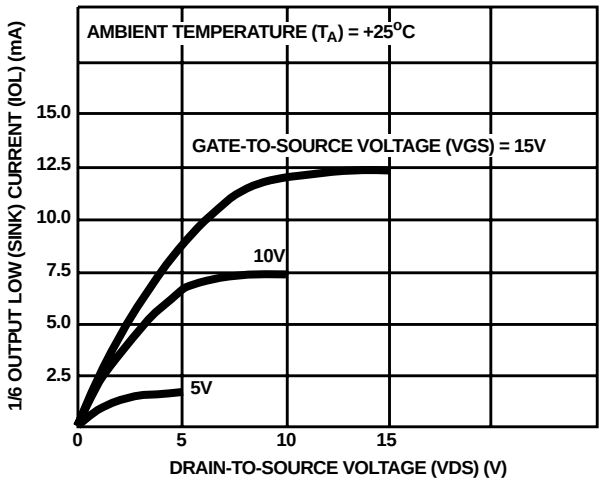


FIGURE 2. MINIMUM OUTPUT LOW (SINK) CURRENT CHARACTERISTICS

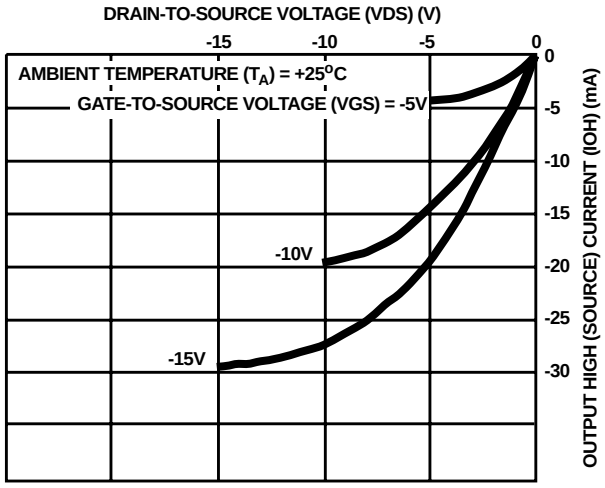


FIGURE 3. TYPICAL OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

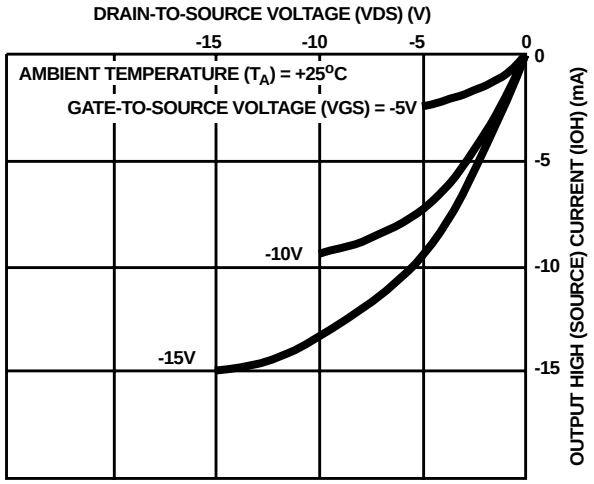


FIGURE 4. MINIMUM OUTPUT HIGH (SOURCE) CURRENT CHARACTERISTICS

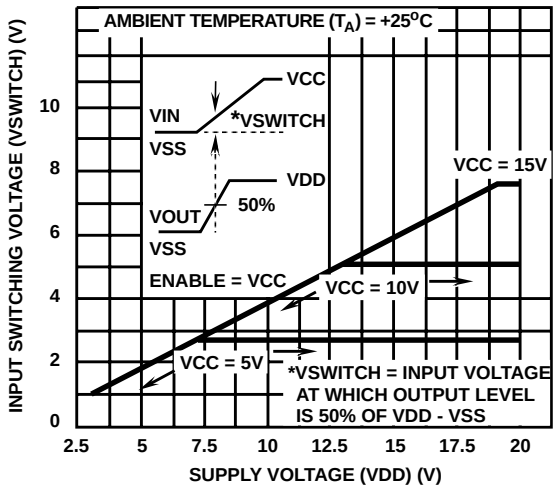


FIGURE 5. TYPICAL INPUT SWITCHING AS A FUNCTION OF HIGH LEVEL SUPPLY VOLTAGE (SELECT AT VCC-CMOS MODE)

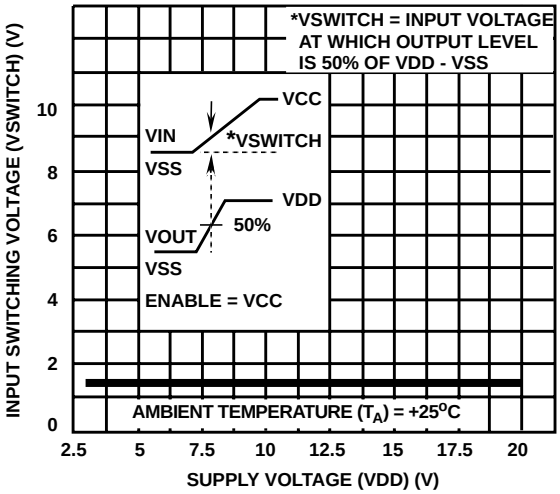


FIGURE 6. TYPICAL INPUT SWITCHING AS A FUNCTION OF HIGH LEVEL SUPPLY VOLTAGE (SELECT AT VSS-TTL MODE)

Typical Performance Characteristics (Continued)

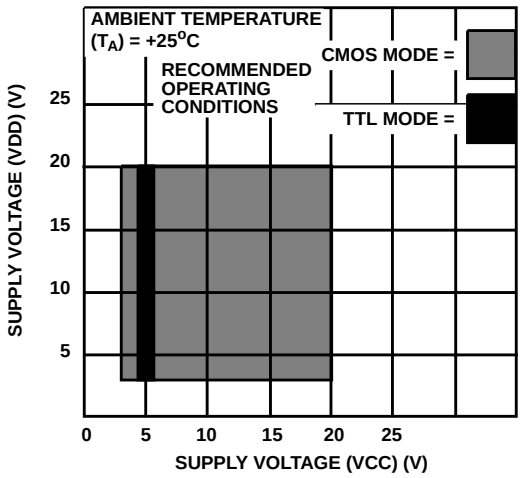
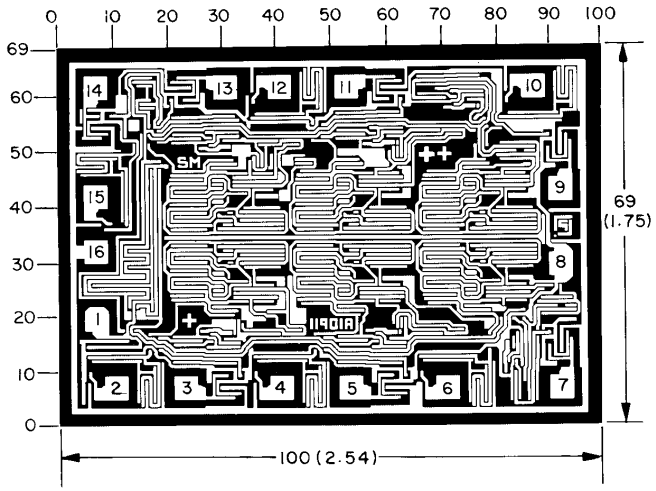


FIGURE 7. HIGH LEVEL SUPPLY VOLTAGE vs LOW LEVEL SUPPLY VOLTAGE

Chip Dimensions and Pad Layout



Dimensions in parenthesis are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

METALLIZATION: Thickness: 11kÅ – 14kÅ, AL.

PASSIVATION: 10.4kÅ - 15.6kÅ, Silane

BOND PADS: 0.004 inches X 0.004 inches MIN

DIE THICKNESS: 0.0198 inches - 0.0218 inches

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.