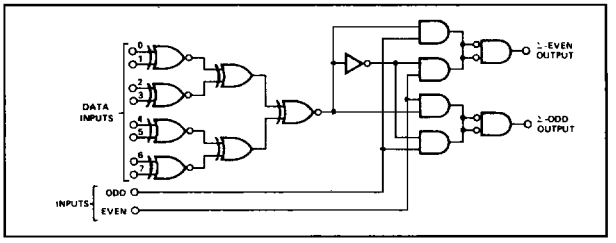
8-BIT ODD/EVEN PARITY GENERATOR/CHECKER 54/74180

SPEED/PACKAGE AVAILABILITY

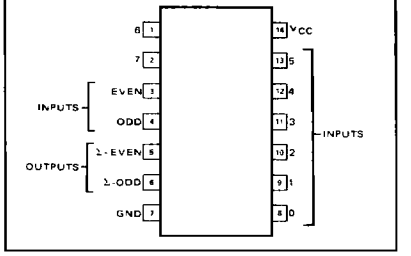
54 F,W 74 A

LOGIC DIAGRAM



PIN CONFIGURATION

A,F,W PACKAGE



SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 C_L=15pF R_L=400Ω			
PARAMETER		FROM INPUT	TO OUTPUT	MIN	TYP	MAX	UNIT
Propagation delay time					Odd input = OV		
t_{PLH}	Low-to-high	Data	ΣEven		40	60	ns
t_{PHL}	High-to-low				45	68	
t_{PLH}	Low-to-high	Data	ΣOdd		32	48	
t_{PHL}	High-to-low				25	38	
					Even input = OV		
t_{PLH}	Low-to-high	Data	ΣEven		32	48	
t_{PHL}	High-to-low				25	38	
t_{PLH}	Low-to-high	Data	ΣOdd		40	60	
t_{PHL}	High-to-low				45	68	
t_{PLH}	Low-to-high	Even, Odd	ΣEven,		13	20	
t_{PHL}	High-to-low		ΣOdd		7	10	

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

4-BIT ARITHMETIC LOGIC UNIT 54/74181

SPEED/PACKAGE AVAILABILITY

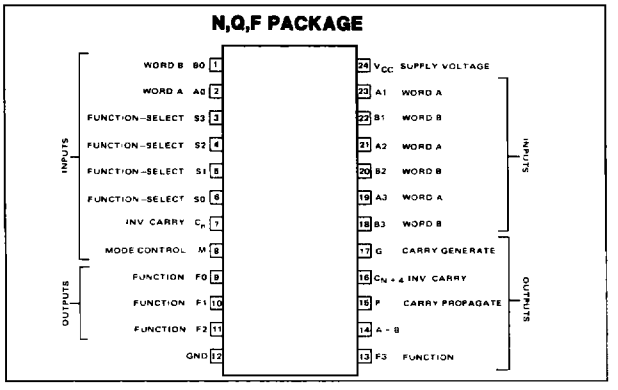
54 Q,F 74 N
54LS Q,F 74LS N
54S Q,F 74S N

TRUTH TABLE

INPUT C_n	OUTPUT C_{n+4}	ACTIVE-HIGH DATA (FIGURE1)	ACTIVE-LOW DATA (FIGURE 2)
H	H	A≤B	A≥B
H	L	A>B	A<B
L	H	A<B	A>B
L	L	A≥B	A≤B

PIN CONFIGURATION

N,Q,F PACKAGE



DESCRIPTION

The S54/N74LS181 arithmetic logic unit (ALU)/function generators have a complexity of 75 equivalent gates on a monolithic chip. These circuits perform 16 binary arithmetic operations on two 4-bit words as shown in Tables 1 and 2. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in these devices for fast, simultaneous carry generation by means of two cascade-outputs (pins 15 and 17) for the four bits in the package. When used in conjunction with the 182 full carry look-ahead circuit, high-speed arithmetic operations can be performed.

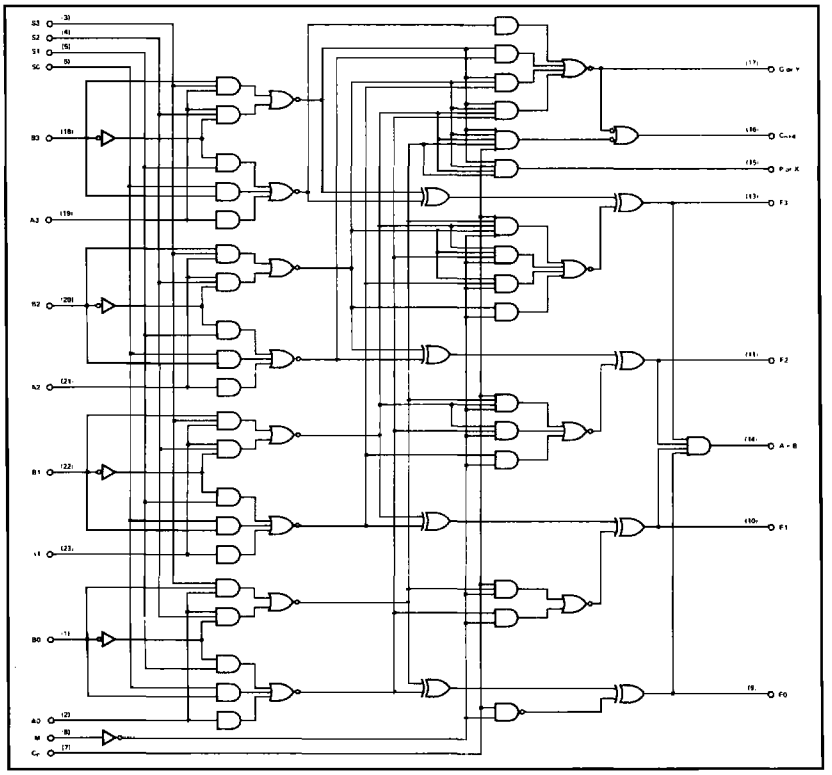
If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_n+4) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be performed without external circuitry.

The S54/N74LS181 will accommodate active-high or active-low data if the pin designations are interpreted as follows: Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A—B—1 which requires an end-around or forced carry to provide A—B.

The S54/74LS181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high level to indicate equality (A = B). The ALU should be in the subtract mode with C_n = H when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_n+4) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the function select inputs S3, S2, S1 S0 at L, H, H, L, respectively.

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode-control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in Tables 1 and 2 and include exclusive-OR, NAND, AND, NOR, and OR functions.

FUNCTIONAL BLOCK DIAGRAM



ALU SIGNAL DESIGNATIONS

The S54/N74LS181 can be used with the signal designations of either Figure 1 or Figure 2.

The logic functions and arithmetic operations obtained with signal designations as in Figure 1 are given in Table 1; those obtained with the signal designations of Figure 2 are given in Table 2.

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Table 1)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C}_n$	$\overline{C}_{n+4}$	X	Y
Active-low data (Table 2)	$\overline{A}_0$	$\overline{B}_0$	$\overline{A}_1$	$\overline{B}_1$	$\overline{A}_2$	$\overline{B}_2$	$\overline{A}_3$	$\overline{B}_3$	$\overline{F}_0$	$\overline{F}_1$	$\overline{F}_2$	$\overline{F}_3$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

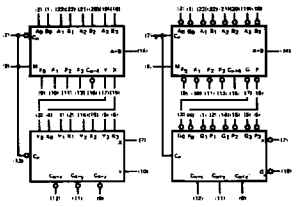


FIGURE 1 (FOR TABLE 1)

FIGURE 2 (FOR TABLE 2)

TABLE 1

SELECTION				ACTIVE-HIGH DATA		
				M=H	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n=H (NO CARRY)	C_n=L (WITH CARRY)
L	L	L	L	$F=\overline{A}$	F=A	F=A PLUS 1
L	L	L	H	$F=\overline{A+B}$	F=A+B	F=(A+B) PLUS 1
L	L	H	L	$F=\overline{A}B$	$F=A+\overline{B}$	$F=(A+\overline{B})$ PLUS 1
L	L	H	H	F=0	F=MINUS 1 (2's COMPL)	F=ZERO
L	H	L	L	$F=\overline{AB}$	$F=A$ PLUS $A\overline{B}$	$F=A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F=\overline{B}$	F=(A+B) PLUS $A\overline{B}$	F=(A-B) PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F=A \oplus B$	F=A MINUS B MINUS 1	F= A MINUS B
L	H	H	H	$F=A\overline{B}$	F=$A\overline{B}$ MINUS 1	F=$A\overline{B}$
H	L	L	L	$F=\overline{A}+B$	F=A PLUS AB	F=A PLUS AB PLUS 1
H	L	L	H	$F=\overline{A \oplus B}$	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	F=(A+$\overline{B}$) PLUS AB	F=(A+$\overline{B}$) PLUS AB PLUS 1
H	L	H	H	F=AB	F=AB MINUS 1	F=AB
H	H	L	L	F=1	F=A PLUS A*	F=A PLUS A PLUS 1
H	H	L	H	$F=A+\overline{B}$	F=(A+B) PLUS A	F=(A+B) PLUS A PLUS 1
H	H	H	L	F=A+B	F=(A+$\overline{B}$) PLUS A	F=(A+$\overline{B}$) PLUS A PLUS 1
H	H	H	H	F=A	F=A MINUS 1	F=A

*Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-LOW DATA		
				M=H	M=L: ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	C_n=L (NO CARRY)	C_n=H (WITH CARRY)
L	L	L	L	$F=\overline{A}$	F=A MINUS 1	F=A
L	L	L	H	$F=\overline{AB}$	F=AB MINUS 1	F=AB
L	L	H	L	$F=\overline{A}+B$	$F=A\overline{B}$ MINUS 1	$F=A\overline{B}$
L	L	H	H	F=1	F=MINUS 1 (2's COMPL)	F=ZERO
L	H	L	L	$F=\overline{A+B}$	F=A PLUS $(A+\overline{B})$	F=A PLUS $(A+\overline{B})$ PLUS 1
L	H	L	H	$F=\overline{B}$	F=AB PLUS $(A+\overline{B})$	F=AB PLUS $(A+\overline{B})$ PLUS 1
L	H	H	L	$F=\overline{A \oplus B}$	F=A MINUS B MINUS 1	F=A MINUS B
L	H	H	H	$F=A+\overline{B}$	$F=A+\overline{B}$	F=$(A+\overline{B})$ PLUS 1
H	L	L	L	$F=\overline{A}B$	F=A PLUS (A+B)	F=A PLUS (A+B) PLUS 1
H	L	L	H	$F=A \oplus B$	F=A PLUS B	F=A PLUS B PLUS 1
H	L	H	L	F=B	$F=A\overline{B}$ PLUS (A+B)	$F=A\overline{B}$ PLUS (A+B) PLUS 1
H	L	H	H	F=A+B	F=A+B	F=(A+B) PLUS 1
H	H	L	L	F=0	F=A PLUS A*	F=A PLUS A PLUS 1
H	H	L	H	$F=A\overline{B}$	F=AB PLUS A	F=AB PLUS A PLUS 1
H	H	H	L	F=AB	$F=A\overline{B}$ PLUS A	$F=A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F=A	F=A	F=A PLUS 1

LOGIC

SWITCHING CHARACTERISTICS V_{CC} = 5V, T_A = 25°C

TEST CONDITIONS				54/74 M=0V S0=S3=4.5V S1=S2=0V *S0=S3=0V *S1=S2=4.5V			54/74LS M=0V S0=S3=4.5V S1=S2=0V *S0=S3=0V *S1=S2=4.5V			54/74S M=0V S0=S3=4.5V S1=S2=0V *S0=S3=0V *S1=S2=4.5V			
PARAMETER		**FROM INPUT**	**TO OUTPUT**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNIT**
Propagation delay time													
t_{PLH}	Low-to-high	C_n	C_{N+4}		12	18		18	27		7	10.5	ns
t_{PHL}	High-to-low				13	19		13	20		7	10.5	
t_{PLH}	Low-to-high	C_n	Any F		13	19		17	26		7	12	
t_{PHL}	High-to-low	SUM or DIFF Mode			12	18		13	20		7	12	
t_{PLH}	Low-to-high	Any A, B SUM Mode	G		13	19		19	29		8	12	
t_{PHL}	High-to-low				13	19		15	23		7.5	12	
t_{PLH}	Low-to-high	*Any A,B DIFF Mode	G		17	25		21	32		10.5	15	
t_{PHL}	High-to-low				17	25		17	26		10.5	15	
t_{PLH}	Low-to-high	Any A,B SUM Mode	P		13	19		20	30		7.5	12	
t_{PHL}	High-to-low				17	25		20	30		7.5	12	
t_{PLH}	Low-to-high	*Any A,B DIFF Mode	P		17	25		20	30		10.5	15	
t_{PHL}	High-to-low				17	25		22	33		10.5	15	
t_{PLH}	Low-to-high	Any A,B SUM Mode	Any F		28	42					11	16.5	
t_{PHL}	High-to-low				21	32					11	16.5	
t_{PLH}	Low-to-high	*Any A,B DIFF Mode	Any F		32	48					14	20	
t_{PHL}	High-to-low				23	34					14	22	
t_{PLH}	Low-to-high	*Any A,B DIFF Mode	A = B		35	50		33	50		15	23	
t_{PHL}	High-to-low				32	48		41	62		20	30	
t_{PLH}	Low-to-high	Any A,B SUM Mode	C_{n+4}					25	38		12.5	18.5	
t_{PHL}	High-to-low							25	38		12.5	18.5	
t_{PLH}	Low-to-high	*Any A,B DIFF Mode	C_{n+4}					27	41		15.5	23	
t_{PHL}								27	41		15.5	23	
t_{PLH}	Low-to-high	A_i,B_i SUM Mode	F_i					21	32				
t_{PHL}	High-to-low							13	20				
t_{PLH}	Low-to-high	*A_i,B_i DIFF Mode	F_i					21	32				
t_{PHL}	High-to-low							15	23				
				M=4.5V						M=4.5V			
t_{PLH}	Low-to-high	Any A,B Logic Mode	Any F		32	48					14	20	
t_{PHL}	High-to-low				23	34					14	22	
							M = 4.5V						
t_{PLH}	Low-to-high	A_i,B_i Logic Mode	F_i					22	33				
t_{PHL}	High-to-low							19	29				

Load circuit and typical waveforms are shown at the front of section.