MSM6389

1,048,576-WORD x 1-BIT SOLID STATE RECORDER DATA REGISTER

GENERAL DESCRIPTION

MSM6389 is a solid state recorder data register in 1,048,576 words x 1 bit configuration.

MSM6389 has a built-in internal address generator circuit allowing continuous serial read/write operation by single external clock input. The internal address is automatically incremented or decremented by one by read/write operation. Address increment or decrement can be selected by external input.

Address designation in units of 1024 words in the direction of words is possible by an external serial address input.

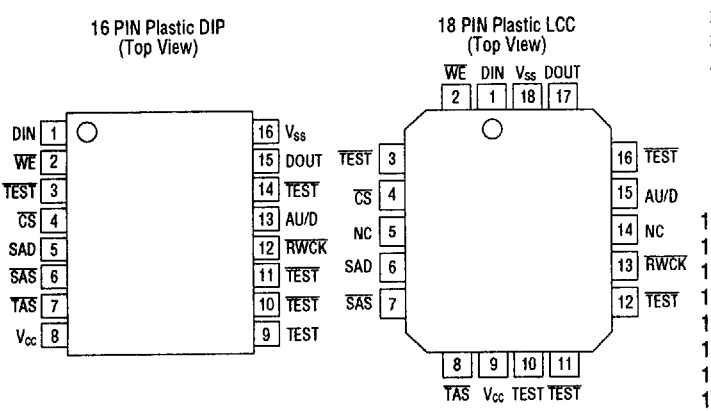
18-pin plastic QFJ (PLCC) is used as the pack are and the operating temperature range is between 0°C and 70°C.

MSM6389 is suitable for storing large capacity data with battery backup. A solid state recording and playback system can easily be built-in combination with OKI's voice synthesizer LSIs, MSM6388 and MSM6588.

FEATURES

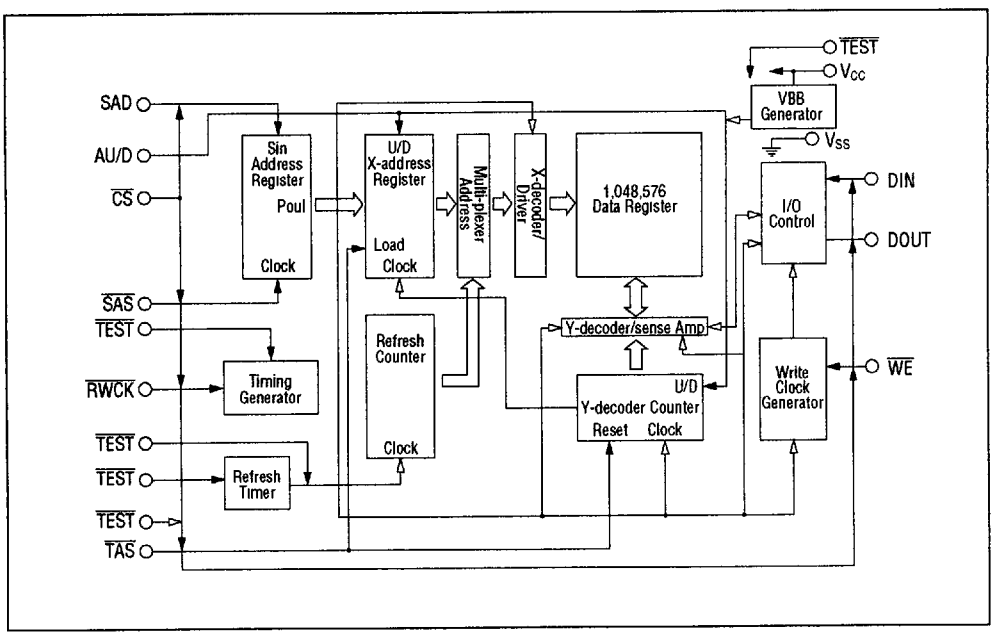
- Configuration: 1,048,576 x 1 bit
- Serial access operation:
  - Serial access time 3.0μs
  - Serial read/write cycle time 4.0μs
- Low current consumption:
  100 μA max. (for data holding, V_{CC}=4.0V)
- Wide operating supply voltage range:
  Single 3.5 to 5.5V
- Refresh operation:
  Self-refresh (refresh-free)
- 18-pin Plastic QFJ (PLCC)
  (QFJ18-P-R290)
- 16-pin Plastic DIP
  (DIP16-P-300-W1)

PIN CONFIGURATION



1 : Data input
2 : Write enable
3 : Test input
4 : Chip select
5 : No connection
6 : Serial address data
7 : Serial address strobe
8 : Transfer address strobe
9 : Power supply (+5V)
10 : Test input
11 : Test input
12 : Test input
13 : Read/write clock
14 : No connection
15 : Address up/down select
16 : Test input
17 : Data output
18 : Ground (0V)

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTIC

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Terminal voltage	V_T	T_a = 25°C, relative to V_{SS}	−1.0 ~ +7.0	V
Output short-circuit current	I_{OS}	T_a = 25°C	50	mA
Power dissipation	P_D	T_a = 25°C	1	W
Operating temperature	T_{OP}	—	0 ~ +70	°C
Storage temperature	T_{stg}	—	−55 ~ +150	°C

Recommended Operating Conditions

(Ta = 0 ~ +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Terminal voltage	V_{CC}	3.5	5.0	5.5	V
Terminal voltage	V_{SS}	0	0	0	V
"H" input voltage	V_{IH}	V_{CC} − 0.5	V_{CC}	V_{CC} + 0.5	V
"L" input voltage	V_{IL}	−0.5	0	0.5	V

DC Characteristics

(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

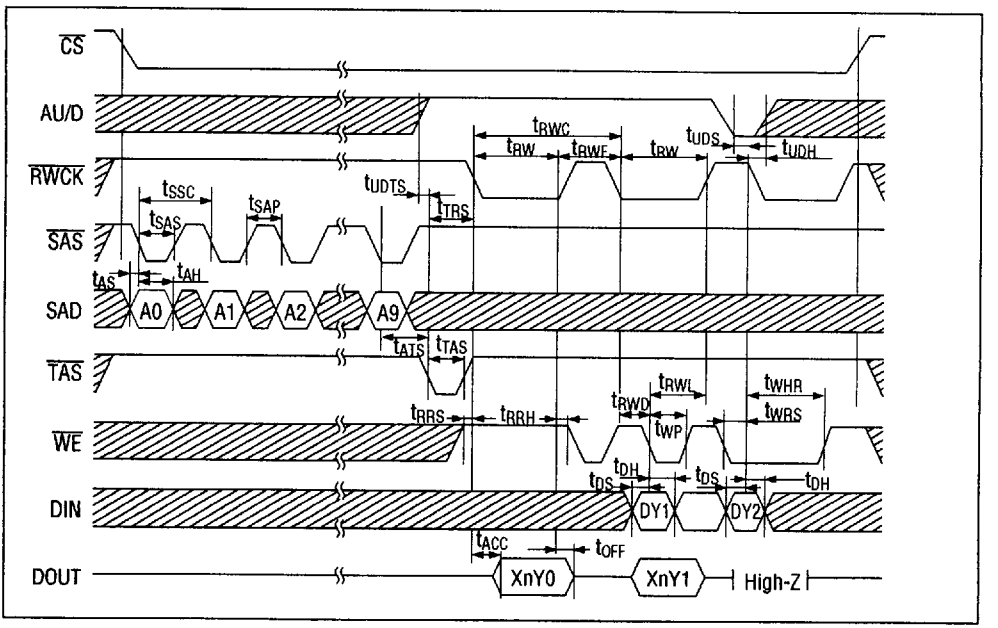
Parameter	Symbol	Conditions	Min.	Max.	Unit
"H" output voltage	V_{OH}	I_{OH} = −0.5mA	V_{CC} − 0.5	—	V
"L" output voltage	V_{OL}	I_{OL} = 0.5mA	—	0.4	V
Input leakage current	I_{LI}	V_I = 0V ~ V_{CC}	−1	1	µA
Output leakage current	I_{LO}	V_O = 0V ~ V_{CC}	−10	10	µA
Supply current (in operating state)	I_{CC1}	V_{CC} = 4V, t_{RC} = 4µs	—	5	mA
Supply currnet (in standby state)	I_{CC2}	V_{CC} = 4V	—	100	µA

• AC Characteristics

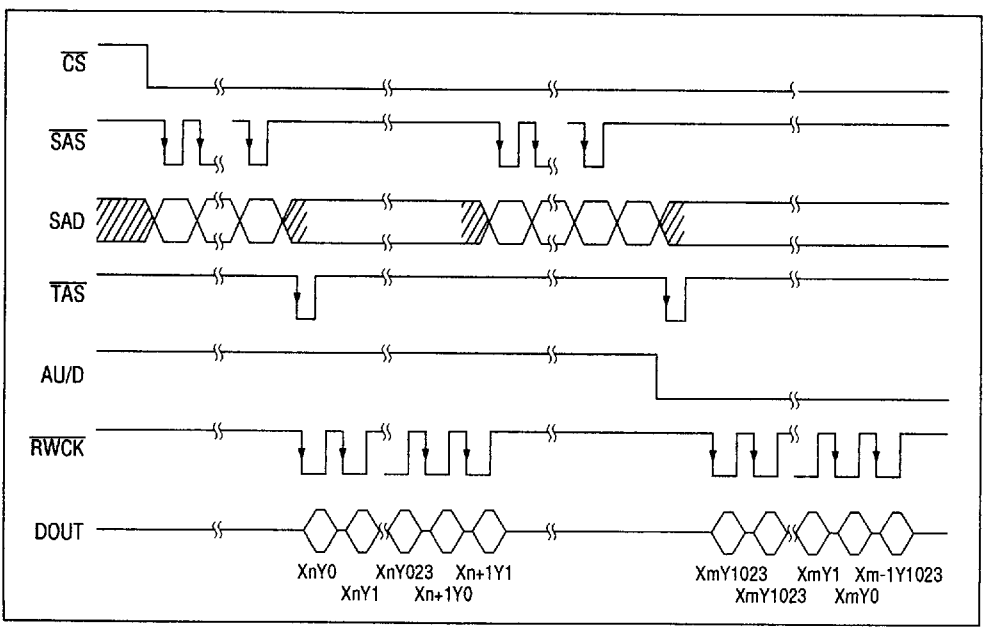
(V_{CC} = 3.5V ~ 5.5V, Ta=0~+70°C)

Parameter	Symbol	Min.	Max.	Unit
Refresh cycle	t_{REF}	—	—	ms
Read/write cycle time	t_{RWC}	4,000	—	ns
Access time	t_{ACC}	—	3,000	ns
Output turn off delay time	t_{OFF}	0	50	ns
Input signal rise/fall time	t_T	3	50	ns
$\overline{RWCK}$ precharge time	t_{RWP}	1,000	—	ns
$\overline{RWCK}$ pulse width	t_{RW}	3,000	10,000	ns
$\overline{SAS}$ cycle time	t_{SSC}	100	—	ns
$\overline{SAS}$ pulse width	t_{SAS}	50	—	ns
$\overline{SAS}$ precharge time	t_{SAP}	50	—	ns
Address setup time	t_{AS}	0	—	ns
Address hold time	t_{AH}	50	—	ns
$\overline{TAS}$ setup time	t_{ATS}	50	—	ns
$\overline{TAS}$ to $\overline{RWCK}$ setup time	t_{TRS}	50	—	ns
$\overline{TAS}$ pulse width	t_{TAS}	50	—	ns
Read command setup time	t_{RRS}	0	—	ns
Read command hold time	t_{RRH}	250	—	ns
Write command setup time	t_{WRS}	0	—	ns
Write command hold time	t_{WRH}	50	—	ns
Write command pulse width	t_{WP}	50	—	ns
Write command to $\overline{RWCK}$ lead time	t_{RWL}	50	—	ns
Data setup time	t_{DS}	0	—	ns
Data hold time	t_{DH}	50	—	ns
$\overline{RWCK}$ to $\overline{WE}$ delay time	t_{RWD}	100	—	ns
AU/D setup time	t_{UDS}	0	—	ns
AU/D hold time	t_{UDH}	50	—	ns
AU/D to $\overline{TAS}$ setup time	t_{UDTS}	0	—	ns

Read/Write/Read Modify Write Cycle



Address Up/Down Select Mode



PIN FUNCTIONS AND OPERATION MODES

Pin	Function
SAD	(Serial Address Input) Pin for inputting the read/write starting address-Designation in units of 1024 words is possible. The 1,024 address data can be input as 10-bit (A0-A9) serial from the SAD pin.
$\overline{SAS}$	(Serial address strode) Pin for the clock used to store the serial address data into the internal register.
$\overline{TAS}$	(Address transfer strode) Input pin for setting the serial address data stored in the address register to the internal address counter. When the $\overline{TAS}$ falls, and the Y address is set to address 0 in the increment mode or to address 1023 in the decrement mode.
$\overline{RWCK}$	(Read/write clock) Input pin for the data register information read/write clock. Internal operation starts at the following edges of $\overline{RWCK}$. The information in the data register is output to the DOUT pin in the read mode, and the information at the DIN pin is written into the data register in the write mode. The internal address counter is automatically incremented or decremented also when $\overline{RWCK}$ falls.
$\overline{WE}$	(Write enable) Input pin for selecting the read mode, write mode or read modify write mode. The read mode is set when $\overline{WE}$ is "H", and the write mode is set when $\overline{WE}$ is "L". When $\overline{WE}$ falls from "H" to "L" while $\overline{RWCK}$ is active, the read modify write mode is set.
DIN	(Data input) Input pin for write data. The information at the data input pin is stored at the falling edge of $\overline{RWCK}$ in the write mode, and at the falling edge of $\overline{WE}$ in the read modify write mode.
DOUT	(Data output) The data output pin is always in kept in the high impedance state when $\overline{RWCK}$ or $\overline{CS}$ is kept at "H". When "H" or "L" information is read in the read operation, the output pin is set to "H" or "L" and holds the read information until $\overline{RWCK}$ is again set to "H". In the early write mode the output pin maintains the high impedance state, so I/O common operation by connecting DIN and DOUT is possible.
AU/D	(Address up/down select) Input pin for selecting the direction of automatic address updating. When the $\overline{TAS}$ signal is input with the AU/D pin set to "H", the internal address counters are set to the externally set address for X and to address 0 for Y. Then the address is incremented by 1 every time $\overline{RWCK}$ is input. When the $\overline{TAS}$ signal is input with the AU/D pin set to "L", the internal address counters are set to the externally set address in the same way for X but set to address 1023 for Y. Then the address is decremented by 1 every time $\overline{RWCK}$ is input. In either case, the X address is automatically incremented or decremented by 1 when read/write operation for 1024 words ends. The AU/D pin setting change is possible in any read/write cycle so long as the timing specifications for t_{UDS}, t_{UDH} are satisfied.
$\overline{CS}$	(Chip select) Input pin for disabling all input and output pins. This pin enables parallel use of multiple MSM6389s by connecting the data input and output pins.