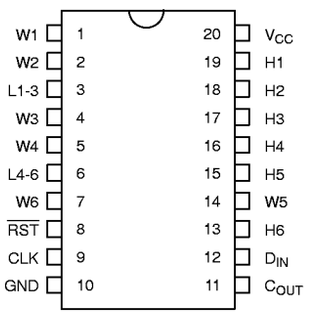
DALLAS SEMICONDUCTOR

DS1806
Digital Sextet Potentiometer

FEATURES

- Six digitally controlled 64–position potentiometers
- 3–Wire Serial Port provides for reading and setting each potentiometer
- Devices can be cascaded for single processor multi–device control
- Standard Resistance Values
  - DS1806–010 – 10K ohm
  - DS1806–050 – 50K ohm
  - DS1806–100 – 100K ohm
- Temperature:
  - Industrial: –40°C to +85° C

PIN ASSIGNMENT



DS1806 20–PIN DIP (300 MIL)
DS1806S 20–PIN SOIC (300 MIL)
DS1806E 20–PIN TSSOP (173 MIL)
See Mech. Drawings Section

PIN DESCRIPTION

V_{CC}	–	3V or 5V Supply
$\overline{RST}$	–	Serial Port Reset Input
D_{IN}	–	Serial Port Data Input
CLK	–	Serial Port Clock Input
C_{OUT}	–	Cascade Data Output
H1 – H6	–	High End Terminal of Pot
W1 – W6	–	Wiper Terminal of Pot
GND	–	Ground
L1–3	–	Low Terminal Pots 1 thru 3
L4–6	–	Low Terminal Pots 4 thru 6

DESCRIPTION

The DS1806 is a six–channel digitally controlled solid–state linear potentiometer. Each potentiometer is comprised of 63 equiresistive sections as illustrated in the block diagram of Figure 1. Each potentiometer has three terminals accessible to the user. These include the high side terminals, H_X, the wiper terminals, W_X, and the low–end terminals, L1–3 and L4–6. Potentiometers 1 through 3 share the same low–end terminal L1–3. And likewise, potentiometers 4 through 6 share the low–end terminal L4–6.

Each wiper's position is selected via an 8–bit register value. Communication and control of the device is accomplished via a 3–wire serial port interface. This interface in conjunction with a cascade output allows the value of the device wiper settings to be read.

For multiple device and single processor environments, the DS1806 can be cascaded or daisy chained. This feature allows a single processor to control multiple devices.

The DS1806 is available in 10K, 50K and 100K ohm versions and is specified over the industrial temperature range. Packages for the device include 20–lead DIPs, SOICs, and TSSOPs.

OPERATION

A block diagram of the device is provided in Figure 1. As shown, the DS1806 contains six 64–position potentiometers whose wiper positions are set by an 8–bit value. The DS1806 contains a 48–bit I/O shift register which is used to store the respective wiper position data for each of the six potentiometers.

Each potentiometer has three terminals accessible to the user. These include the high side terminals, H_X, the wiper terminals, W_X, and the low–end terminals, L1–3 and L4–6. Potentiometers 1 through 3 share the same low–end terminal L1–3. And likewise, potentiometers 4 through 6 share the low–end terminal L4–6.

Control of the DS1806 is accomplished via a 3–wire serial communication interface which allows the user to set the wiper position value for each potentiometer. The 3–wire serial interface consists of the control signals $\overline{RST}$, D_{IN}, and CLK. On power–up, the wiper positions of each potentiometer are set to the low–end terminal L_X (00000000).

The $\overline{RST}$ control signal is used to enable 3–wire serial port operation. The $\overline{RST}$ signal (3–wire serial port) is active when in a high state. Any communication intended to change wiper settings must begin with the transition of the $\overline{RST}$ from the low–state to the high–state.

The CLK signal input is used to provide timing synchronization for data input and output. Wiper position data is loaded into the DS1806 through the D_{IN} input terminal. This data is shifted one bit at a time into the 48–bit I/O shift register of the part, LSB first. Figure 3 provides an illustration of the 48–bit shift register.

Figure 4 provides 3–wire serial port protocol and timing diagrams. As shown, the 3–wire port is inactive when the $\overline{RST}$ signal input is low. Once $\overline{RST}$ has transitioned from the low to the high state, the serial port becomes active. When active, data is loaded into the I/O shift register on the low–to–high transition of the CLK.

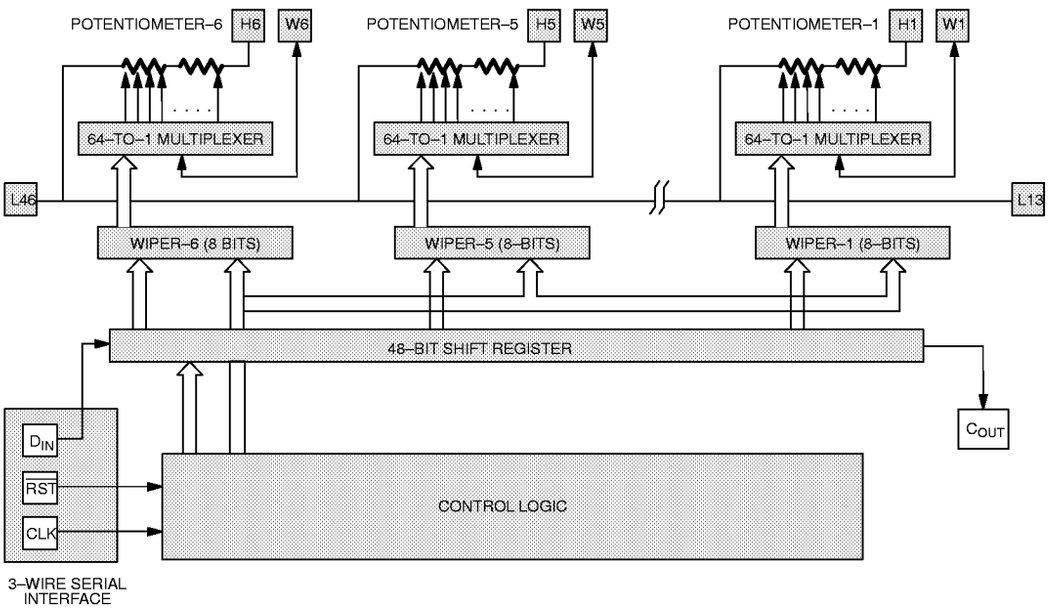
Data is transmitted in order of LSB first. Potentiometers are designated from 1 through 6 and the value for potentiometer–1 will be the first data entered into the shift register, followed by that of potentiometer–2 and so forth.

Each wiper has an 8–bit register which is used for setting the position of the wiper on the resistor array. Because the DS1806 is a 64–position potentiometer, only six bits of information are needed to set wiper position. The remaining two bits of information are used to provide a “don’t change” feature. Wiper position is controlled by bit positions 0 through 5 of each register. The “don’t change” feature is controlled by bits 6 and 7 of each register. When bits 6 and 7 have value “11 xxxxxx”, wiper position will not change regardless of the states of bits 0 through 5. If bits 6 and 7 are set to any other value, bits 0 through 5 will be used as the new wiper position. The “don’t change” feature allows the user to change the value of any potentiometer of the DS1806 without affecting or having to remember the remaining positions of the potentiometer wipers. Figure 2 provides the format for a wiper’s register.

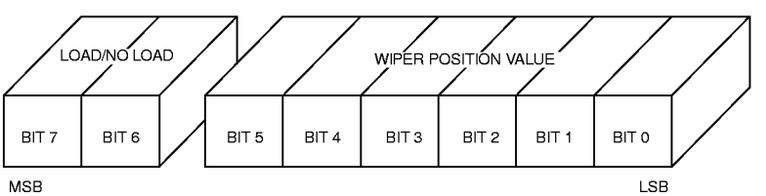
Wiper placement for each potentiometer is such that position–63 corresponds to the H_X terminal of the device while position–0 corresponds to the ground terminal. For example, to set a potentiometer’s wiper position to 15 (decimal), the binary value shifted into the wiper register should be 00001111. This will place the wiper tap at the 15th step above the low end terminal, L_X.

All communication transactions should provide the total 48 bits of information when writing or reading from the part. This is especially true for applications using all six potentiometers. If a complete set of 48 bits is not transmitted to the part, undesired wiper position settings may occur.

DS1806 BLOCK DIAGRAM Figure 1



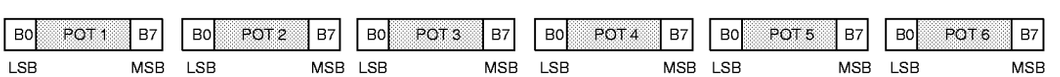
WIPER REGISTER CONFIGURATION Figure 2



Bits 6 and 7 Functionality

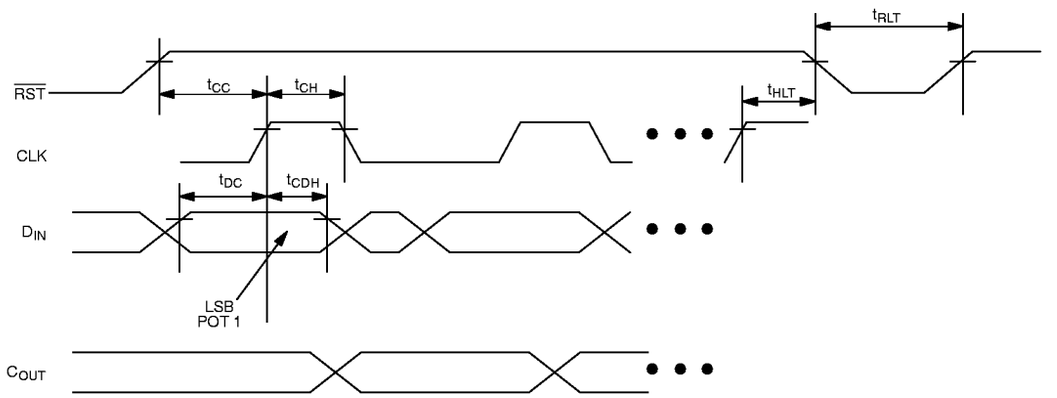
11 – Do not load wiper value
10 – Load wiper value
01 – Load wiper value
00 – Load wiper value

48–BIT I/O SHIFT REGISTER Figure 3



Data entered LSB first, starting with potentiometer–1.

3–WIRE SERIAL PORT TIMING Figure 4



CASCADE OPERATION

A feature of the DS1806 is the ability to control multiple devices from a single processor. Multiple DS1806s can be linked or daisy chained as shown in Figure 5. As a data bit is entered into the I/O shift register of the DS1806, a bit will appear at the C_{OUT} terminal before a maximum delay of 50 nanoseconds. The LSB of potentiometer–1 will always be the first out of the part at the beginning of a transaction. Additionally, the C_{OUT} terminal is always active regardless of the state $\overline{RST}$. However, D_{IN} and CLK inputs are ignored when $\overline{RST}$ is in the low state.

The C_{OUT} output of the DS1806 can be used to drive the D_{IN} input of another DS1806. When cascading multiple devices, the total number of bits transmitted is always 48 multiplied by the total number of DS1806s being cascaded.

An optional feedback resistor can be placed between the C_{OUT} terminal of the last device and the first DS1806 D_{IN} input, which allows the controlling processor to read, as well as, write data, or circularly clock data through the daisy chain. The value of the feedback or isolation resistor should be in the range from 1KΩ to 10KΩ.

To read data, the reading device configures itself as an input and monitors the state of the D_{IN} line, which is driven by C_{OUT} through the isolation resistor. When $\overline{RST}$ is driven high, bit 48 is present on the C_{OUT} pin, which is fed back to the input D_{IN} pin through the isolation resistor. When the CLK input transitions low to high, bit 48 is loaded into the first position of the I/O shift register and bit 47 becomes present on C_{OUT} and D_{IN} of the next device. After 48 bits (or 48 times the number of the DS1806s in the daisy chain), the data has shifted completely around and back to its original position. When $\overline{RST}$ transitions to the low state to end data transfer, the value (the same as before the read occurred) is loaded in the shift register.

ABSOLUTE AND RELATIVE LINEARITY

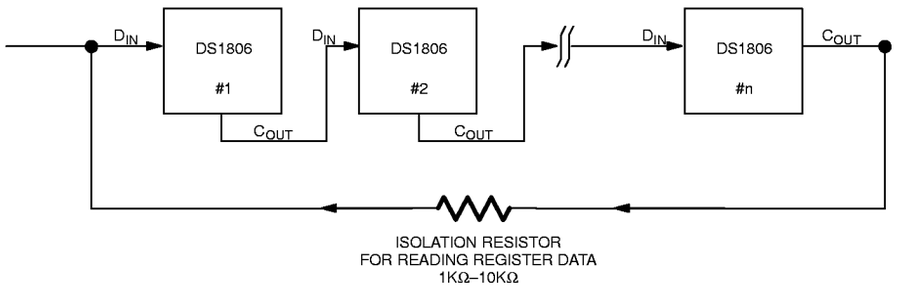
Absolute linearity is defined as the difference between the actual measured output voltage and the expected output voltage. Absolute linearity is given in terms of a minimum increment or expected output when the wiper is moved one position. The DS1806 is specified to have an absolute linearity of ±0.50 LSB.

Relative linearity is a measure of error between two adjacent wiper position points. The DS1806 is specified to have a relative linearity of ±0.25 LSB.

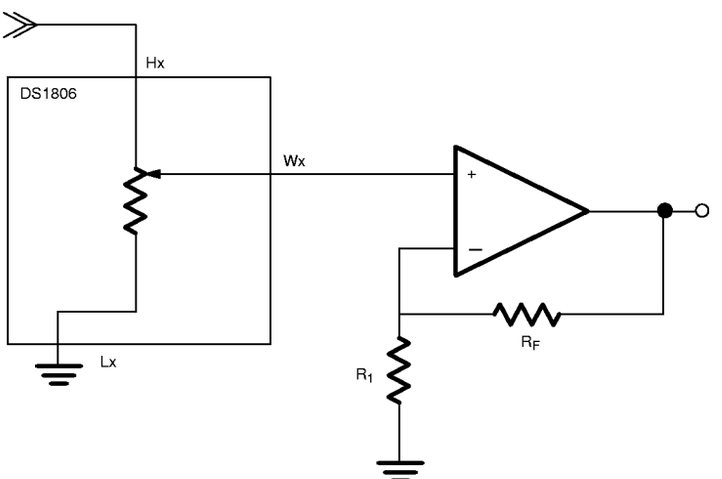
TYPICAL APPLICATION CONFIGURATIONS

Figure 6 shows the typical application configuration of the DS1806 as a fixed gain attenuator. In this configuration, the DS1806 adjusts the attenuation level of the incoming signal. Variations in wiper resistance are minimized by connecting the wiper terminal of the part to a high impedance load. Depending on voltage across the wiper, its resistance may vary from 400 ohms to 1000 ohms. Note that the resistance R1 in Figure 6 should be chosen to be much greater than the wiper resistance R_W.

CASCADING MULTIPLE DEVICES Figure 5



FIXED GAIN ATTENUATOR Figure 6



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to Ground	–0.5V to +7.0V
Operating Temperature	–40°C to +85°C; industrial
Storage Temperature	–55°C to +125°C
Soldering Temperature	260°C for 10 seconds

* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(-40°C to +85°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_{CC}	+2.7		5.5	V	1

DC ELECTRICAL CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Supply Current Active	I_{CC}		1.3	2	mA	
Input Leakage	I_{IL}	–1		+1	µA	
Wiper Resistance	R_W		400	1000	Ω	
Wiper Current	I_W			1	mA	
Input Logic 1	V_{IH}	2.0		V_{CC}+0.5	V	1
Input Logic 0	V_{IL}	–0.5		+0.8 +0.6	V	1, 6
Logic 1 Output @ 2.4 Volts	I_{OH}	–1			mA	
Logic 0 Output @ 0.4 Volt	I_{OL}			4	mA	6
Standby Current: 3 Volts 5 Volts	I_{STBY}		12 20	 40	µA µA	9
Resistor Inputs	H_X, L_X, W_X	GND –0.5		V_{CC} +0.5	µA	2

ANALOG RESISTOR CHARACTERISTICS

(–40°C to +85°C; V_{CC} = 2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
End–to–End Resistor Tolerance		–20		+20	%	
Absolute Linearity		–0.5		+0.5	LSB	7
Relative Linearity		–0.25		+0.25	LSB	8
–3 dB Cutoff Frequency	I_{cutoff}				Hz	4
Temperature Coefficient			650		PPM/°C	

CAPACITANCE

(t_A = 25°C)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	C_{IN}			5	pF	3
Output Capacitance	C_{OUT}			7	pF	3

AC ELECTRICAL CHARACTERISTICS

(-40°C to +85°C; V_{CC} = 2.7 to 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency	f_{CLK}	DC		10	MHZ	5
Width of CLK Pulse	t_{CH}	50			ns	5
Data Setup Time	t_{DC}	30			ns	5
Data Hold Time	t_{CDH}	0			ns	5
Propagation Delay Time Low to High Level Clock to Output	t_{PLH}			50	ns	5
$\overline{RST}$ High to Clock Input High	t_{CC}	50			ns	5
$\overline{RST}$ Low from lock Input High	t_{HLT}	50			ns	5
$\overline{RST}$ Inactive	t_{RLT}	125			ns	5
CLK Rise Time, CLK Fall Time	t_{CR}			50	ns	5

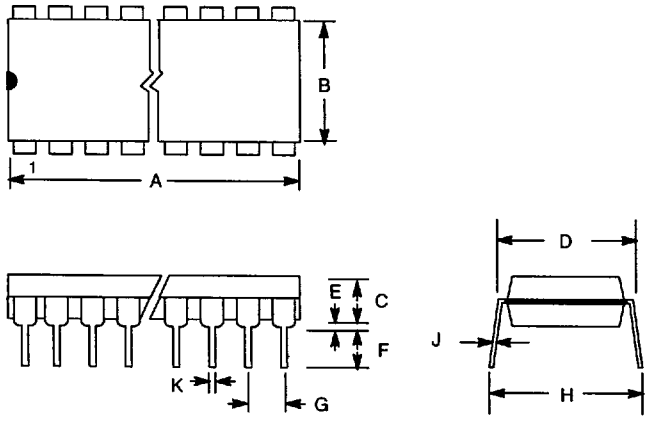
NOTES:

1. All voltages are referenced to ground.
2. Resistor inputs cannot go below GND by more than 0.5 volts or above V_{CC} by 0.5 volts in the positive direction.
3. Capacitance values apply at 25°C.
4. –3 dB cutoff frequency characteristics for the DS1806 depend on potentiometer total resistance: DS1806–010; 1 MHz; DS1806–050; 200 KHz, DS1806–100; 100 KHz.
5. See Figure 4.
6. For V_{CC} = 5V ± 10% maximum V_{IL} = +0.8V. For V_{CC} = 3.0 ± 10% V_{IL} = +0.6V.
7. Absolute Linearity is to used measure expected wiper voltage versus measured wiper voltage as determined by wiper position. The DS1806 is specified to provide an Absolute Linearity of +0.5 LSB.
8. Relative Linearity is used to determine the change in wiper voltage between two adjacent wiper positions. The DS1806 is specified to provide a relative linearity of +0.25 LSB.
9. Standby current levels apply when all inputs are driven to appropriate supply levels.

DS1806 ORDERING INFORMATION

ORDERING NUMBER	PACKAGE	OPERATING TEMPERATURE	VERSION
DS1806–010	20L DIP	–40°C TO +85°C	10KΩ
DS1806–050	20L DIP	–40°C TO +85°C	50KΩ
DS1806–100	20L DIP	–40°C TO +85°C	100KΩ
DS1806E–010	20L TSSOP (173 MIL)	–40°C TO +85°C	10KΩ
DS1806E–050	20L TSSOP (173 MIL)	–40°C TO +85°C	50KΩ
DS1806E–100	20L TSSOP (173 MIL)	–40°C TO +85°C	100KΩ
DS1806S–010	20L SOIC (300 MIL)	–40°C TO +85°C	10KΩ
DS1806S–050	20L SOIC (300 MIL)	–40°C TO +85°C	50KΩ
DS1806S–100	20L SOIC (300 MIL)	–40°C TO +85°C	100KΩ

8– TO 28–PIN DIP (300 MIL)



Includes:

DS1000	DS1211	DS1621
DS1000M	DS1215	DS1625
DS1003	DS1221	DS1632
DS1003M	DS1222	DS1640
DS1004M	DS1228	DS1651
DS1005	DS1229	DS1652
DS1005M	DS1231	DS1652B
DS1007	DS1232	DS1653
DS1010	DS1232LP	DS1666
DS1012M	DS1234	DS1667
DS1013	DS1236	DS1669
DS1013M	DS1237	DS1802
DS1020	DS1238	DS1830
DS1033M	DS1239	DS1832
DS1035M	DS1259	DS1867
DS1040M	DS1267	DS1868
DS1044	DS1275	DS1869
DS1045	DS1291	DS2009D
DS1200	DS1293	DS2010D
DS1206	DS1336	DS2011D
DS1210	DS1620	DS2013D

PKG	8-PIN		10-PIN		14-PIN		16-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.360	0.400	0.480	0.520	0.740	0.780	0.740	0.780
MM	9.14	10.16	12.19	13.21	18.80	19.81	18.80	19.81
B IN.	0.240	0.260	0.240	0.260	0.240	0.260	0.240	0.260
MM	6.10	6.60	6.10	6.60	6.10	6.60	6.10	6.60
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.300	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.62	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.040
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.02
F IN.	0.120	0.140	0.110	0.130	0.120	0.140	0.120	0.140
MM	3.04	3.56	2.79	3.30	3.04	3.56	3.04	3.56
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.29	2.79	2.29	2.79	2.29	2.79	2.29	2.79
H IN	0.320	0.370	0.320	0.370	0.320	0.370	0.320	0.370
MM	8.13	9.40	8.13	9.40	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.021	0.015	0.021
MM	0.38	0.53	0.38	0.53	0.38	0.53	0.38	0.53

Continued on following page.

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MECHANICAL DRAWINGS

PKG	18-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN.	0.890	0.920	0.970	1.040	1.150	1.260	1.345	1.370
MM	22.61	23.36	24.63	26.42	29.21	32.00	34.16	34.80
B IN.	0.240	0.260	0.240	0.270	0.250	0.270	0.270	0.295
MM	6.10	6.60	6.09	6.86	6.35	6.86	6.85	7.49
C IN.	0.120	0.140	0.120	0.140	0.120	0.140	0.120	0.140
MM	3.05	3.56	3.05	3.56	3.05	3.56	3.05	3.56
D IN.	0.300	0.325	0.295	0.325	0.300	0.325	0.300	0.325
MM	7.62	8.26	7.49	8.26	7.62	8.26	7.62	8.26
E IN.	0.015	0.040	0.015	0.040	0.015	0.040	0.015	0.050
MM	0.38	1.02	0.38	1.02	0.38	1.02	0.38	1.27
F IN.	0.120	0.140	0.120	0.140	0.125	0.135	0.125	0.135
MM	3.04	3.56	3.04	3.56	3.18	3.48	3.18	3.48
G IN.	0.090	0.110	0.090	0.110	0.090	0.110	0.090	0.110
MM	2.23	2.79	2.23	2.79	2.23	2.79	2.23	2.79
H IN	0.320	0.370	0.310	0.390	0.320	0.370	0.320	0.370
MM	8.13	9.40	7.87	9.91	8.13	9.40	8.13	9.40
J IN	0.008	0.012	0.008	0.012	0.008	0.012	0.008	0.012
MM	0.20	0.30	0.20	0.30	0.20	0.30	0.20	0.30
K IN.	0.015	0.021	0.015	0.021	0.015	0.022	0.015	0.022
MM	0.38	0.53	0.38	0.53	0.38	0.56	0.38	0.56

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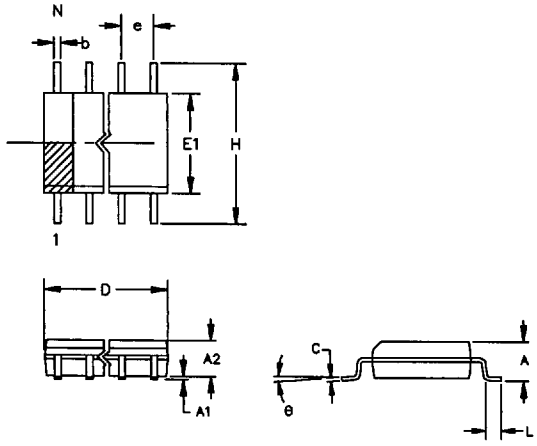
16–, 20–, 24–, 28–PIN SOIC (300 MIL)



Includes:

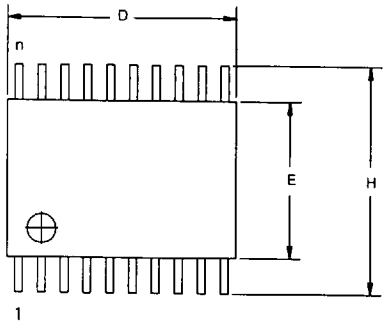
DS1000S	DS1227S	DS1360S
DS1005S	DS1231S	DS1380S
DS1007S	DS1228S	DS1609S
DS1010S	DS1229S	DS1610S
DS1013S	DS1232S	DS1620
DS1020S	DS1232LPS	DS1632S
DS1021S	DS1234S	DS1640S
DS1045S	DS1236S	DS1653S
DS1200S	DS1237S	DS1710S
DS1205S	DS1238S	DS2107AS
DS1206	DS1239S	DS2107S
DS1209S-B1	DS1259S	DS2175S
DS1210S	DS1267S	DS2186S
DS1211S	DS12885S	DS2187S
DS1215S	DS1336S	DS2188S
DS1221S	DS1359S	
DS1222S		

The chamfer on the body is optional. If it is not present, a terminal 1 identifier must be positioned so that 1/2 or more of its area is contained in the hatched zone.

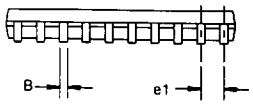
PKG	16-PIN		20-PIN		24-PIN		28-PIN	
DIM	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A IN. MM	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.38	0.105 2.68	0.094 2.39	0.105 2.67
A1 IN. MM	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30	0.004 0.102	0.012 0.30
A2 IN. MM	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41	0.089 2.26	0.095 2.41
b IN. MM	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51	0.013 0.33	0.020 0.51
C IN MM	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33	0.009 0.229	0.013 0.33
D IN. MM	0.398 10.11	0.412 10.46	0.498 12.65	0.511 12.99	0.598 15.19	0.612 15.54	0.698 17.73	0.712 18.08
e IN. MM	0.050 BSC 1.27 BSC						0.050 BSC 1.27 BSC	
E1 IN. MM	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62	0.290 7.37	0.300 7.62
H IN MM	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57	0.398 10.11	0.416 10.57
L IN MM	0.016 0.40	0.040 1.02	0.016 0.406	0.040 1.20	0.016 0.40	0.040 1.02	0.016 0.40	0.040 1.02
Θ	0°	8°	0°	8°	0°	8°	0°	8°

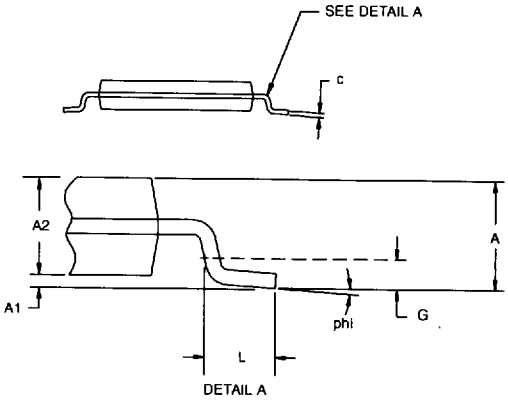
2614130 0014420 576

–14, –20–PIN TSSOP



14–PIN	20–PIN
DS1801	DS1033E
DS1803	DS1035E
DS1807	DS1802
	DS1867
	DS2430
	DS1267
	DS1806
	DS1800





DIM	14–PIN MIN	14–PIN MAX	20–PIN MIN	20–PIN MAX
A MM	–	1.10	–	1.10
A1 MM	0.05	–	0.05	–
A2 MM	0.75	1.05	0.75	1.05
C MM	0.09	0.18	0.09	0.18
L MM	0.50	0.70	0.50	0.70
e1 MM	0.65 BSC		0.65 BSC	
B MM	0.18	0.30	0.18	0.30
D MM	4.90	5.10	6.40	6.90
E MM	4.40 NOM		4.40 NOM	
G MM	0.25 REF		0.25 REF	
H MM	6.25	6.55	6.25	6.55
phi	0°	8°	0°	8°
n	14		20	

2614130 0014422 349