



Quint 2-Input AND/NAND Gate

Product Preview
ELECTRICALLY TESTED PER:
100E504

The 100E504 is a quint 2-input **AND/NAND** gate. The function output F is the OR of all five AND gate outputs, while \bar{F} is the NOR. The Q outputs need not be terminated if only the F outputs are to be used.

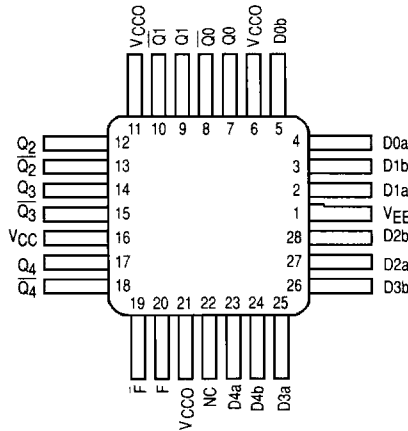
- 600 ps Max. Propagation Delay
- OR/NOR Function Outputs
- Extended 100E V_{EE} Range of - 4.2 V to - 5.46 V
- 75 k Ω Input Pulldown Resistors

PIN NAME

Pin	Function
D _{0a} - D _{4b}	Data Inputs
Q ₀ - Q ₄	AND Outputs
\bar{Q}_0 - \bar{Q}_4	NAND Outputs
F	OR Output
\bar{F}	NOR Output

FUNCTION OUTPUTS

$$F = (D_{0a} \cdot D_{0b}) + (D_{1a} \cdot D_{1b}) + (D_{2a} \cdot D_{2b}) + (D_{3a} \cdot D_{3b}) + (D_{4a} \cdot D_{4b})$$



Military 100E504

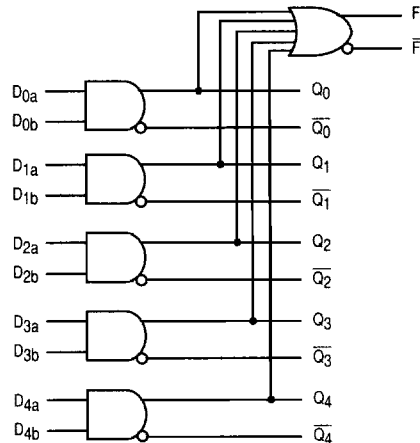


AVAILABLE AS

- 1) JAN: N/A
 - 2) SMD: N/A
 - 3) 883: Planned
- X = CASE OUTLINE AS FOLLOWS:

PACKAGE: NON-Compliant
QFP: X

LOGIC DIAGRAM



100E504

100E Series DC CHARACTERISTICS: $V_{EE} = -4.2 \text{ V to } -5.46 \text{ V}$, $V_{CC} = V_{CCO} = \text{GND}$; $-55^\circ\text{C to } +125^\circ\text{C}$

Symbol	Parameter	Min	Max	Units	TEST CONDITION APPLIED:	
V_{OH}	Output HIGH Voltage	-1025	-880	mV	$V_{IN} = V_{IH(\text{max})}$	Loading with
V_{OL}	Output LOW Voltage	-1810	-1620	mV	or $V_{IN} = V_{IL(\text{min})}$	50Ω to -2.0 V
V_{OHA}	Output HIGH Voltage	-1035		mV	$V_{IN} = V_{IH(\text{min})}$	Loading with
V_{OLA}	Output LOW Voltage		-1610	mV	or $V_{IN} = V_{IL(\text{max})}$	50Ω to -2.0 V
V_{IH}	Input HIGH Voltage	-1165	-880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input LOW Voltage	-1810	-1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IL}	Input LOW Current	0.5		μA	$V_{IN} = V_{IL(\text{min})}$	

DC CHARACTERISTICS: $V_{EE} = V_{EE(\text{min})}$ to $V_{EE(\text{max})}$, $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
		+ 25° C		+ 125° C		- 55° C			
		Min	Max	Min	Max	Min	Max		
I_{IH}	Input High Current		200		200		200	μA	
I_{EE}	Power Supply Current		46		53		46	mA	

AC CHARACTERISTICS: $V_{EE} = V_{EE(\text{min})}$ to $V_{EE(\text{max})}$, $V_{CC} = V_{CCO} = \text{GND}$

Symbol	Parameter	Limits						Units	TEST CONDITION APPLIED:
		+ 25° C		+ 125° C		- 55° C			
		Min	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay to Output D to Q D to F	225 500	600 1000	225 500	600 1000	225 500	600 1000	ps ps	
t_{Skew}	Within-device Skew D to Q	75		75		75		ps	(Note 1)
t_r t_f	Rise/Fall Times 20 - 80% Q F	275 300	700 700	275 300	700 700	275 300	700 700	ps ps	

1. Within-device skew is defined as identical transitions on similar paths through a device.