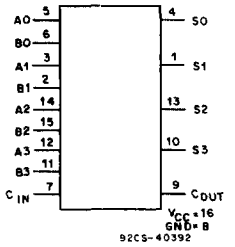
File Number **1848**

CD54/74HC283
CD54/74HCT283

High-Speed CMOS Logic



FUNCTIONAL DIAGRAM

4-Bit Binary Full Adder With Fast Carry

Type Features:

- *Adds two binary numbers*
- *Full internal lookahead*
- *Fast ripple carry for economical expansion*
- *Operates with both positive and negative logic*

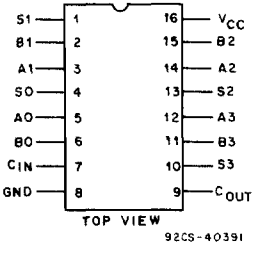
The RCA-CD54/74HC283 and CD54/74HCT283 are binary-full adders that add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

Because of the symmetry of the add function, this device can be used with either all active-High operands (positive logic) or with all active-Low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

The CD54HC/HCT283 are supplied in 16-lead hermetic dual-in-line frit seal ceramic packages (F suffix). The CD74HC/HCT283 are supplied in 16-lead dual-in-line plastic packages (E suffix) and in 16-lead dual-in-line surface mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- *Fanout (Over Temperature Range):*
  Standard Outputs - 10 LSTTL Loads
  Bus Driver Outputs - 15 LSTTL Loads
- *Wide Operating Temperature Range:*
  CD74HC/HCT: -40 to +85° C
- *Balanced Propagation Delay and Transition Times*
- *Significant Power Reduction Compared to LSTTL Logic ICs*
- *Alternate Source is Philips/Signetics*
- *CD54HC/CD74HC Types:*
  2 to 6 V Operation
  High Noise Immunity: N_{IL} = 30%, N_{IH} = 30% of V_{CC}, @ V_{CC} = 5 V
- *CD54HCT/CD74HCT Types:*
  4.5 to 5.5 V Operation
  Direct LSTTL Input Logic Compatibility
  V_{IL} = 0.8 V Max., V_{IH} = 2 V Min.
  CMOS Input Compatibility
  $I_I \leq 1\ \mu A$ @ V_{OL}, V_{OH}



TERMINAL ASSIGNMENT

CD54/74HC283
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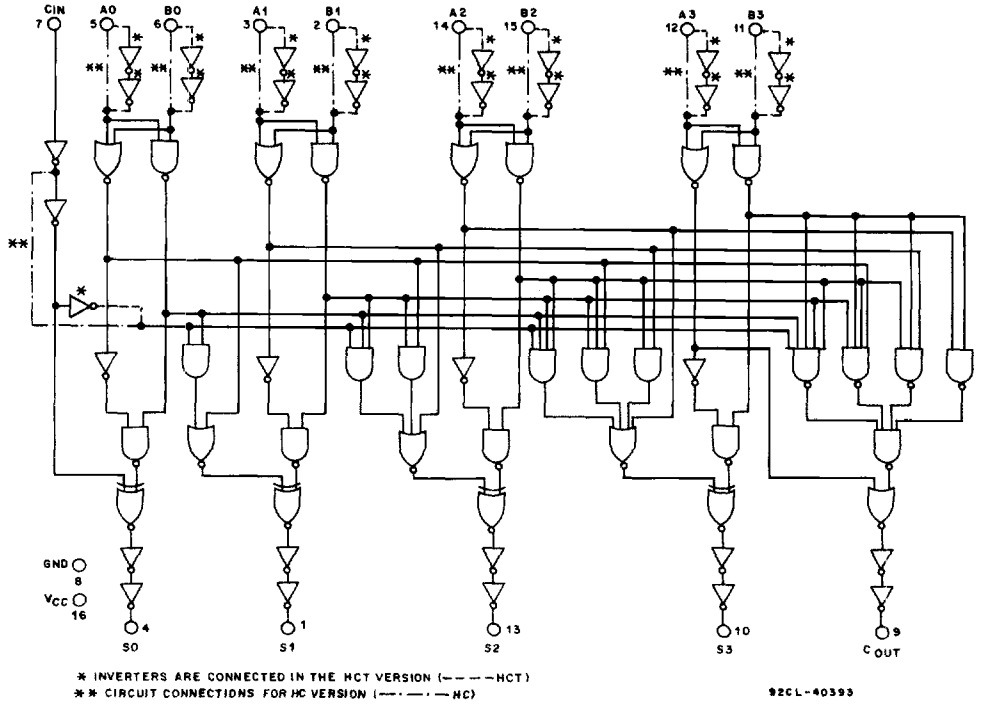

Fig. 1 - Logic diagram for HC/HCT types.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) ..... -0.5 to +7 V
DC INPUT DIODE CURRENT, I_{IK} (FOR $V_I < -0.5$ V OR $V_I > V_{CC}$ +0.5 V) ..... ±20 mA
DC OUTPUT DIODE CURRENT, I_{OK} (FOR $V_O < -0.5$ V OR $V_O > V_{CC}$ +0.5 V) ..... ±20 mA
DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR $-0.5 V < V_O < V_{CC}$ +0.5 V) ..... ±25 mA
DC V_{CC} OR GROUND CURRENT, (I_{CC}): ..... ±50 mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -40 to +60° C (PACKAGE TYPE E) ..... 500 mW
For T_A = +60 to +85° C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -55 to +100° C (PACKAGE TYPE F, H) ..... 500 mW
For T_A = +100 to +125° C (PACKAGE TYPE F, H) ..... Derate Linearly at 8 mW/° C to 300 mW
For T_A = -40 to +70° C (PACKAGE TYPE M) ..... 400 mW
For T_A = +70 to +125° C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/° C to 70 mW
OPERATING-TEMPERATURE RANGE (T_A):
PACKAGE TYPE F, H ..... -55 to +125° C
PACKAGE TYPE E, M ..... -40 to +85° C
STORAGE TEMPERATURE (T_{stg}) ..... -65 to +150° C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. ..... +265° C
Unit inserted into a PC board (min. thickness 1/16 in., 1.59 mm)
with solder contacting lead tips only ..... +300° C

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STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC283/CD54HC283										CD74HCT283/CD54HCT283									UNITS
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPES		54HC TYPES		TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPES		54HCT TYPES		
				+25°C			-40/ +85°C		-55/ +125°C				+25°C			-40/ +85°C		-55/ +125°C		
	V_I V	I_O mA	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	V_I V	V_{CC} V	Min	Typ	Max	Min	Max	Min	Max	
High-Level Input Voltage V_{IH}			2	1.5	—	—	1.5	—	1.5	—	—	4.5 to 5.5	2	—	—	2	—	2	—	V
			4.5	3.15	—	—	3.15	—	3.15	—										
			6	4.2	—	—	4.2	—	4.2	—										
Low-Level Input Voltage V_{IL}			2	—	—	0.5	—	0.5	—	0.5	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	V
			4.5	—	—	1.35	—	1.35	—	1.35										
			6	—	—	1.8	—	1.8	—	1.8										
High-Level Output Voltage V_{OH} CMOS Loads	V_{IL} or V_{IH}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V_{IL} or V_{IH}	4.5	4.4	—	—	4.4	—	4.4	—	V
			4.5	4.4	—	—	4.4	—	4.4	—										
			6	5.9	—	—	5.9	—	5.9	—										
TTL Loads	V_{IL} or V_{IH}	-4	4.5	3.98	—	—	3.84	—	3.7	—	V_{IL} or V_{IH}	4.5	3.98	—	—	3.84	—	3.7	—	V
		-5.2	6	5.48	—	—	5.34	—	5.2	—										
Low-Level Output Voltage V_{OL} CMOS Loads	V_{IL} or V_{IH}	0.02	2	—	—	0.1	—	0.1	—	0.1	V_{IL} or V_{IH}	4.5	—	—	0.1	—	0.1	—	0.1	V
			4.5	—	—	0.1	—	0.1	—	0.1										
			6	—	—	0.1	—	0.1	—	0.1										
TTL Loads	V_{IL} or V_{IH}	4	4.5	—	—	0.26	—	0.33	—	0.4	V_{IL} or V_{IH}	4.5	—	—	0.26	—	0.33	—	0.4	V
		5.2	6	—	—	0.26	—	0.33	—	0.4										
Input Leakage Current I_I	V_{CC} or Gnd		6	—	—	±0.1	—	±1	—	±1	Any Voltage Between V_{CC} & Gnd	5.5	—	—	±0.1	—	±1	—	±1	μA
Quiescent Device Current I_{CC}	V_{CC} or Gnd	0	6	—	—	8	—	80	—	160	V_{CC} or Gnd	5.5	—	—	8	—	80	—	160	μA
Additional Quiescent Device Current per input pin: 1 unit load ΔI_{CC}*											V_{CC} -2.1	4.5 to 5.5	—	100	360	—	450	—	490	μA

*For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS *
C_{IN}	1.5
B1, A1, A0	1
B0	0.4
B3, A3, A2, B2	0.5

* Unit Load is ΔI_{CC} limit specified in Static Characteristics Chart, e.g., 360 μA max. @ 25°C.

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RECOMMENDED OPERATING CONDITIONS:
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range) V_{CC}:*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V_I, V_O	0	V_{CC}	V
Operating Temperature T_A:			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	°C
Input Rise and Fall Times, t_r, t_f			
at 2 V	0	1000	ns
at 4.5 V	0	500	ns
at 6 V	0	400	ns

* Unless otherwise specified, all voltages are referenced to Ground.

SWITCHING CHARACTERISTICS (V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns)

CHARACTERISTIC		CL (pF)	TYPICAL VALUES		UNITS
			HC	HCT	
Propagation Delay,					ns
C_{IN} to S0	t_{PLH}, t_{PHL}	15	13	13	
C_{IN} to S1	t_{PLH}, t_{PHL}	15	15	18	
C_{IN} to S2	t_{PLH}, t_{PHL}	15	16	19	
C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	15	16	19	
C_{IN} to S3	t_{PHL}, t_{PLH}	15	19	22	
A_n, B_n to C_{OUT}	t_{PHL}, t_{PLH}	15	16	20	
A_n, B_n to S_n	t_{PHL}, t_{PLH}	15	18	21	
Power Dissipation Capacitance *	C_{PD}	—	70	82	pF

* C_{PD} is used to determine the dynamic power consumption, per package.
$P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
C_L = output load capacitance
V_{CC} = supply voltage

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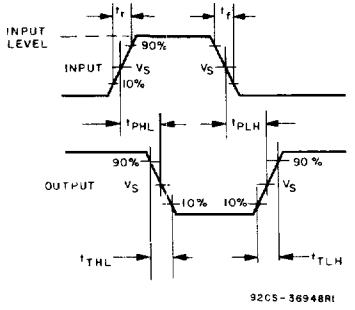
SWITCHING CHARACTERISTICS (C_L = 50 pF, Input t_r, t_f = 6 ns)

CHARACTERISTIC		TEST CONDITION V_{CC} V	LIMITS 25°C HC Min.	HC Max.	HCT Min.	HCT Max.	-40°C to +85°C 74HC Min.	74HC Max.	74HCT Min.	74HCT Max.	-55°C to +125°C 54HC Min.	54HC Max.	54HCT Min.	54HCT Max.	UNITS
Propagation	t_{PLH}	2	—	160	—	—	—	200	—	—	—	240	—	—	
Delay	t_{PHL}	4.5	—	32	—	31	—	40	—	39	—	48	—	47	
C_{IN} to S0		6	—	27	—	—	—	34	—	—	—	41	—	—	
	t_{PLH}	2	—	180	—	—	—	225	—	—	—	270	—	—	
C_{IN} to S1	t_{PHL}	4.5	—	36	—	43	—	45	—	54	—	54	—	65	
		6	—	31	—	—	—	38	—	—	—	46	—	—	
C_{IN} to S2,	t_{PLH}	2	—	195	—	—	—	245	—	—	—	295	—	—	
C_{IN} to C_{OUT}	t_{PHL}	4.5	—	39	—	46	—	49	—	58	—	59	—	69	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
	t_{PLH}	2	—	230	—	—	—	290	—	—	—	345	—	—	
C_{IN} to S3	t_{PHL}	4.5	—	46	—	53	—	58	—	66	—	69	—	80	ns
		6	—	39	—	—	—	49	—	—	—	59	—	—	
	t_{PLH}	2	—	195	—	—	—	245	—	—	—	295	—	—	
A_n, B_n to C_{OUT}	t_{PHL}	4.5	—	39	—	48	—	49	—	60	—	59	—	72	
		6	—	33	—	—	—	42	—	—	—	50	—	—	
	t_{PLH}	2	—	210	—	—	—	265	—	—	—	315	—	—	
A_n, B_n to S_n	t_{PHL}	4.5	—	42	—	49	—	53	—	61	—	63	—	74	
		6	—	36	—	—	—	45	—	—	—	54	—	—	
Output	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	—	
Transition	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—	22	
Time		6	—	13	—	—	—	16	—	—	—	19	—	—	
Input Capacitance	C_I		—	10	—	10	—	10	—	10	—	10	—	10	pF



	54/74HC	54/74HCT
Input Level	V_{CC}	3 V
Switching Voltage, V_S	50% V_{CC}	1.3 V

Fig. 2 - Transition and propagation delay times.