Signetics

Military Logic Products

54S157, 54S158
Data Selectors/Multiplexers

54S157 Quad 2-Input Data Selector/Multiplexer (Non-Inverted)
54S158 Quad 2-Input Data Selector/Multiplexer (Inverted)

Product Specification

DESCRIPTION

The 54S157 is a quad 2-input multiplexer which selects four bits of data from two sources under the control of a common Select input (S). The Enable input ($\overline{E}$) is active Low. When $\overline{E}$ is High, all of the outputs (Y) are forced Low regardless of all other input conditions.

Moving data from two groups of registers to four common output buses is a common use of the 54S157. The state of the Select input determines the particular register from which the data comes. It can also be used as a function generator. The device is useful for implementing highly irregular logic by generating any four of the 16 different functions of two variables with one variable common.

The device is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. Logic equations for the outputs are shown below:

$$Y_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$Y_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$Y_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$Y_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

The 54S158 is similar but has inverting outputs:

$$\overline{Y}_a = \overline{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \overline{S})$$
$$\overline{Y}_b = \overline{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \overline{S})$$
$$\overline{Y}_c = \overline{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \overline{S})$$
$$\overline{Y}_d = \overline{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \overline{S})$$

ORDERING INFORMATION

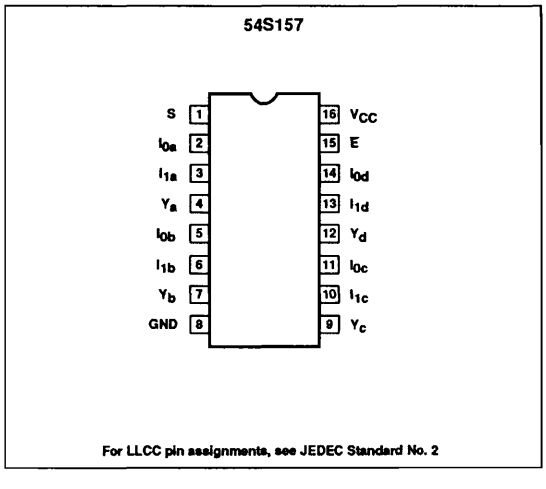
DESCRIPTION	ORDER CODE
16-Pin Ceramic DIP	54S157/BEA, 54S158/BEA
16-Pin Ceramic FlatPack	54S157/BFA, 54S158/BFA
20-Pin Ceramic LLCC	54S157/B2A, 54S158/B2A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54S
S, $\overline{E}$	Inputs	2SUL
Data	Inputs	1SUL
All	Outputs	10SUL

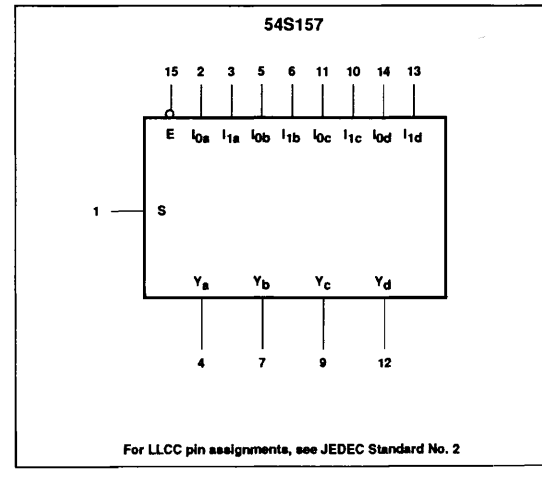
NOTE: Where a 54S Unit Load (SUL) is 50μA I_{IH} and -2.0mA I_{IL}.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



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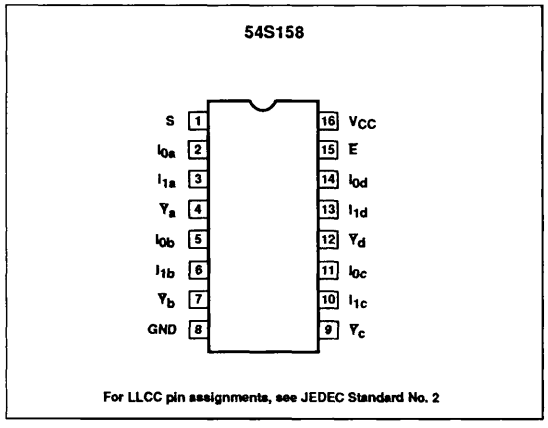
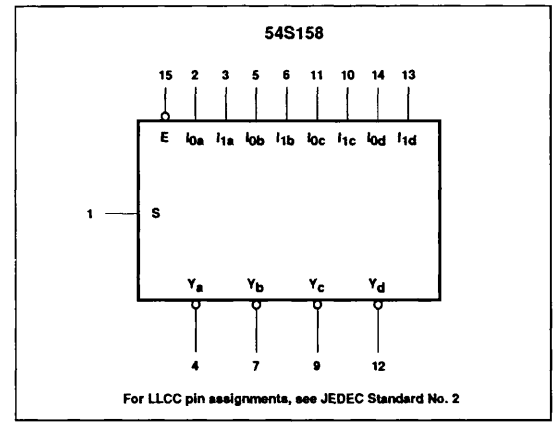
PIN CONFIGURATION



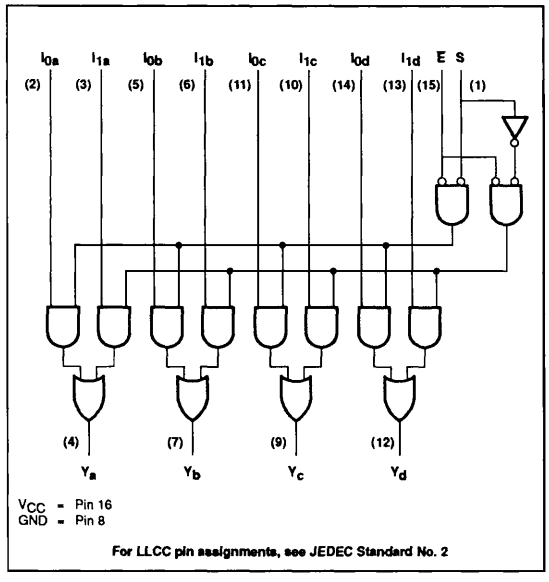
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



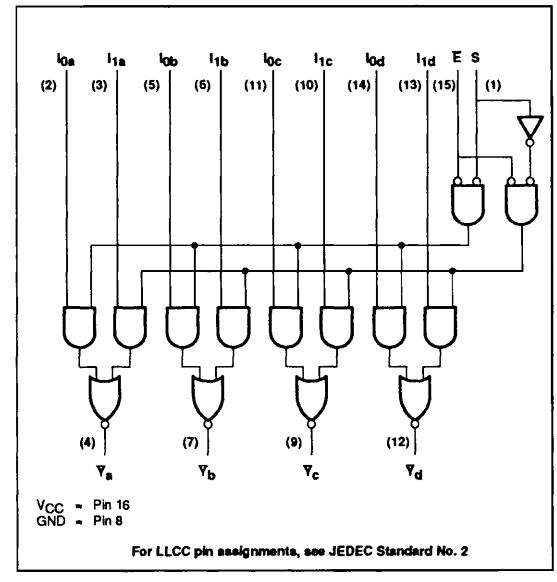
For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM 54F157



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC DIAGRAM, 54F158



For LLCC pin assignments, see JEDEC Standard No. 2

FUNCTION TABLE, 54F157

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	Y
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = High voltage level
L = Low voltage level
X = Don't care

FUNCTION TABLE, 54F158

ENABLE	SELECT INPUT	DATA INPUTS		OUTPUT
$\overline{E}$	S	I_0	I_1	$\overline{Y}$
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	7.0	V
V_I	Input voltage range	-0.5 to +5.5	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				+0.8	V
		+125°C			+0.7	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-1000	µA
I_{OL}	Low-level output current				20	mA
T_A	Operating free-air temperature range		-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]		LIMITS			UNIT
				Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IH} = Min, V_{IL} = Max, I_{OH} = Max		2.5	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = Min, I_{OL} = Max, V_{IH} = Min,				0.5	V
		V_{IL} = Max	+125°C			0.45	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}				-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 5.5V				1.0	mA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V	S, $\overline{E}$ inputs			100	µA
			Data inputs			50	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V	S, $\overline{E}$ inputs			-4	mA
			Data inputs			-2	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max		-40		-110	mA
I_{CC}	Supply current[4,5] (total)	V_{CC} = Max	54S157 All inputs ≥ 4.0V		50	78	mA
			54S158 All inputs ≥ 4.0V		39	61	mA
			54S158 I_{0a}, I_{0b}, I_{0c}, I_{0d} at ≥ 4.0V – other inputs at 0V		41	81	mA

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 15pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2, 54S157		7.5 6.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1, 54S157		12.5 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2, 54S157		15 15	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 3, 54S158		6.0 6.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 4, 54S158		11.5 12	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 3, 54S158		12 12	ns ns

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5.0V$[6]

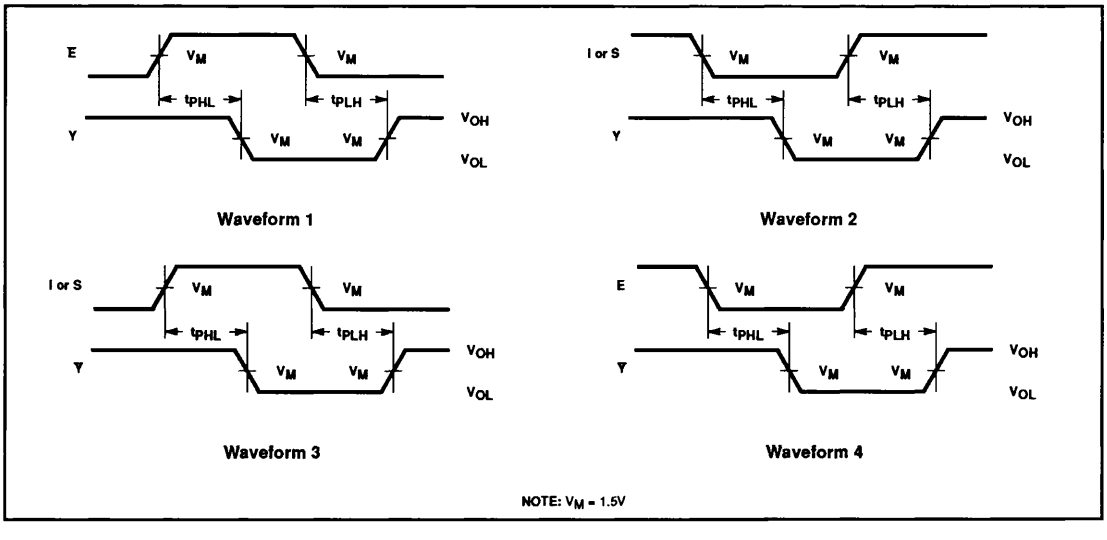
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$C_L = 50pF$		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2, 54S157		10.0 9.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1, 54S157		15.0 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2, 54S157		17.5 17.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 3, 54S158		8.5 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 4, 54S158		14.0 14.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 3, 54S158		14.5 14.5	ns ns

AC ELECTRICAL CHARACTERISTICS T_A = -55°C and +125°C, V_{CC} = 5.0V[6]

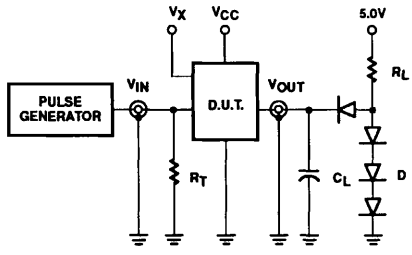
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			C_L = 50pF		
			Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 2, 54S157		13.0 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 1, 54S157		20.0 19.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 2, 54S157		23.0 23.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Data to output	Waveform 3, 54S158		11.0 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Enable to output	Waveform 4, 54S158		18.0 19.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Select to output	Waveform 3, 54S158		19.0 19.0	ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions and function table operating mode.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
4. I_{CC} is measured with ≥ 4.0V applied to all inputs and all outputs open.
5. I_{CC} is measured with all outputs open.
6. These parameters are guaranteed, but not tested.

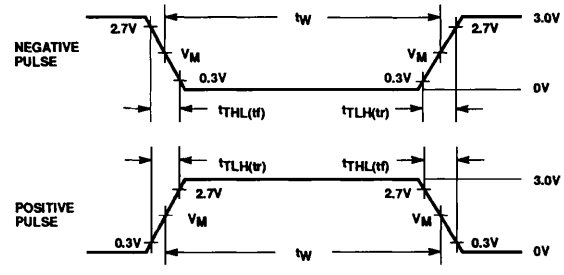
AC WAVEFORMS



TEST CIRCUIT AND WAVEFORM



Test Circuit for 54 Totem-Pole Outputs



Input Pulse Definition

FAMILY	INPUT PULSE CHARACTERISTICS					
	R_L	V_M	Rep. Rate	T_W	T_{TLH}	T_{THL}
54SXXX	280Ω	1.5V	1MHz	500ns	≤2.5ns	≤2.5ns

DEFINITIONS:
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
D = Diodes are 1N916, 1N3064, or equivalent.
V_X = Unclocked pins must be held at ≤0.8V, ≥2.7V or open per FunctionTable.