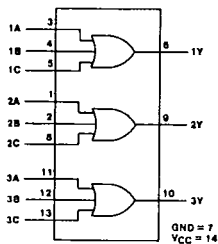


CD54/74HC4075
CD54/74HCT4075

File Number 1778

HARRIS SEMICONDUCTOR SECTOR 27E D ■ 4302271 0017955 8 ■ HAS

High-Speed CMOS Logic



Triple 3-Input OR Gate

Type Features:

- Buffered inputs
- Typical CD54/74HC4075 Propagation Delay = 8ns
@ $V_{CC} = 5V$, $C_L = 15pF$, $T_A = 25^\circ C$

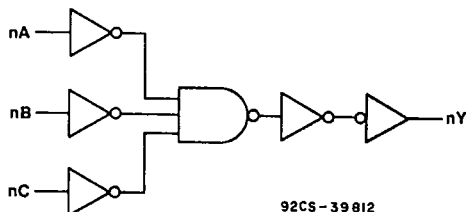
92CS-39816
FUNCTIONAL DIAGRAM

The RCA-CD54/74HC4075 and CD54/74HCT4075 logic gates utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. All devices have the ability to drive 10 LSTTL loads. The CD54/74HCT logic family is functionally as well as pin compatible with the standard 54LS/74LS logic family.

The CD54HC4075 and CD54HCT4075 are supplied in 14-lead hermetic dual-in-line ceramic packages (F suffix). The CD74HC4075 and CD74HCT4075 are supplied in 14-lead dual-in-line plastic packages (E suffix) and in 14-lead dual-in-line surface-mount plastic packages (M suffix). Both types are also available in chip form (H suffix).

Family Features:

- Fanout (over temperature range):
Standard Outputs - 10 LSTTL loads
Bus driver outputs - 15 LSTTL loads
- Wide Operating temperature range:
CD74HC/HCT: -40 to +85°C
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL logic ICs
- Alternate source is Philips/Signetics
- CD54HC/CD74HC Types:
2 to 6 V Operation
High noise immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC}
@ $V_{CC} = 5V$
- CD54HCT/CD74HCT Types:
4.5 to 5.5 V Operation
Direct LSTTL input logic compatibility
 $V_{IL} = 0.8V$ max., $V_{IH} = 2V$ Min.
CMOS input compatibility
 $I_I \leq 1 \mu A$ @ V_{OL} , V_{OH}



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LOGIC DIAGRAM

TRUTH TABLE

nA	nB	nC	nY
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

L = Low voltage Level
H = High voltage Level
X = Don't Care

CD54/74HC4075
CD54/74HCT4075

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE, (V_{CC}):
(Voltages referenced to ground) -0.5 to + 7 V

DC INPUT DIODE CURRENT, I_{IK} (FOR V_I < -0.5 V OR V_I > V_{CC} + 0.5V) ±20mA

DC OUTPUT DIODE CURRENT, I_{OK} (FOR V_O < -0.5 V OR V_O > V_{CC} + 0.5V) ±20mA

DC DRAIN CURRENT, PER OUTPUT (I_O) (FOR -0.5 V < V_O < V_{CC} + 0.5V) ±25mA

DC V_{CC} OR GROUND CURRENT (I_{CC}) ±50mA

POWER DISSIPATION PER PACKAGE (P_O):

For T_A = -40 to +60°C (PACKAGE TYPE E) 500 mW

For T_A = +60 to +85°C (PACKAGE TYPE E) Derate Linearly at 8 mW/°C to 300 mW

For T_A = -55 to +100°C (PACKAGE TYPE F, H) 500 mW

For T_A = +100 to +125°C (PACKAGE TYPE F, H) Derate Linearly at 8 mW/°C to 300 mW

For T_A = -40 to +70°C (PACKAGE TYPE M) 400 mW

For T_A = +70 to +125°C (PACKAGE TYPE M) Derate Linearly at 6 mW/°C to 70 mW

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPE F, H -55 to +125°C

PACKAGE TYPE E, M -40 to +85°C

STORAGE TEMPERATURE (T_{stg}) -65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s max. +265°C

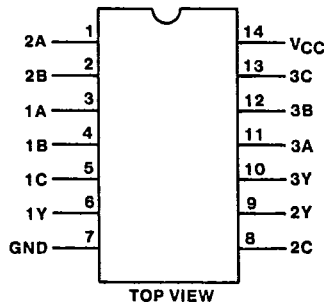
Unit inserted into a PC Board (min. thickness 1/16 in., 1.59 mm) with solder contacting lead tips only +300°C

RECOMMENDED OPERATING CONDITIONS:

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range (For T _A = Full Package-Temperature Range) V _{CC} .*			
CD54/74HC Types	2	6	V
CD54/74HCT Types	4.5	5.5	V
DC Input or Output Voltage V _I , V _O	0	V _{CC}	V
Operating Temperature T _A :			
CD74 Types	-40	+85	°C
CD54 Types	-55	+125	
Input Rise and Fall Times t _r , t _f			
at 2 V	0	1000	ns
at 4.5 V	0	500	
at 6 V	0	400	

*Unless otherwise specified, all voltages are referenced to Ground.



92CS-39813

TERMINAL ASSIGNMENT

HARRIS SEMICONDUCTOR 27E D 430227J 0017956 T HAS

CD54/74HC4075
CD54/74HCT4075

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CD74HC4075/CD54HC4075										CD74HCT4075/CD54HCT4075										UNITS		
	TEST CONDITIONS			74HC/54HC TYPES			74HC TYPE		54HC TYPE			TEST CONDITIONS		74HCT/54HCT TYPES			74HCT TYPE		54HCT TYPE				
	V _i V	I _o mA	V _{cc} V	+25°C			-40/ +85°C		-55/ +125°C			V _i V	V _{cc} V	+25°C			-40/ +85°C		-55/ +125°C				
				Min	Typ	Max	Min	Max	Min	Max	Min			Max	Min	Typ	Max	Min	Max	Min		Max	
High-Level Input Voltage V _{ih}			2	1.5	—	—	1.5	—	1.5	—	—	—	4.5 to 5.5	2	—	—	2	—	2	—	—	V	
			4.5	3.15	—	—	3.15	—	3.15	—	—			—	—	—	—	—	—	—	—		—
			6	4.2	—	—	4.2	—	4.2	—	—			—	—	—	—	—	—	—	—		—
Low-Level Input Voltage V _{il}			2	—	—	0.5	—	0.5	—	0.5	—	—	4.5 to 5.5	—	—	0.8	—	0.8	—	0.8	—	V	
			4.5	—	—	1.35	—	1.35	—	1.35	—			—	—	—	—	—	—	—	—		—
			6	—	—	1.8	—	1.8	—	1.8	—			—	—	—	—	—	—	—	—		—
High-Level Output Voltage V _{oh} or CMOS Loads	V _{ih} or V _{oh}	-0.02	2	1.9	—	—	1.9	—	1.9	—	V _{ih} or V _{oh}	4.5	4.4	—	—	4.4	—	4.4	—	4.4	—	V	
			4.5	4.4	—	—	4.4	—	4.4	—			—	—	—	—	—	—	—	—			
			6	5.9	—	—	5.9	—	5.9	—			—	—	—	—	—	—	—	—	—		—
TTL Loads	V _{ih} or V _{oh}	-4 or -5.2	4.5	3.98	—	—	3.84	—	3.7	—	V _{ih} or V _{oh}	4.5	3.98	—	—	3.84	—	3.7	—	—	V		
			6	5.48	—	—	5.34	—	5.2	—			—	—	—	—	—	—	—	—			
			—	—	—	—	—	—	—	—			—	—	—	—	—	—	—	—		—	—
Low-Level Output Voltage V _{ol} or CMOS Loads	V _{ih} or V _{oh}	0.02	2	—	—	0.1	—	0.1	—	V _{ih} or V _{oh}	4.5	—	—	0.1	—	0.1	—	0.1	—	0.1	—	V	
			4.5	—	—	0.1	—	0.1	—			0.1	—	—	—	—	—	—	—	—			
			6	—	—	0.1	—	0.1	—			0.1	—	—	—	—	—	—	—	—	—		
TTL Loads	V _{ih} or V _{oh}	4 or 5.2	4.5	—	—	0.26	—	0.33	—	V _{ih} or V _{oh}	4.5	—	—	0.26	—	0.33	—	0.4	—	0.4	—	V	
			6	—	—	0.26	—	0.33	—			0.4	—	—	—	—	—	—	—	—			
			—	—	—	—	—	—	—			—	—	—	—	—	—	—	—	—	—		—
Input Leakage Current I _i	V _{cc} or Gnd		6	—	—	±0.1	—	±1	—	±1	—	Any Voltage Between V _{cc} & Grid	5.5	—	—	±0.1	—	±1	—	±1	—	μA	
Quiescent Device Current I _{cc}	V _{cc} or Gnd	0	6	—	—	2	—	20	—	40	V _{cc} or Gnd	5.5	—	—	2	—	20	—	40	—	μA		
Additional Quiescent Device Current per input pin: 1 unit load ΔI _{cc} *											V _{cc} -2.1 to 5.5	—	—	100	360	—	450	—	490	—	μA		

*For dual-supply systems theoretical worst case (V_i = 2.4 V, V_{cc} = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS*
All	1.6

*Unit Load is ΔI_{cc} limit specified in Static Characteristic Chart, e.g., 360 μA max. @25° C.

HARRIS SEMICONDUCTOR 27E D 430227J 00J7957 J HAS

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CD54/74HC4075
CD54/74HCT4075

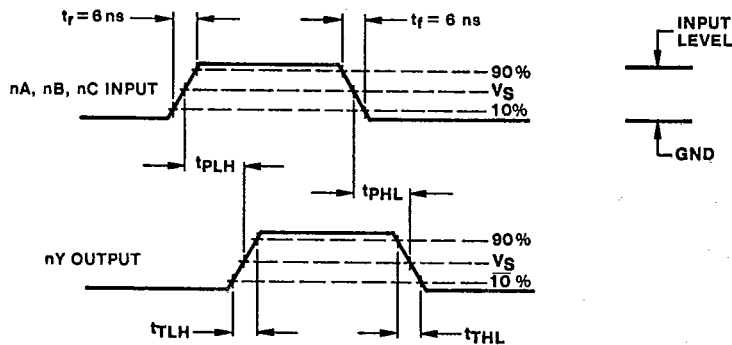
SWITCHING CHARACTERISTICS ($V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$, Input $t_r = 6\text{ ns}$)

CHARACTERISTIC	CL (pF)	TYPICAL		UNITS	
		HC	HCT		
Propagation Delay, Data Input to Output Y (Fig. 1)	t_{PLH}, t_{PHL}	15	8	9	ns
Power Dissipation Capacitance*	C_{PD}	—	26	28	pF

* C_{PD} is used to determine the dynamic power consumption, per gate.
 $P_o = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = input frequency
 C_L = load capacitance
 V_{CC} = supply voltage

SWITCHING CHARACTERISTICS ($C_L = 50\text{ pF}$, Input $t_r = 6\text{ ns}$)

CHARACTERISTIC	V_{CC}	25°C				-40°C to +85°C				-55°C to +125°C				UNITS	
		HC		HCT		74HC		74HCT		54HC		54HCT			
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Propagation Delay, Input to Output (Fig. 1)	t_{PLH}	2	—	100	—	—	—	125	—	—	—	150	—	ns	
	t_{PHL}	4.5	—	20	—	24	—	25	—	30	—	30	—		36
		6	—	17	—	—	—	21	—	—	—	26	—		
Transition Times (Fig. 1)	t_{TLH}	2	—	75	—	—	—	95	—	—	—	110	—	ns	
	t_{THL}	4.5	—	15	—	15	—	19	—	19	—	22	—		22
		6	—	13	—	—	—	16	—	—	—	19	—		
Input Capacitance	C_i	—	10	—	10	—	10	—	10	—	10	—	10	pF	



92CS-398II

	54/74HC	54/74HCT
Input Level	V_{CC}	3V
Switching Voltage, V_S	50% V_{CC}	1.3V

Fig. 1 - Transition times and propagation delay times.