National Semiconductor

DS55460/DS75460 Series Dual Peripheral Drivers

General Description

The DS55460/DS75460 series of dual peripheral drivers are functionally interchangeable with DS55450/DS75450 series peripheral drivers, but are designed for use in systems that require higher breakdown voltages than DS55450/DS75450 series can provide at the expense of slightly slower switching speeds. Typical applications include power drivers, logic buffers, lamp drivers, relay drivers, MOS drivers, line drivers and memory drivers.

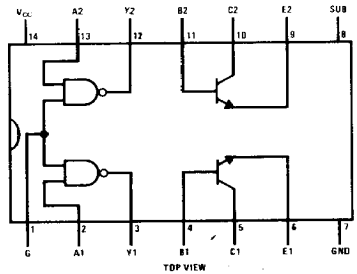
The DS55460 and DS75460 are unique general-purpose devices each featuring two standard 54/74 series TTL gates and two uncommitted, high current, high voltage, NPN transistors. These devices offer the system designer the flexibility of tailoring the circuit to the application.

The DS55461/DS75461, DS55462/DS75462, DS55463/DS75463 and DS55464/DS75464 are dual peripheral AND, NAND, OR and NOR drivers, respectively, (positive logic) with the output of the logic gates internally connected to the bases of the NPN output transistors.

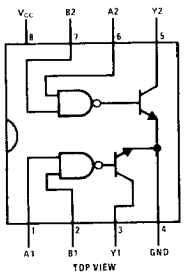
Features

- 300 mA output current capability
- High voltage outputs
- No output latch-up at 30V
- Medium speed switching
- Circuit flexibility for varied applications and choice of logic function
- TTL or DTL compatible diode-clamped inputs
- Standard supply voltages

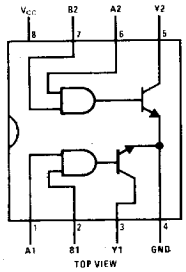
Connection Diagrams (Dual-In-Line and Metal Can Packages)



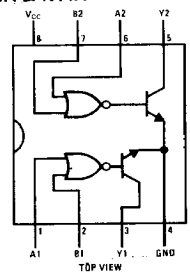
Order Number
DS55460J, DS75460J, or DS75460N
See NS Package J14A or N14A



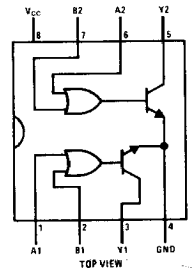
Order Number DS55461J-8, DS75461J-8 or DS75461N-8



Order Number DS55462J-8, DS75462J-8 or DS75462N-8

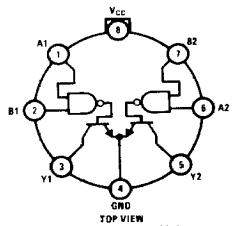


Order Number DS55463J-8, DS75463J-8 or DS75463N-8

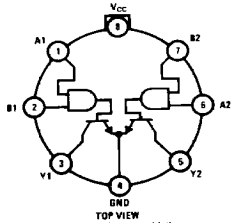


Order Number DS55464J-8, DS75464J-8 or DS75464N-8

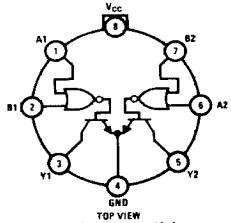
See NS Package J08A or N08A



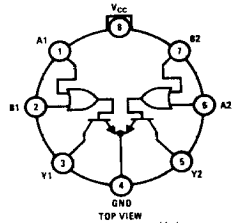
Order Number
DS55461H or DS75461H



Order Number
DS55462H or DS75462H



Order Number
DS55463H or DS75463H



Order Number
DS55464H or DS75464H

See NS Package H08C

Absolute Maximum Ratings (Note 1)

Supply Voltage (Note 2)	7V
Input Voltage	5.5V
Inter-emitter Voltage (Note 3)	5.5V
V_{CC}-to-Substrate Voltage	
DS55460/DS75460	40V
Collector-to-Substrate Voltage	
DS55460/DS75460	40V
Collector-Base Voltage	
DS55460/DS75460	40V
Collector-Emitter Voltage	
DS55460/DS75460 (Note 4)	40V
DS55460/DS75460 (Note 5)	25V
Emitter-Base Voltage	
DS55460/DS75460	5V
Output Voltage (Note 6)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	35V
Collector Current (Note 7)	
DS55460/DS75460	300 mA
Output Current (Note 7)	
DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464	300 mA
Continuous Total Dissipation	800 mW
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C

Operating Conditions (Note 7)

	MIN	MAX	UNITS
Supply Voltage (V_{CC})			
DS5546X	4.5	5.5	V
DS7546X	4.75	5.25	V
Temperature (T_A)			
DS5546X	−55	+125	°C
DS7546X	0	+70	°C

Electrical Characteristics

DS55460/DS75460 (Notes 8 and 9)

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
TTL GATES							
V_{IH}	High Level Input Voltage	*(Figure 1)*		2			V
V_{IL}	Low Level Input Voltage	*(Figure 2)*				0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA, *(Figure 3)*			−1.2	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, V_{IL} = 0.8V, I_{OH} = −400μA, *(Figure 2)*		2.4	3.3		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, V_{IH} = 2V, I_{OL} = 16 mA, *(Figure 1)*	DS55460		0.25	0.5	V
			DS75460		0.25	0.4	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 4)*	Input A			1	mA
			Input G			2	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 4)*	Input A			40	μA
			Input G			80	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 3)*	Input A			−1.6	mA
			Input G			−3.2	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max, (Note 10), *(Figure 5)*		−18	−35	−55	mA
I_{CCH}	Supply Current	V_{CC} = Max, V_I = 0V, Outputs High, *(Figure 6)*			2.8	4	mA
I_{CCL}	Supply Current	V_{CC} = Max, V_I = 5V, Outputs Low, *(Figure 6)*			7	11	mA
OUTPUT TRANSISTORS							
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	I_C = 100μA, I_E = 0		40			V
$V_{(BR)CER}$	Collector-Emitter Breakdown Voltage	I_C = 100μA, R_{BE} = 500Ω		40			V
$V_{(BR)CEO}$		I_C = 10 mA, I_B = 0 (Note 12)		25			V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	I_E = 100μA, I_C = 0		5			V
h_{FE}	Static Forward Current Transfer Ratio	V_{CE} = 3V, (Note 12)	DS55460, T_A = 25°C, I_C = 100 mA	25			
			DS55460, T_A = 25°C, I_C = 300 mA	30			
			DS55460, T_A = −55°C, I_C = 100 mA	10			
			DS55460, T_A = −55°C, I_C = 300 mA	15			
			DS75460, T_A = 25°C, I_C = 100 mA	25			
			DS75460, T_A = 25°C, I_C = 300 mA	30			
			DS75460, T_A = 0°C, I_C = 100 mA	20			
			DS75460, T_A = 0°C, I_C = 300 mA	25			

Electrical Characteristics DS55460/DS75460 (Continued)

	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
V_{BE}	Base-Emitter Voltage	(Note 12)	DS55460	I_B = 10 mA, I_C = 100 mA		0.85	1.2	V
				I_B = 30 mA, I_C = 300 mA		1	1.4	V
			DS75460	I_B = 10 mA, I_C = 100 mA		0.85	1	V
				I_B = 30 mA, I_C = 300 mA		1	1.2	V
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	(Note 12)	DS55460	I_B = 10 mA, I_C = 100 mA		0.25	0.5	V
				I_B = 30 mA, I_C = 300 mA		0.45	0.8	V
			DS75460	I_B = 10 mA, I_C = 100 mA		0.25	0.4	V
				I_B = 30 mA, I_C = 300 mA		0.45	0.7	V

Switching Characteristics

DS55460/DS75460 V_{CC} = 5V, T_A = 25°C

	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates Only, *(Figure 12)*		22		ns
			R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*		45	65	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	C_L = 15 pF	R_L = 400Ω, TTL Gates Only, *(Figure 12)*		8		ns
			R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*		35	50	ns
t_{TLH}	Transition Time, Low-To-High Level Output	C_L = 15 pF, R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*			10	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	C_L = 15 pF, R_L = 50Ω, I_C ≈ 200 mA, Gates and Transistors Combined, *(Figure 14)*			10	20	ns
V_{OH}	High Level Output Voltage After Switching	V_S = 30V, I_C ≈ 300 mA, R_{BE} = 500Ω, *(Figure 15)*		V_S−10			mV
t_d	Delay Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			10		ns
t_r	Rise Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			16		ns
t_s	Storage Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			23		ns
t_f	Fall Time	I_C = 200 mA, $I_{B(1)}$ = 20 mA, $I_{B(2)}$ = −40 mA, $V_{BE(OFF)}$ = −1V, C_L = 15 pF, R_L = 50Ω, (Note 13), *(Figure 13)*			14		ns

Electrical Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 (Notes 8 and 9)

PARAMETER		CONDITIONS			MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	*(Figure 7)*			2			V
V_{IL}	Low Level Input Voltage	*(Figure 7)*					0.8	V
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.2	−1.5	V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, *(Figure 7)*	DS55461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.5	V
				I_{OL} = 300 mA		0.36	0.8	V
			DS55462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.5	V
				I_{OL} = 300 mA		0.35	0.8	V
			DS55463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.5	V
				I_{OL} = 300 mA		0.39	0.8	V
			DS55464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.5	V
				I_{OL} = 300 mA		0.38	0.8	V
			DS75461, V_{IL} = 0.8V	I_{OL} = 100 mA		0.15	0.4	V
				I_{OL} = 300 mA		0.36	0.7	V
			DS75462, V_{IH} = 2V	I_{OL} = 100 mA		0.16	0.4	V
				I_{OL} = 300 mA		0.35	0.7	V
			DS75463, V_{IL} = 0.8V	I_{OL} = 100 mA		0.18	0.4	V
				I_{OL} = 300 mA		0.39	0.7	V
			DS75464, V_{IH} = 2V	I_{OL} = 100 mA		0.17	0.4	V
				I_{OL} = 300 mA		0.38	0.7	V
I_{OH}	High Level Output Current	V_{CC} = Min, V_{OH} = 35V, *(Figure 7)*	V_{IH} = 2V	DS55461, DS55463			300	μA
				DS75461, DS75463			100	μA
			V_{IL} = 0.8V	DS55462, DS55464			300	μA
				DS75462, DS75464			100	μA
I_I	Input Current at Maximum Input Voltage	V_{CC} = Max, V_I = 5.5V, *(Figure 9)*					1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V, *(Figure 9)*					40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V, *(Figure 8)*				−1	−1.6	mA
I_{CCH}	Supply Current	V_{CC} = Max, Outputs High, *(Figure 11)*	V_I = 5V	DS55461/ DS75461, DS55463/ DS75463		8	11	mA
			V_I = 0V	DS55462/ DS75462		13	17	mA
				DS55464/ DS75464		14	19	mA
I_{CCL}	Supply Current	V_{CC} = Max, Outputs Low, *(Figure 11)*	V_I = 0V	DS55461/ DS75461		61	76	mA
				DS55463/ DS75463		63	76	mA
			V_I = 5V	DS55462/ DS75462		65	76	mA
				DS55464/ DS75464		72	85	mA

Switching Characteristics

DS55461/DS75461, DS55462/DS75462, DS55463/DS75463, DS55464/DS75464 $V_{CC} = 5V$, $T_A = 25°C$

PARAMETER		CONDITIONS		MIN	TYP	MAX	UNITS
t_{PLH}	Propagation Delay Time, Low-To-High Level Output	$I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461, DS55463/ DS75463		45	55	ns
			DS55462/ DS75462, DS55464/ DS75464		50	65	ns
t_{PHL}	Propagation Delay Time, High-To-Low Level Output	$I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461, DS55463/ DS75463		30	40	ns
			DS55462/ DS75462, DS55464/ DS75464		40	50	ns
t_{TLH}	Transition Time, Low-To-High Level Output	$I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461		8	20	ns
			DS55462/ DS75462		12	25	ns
			DS55463/ DS75463		8	25	ns
			DS55464/ DS75464		12	20	ns
t_{THL}	Transition Time, High-To-Low Level Output	$I_O \approx 200$ mA, $C_L = 15$ pF, $R_L = 50\Omega$, *(Figure 14)*	DS55461/ DS75461		10	20	ns
			DS55462/ DS75462, DS55464/ DS75464		15	20	ns
			DS55463/ DS75463		10	25	ns
V_{OH}	High-Level Output Voltage After Switching	$V_S = 30V$, $I_O \approx 300$ mA, *(Figure 15)*		V_S-10			mV

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Voltage values are with respect to network ground terminal unless otherwise specified.

Note 3: This is the voltage between two emitters of a multiple-emitter transistor.

Note 4: This value applies when the base-emitter resistance (R_{BE}) is equal to or less than 500 Ω.

Note 5: This value applies between 0 and 10 mA collector current when the base-emitter diode is open circuited.

Note 6: This is the maximum voltage which should be applied to any output when it is in the "OFF" state.

Note 7: Both halves of these dual circuits may conduct rated current simultaneously; however, power dissipation averaged over a short time interval must fall within the continuous dissipation rating.

Note 8: Unless otherwise specified min/max limits apply across the −55°C to +125°C temperature range for the DS55460 series and across the 0°C to +70°C range for the DS75460 series. All typicals are given for $V_{CC} = +5V$ and $T_A = 25°C$.

Note 9: All currents into device pins shown as positive, out of device pins as negative, all voltages referenced to ground unless otherwise noted. All values shown as max or min on absolute value basis.

Note 10: Only one output at a time should be shorted.

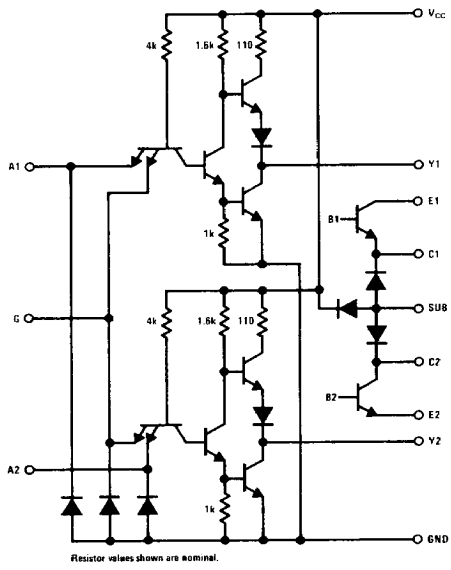
Note 11: For the DS55460/DS75460 only, the substrate (pin 8) must always be at the most negative device voltage for proper operation.

Note 12: These parameters must be measured using pulse techniques. $t_W = 300\mu s$, duty $< 2\%$.

Note 13: Applies to output transistors only.

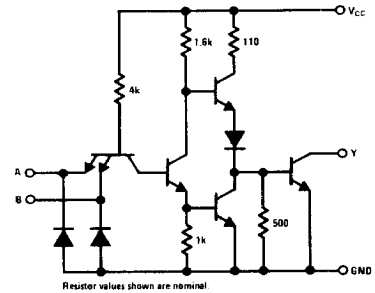
Schematic Diagrams

DS55460/DS75460



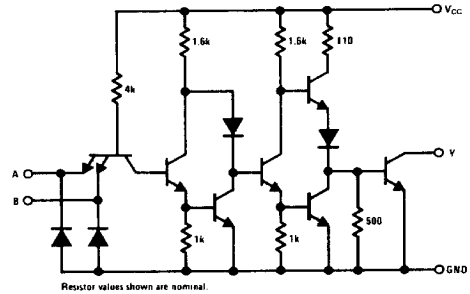
Resistor values shown are nominal.

DS55461/DS75461



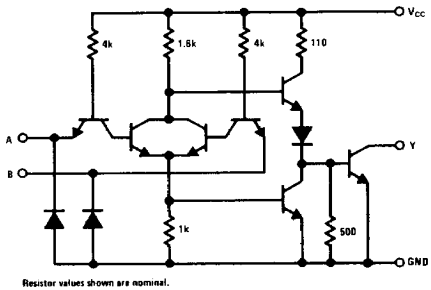
Resistor values shown are nominal.

DS55462/DS75462



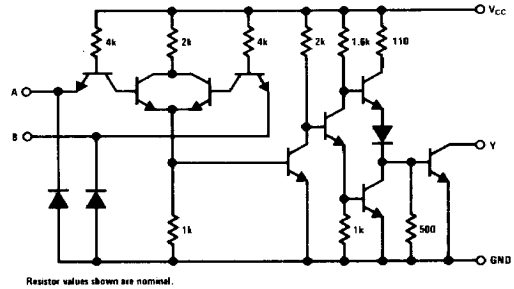
Resistor values shown are nominal.

DS55463/DS75463



Resistor values shown are nominal.

DS55464/DS75464



Resistor values shown are nominal.

Truth Tables (H = high level, L = low level)

DS55461/DS75461

A	B	Y
L	L	L (ON State)
L	H	L (ON State)
H	L	L (ON State)
H	H	H (OFF State)

DS55462/DS75462

A	B	Y
L	L	H (OFF State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	L (ON State)

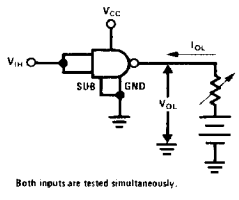
DS55463/DS75463

A	B	Y
L	L	L (ON State)
L	H	H (OFF State)
H	L	H (OFF State)
H	H	H (OFF State)

DS55464/DS75464

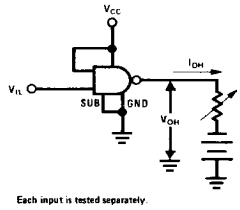
A	B	Y
L	L	H (OFF State)
L	H	L (ON State)
H	L	L (ON State)
H	H	L (ON State)

DC Test Circuits



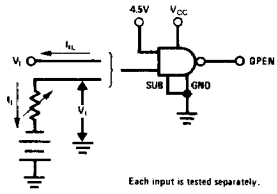
Both inputs are tested simultaneously.

FIGURE 1. V_{IH}, V_{OL}



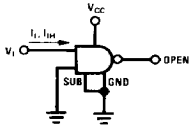
Each input is tested separately.

FIGURE 2. V_{IL}, V_{OH}



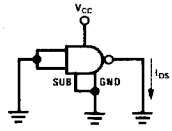
Each input is tested separately.

FIGURE 3. V_I, I_{IL}



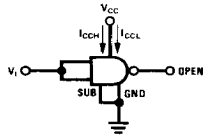
Each input is tested separately.

FIGURE 4. I_I, I_{IH}



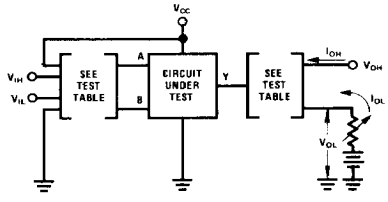
Each gate is tested separately.

FIGURE 5. I_{OS}



Both gates are tested simultaneously.

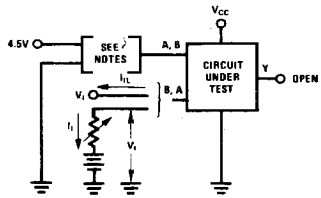
FIGURE 6. I_{CCH}, I_{CCL}



CIRCUIT	INPUT UNDER TEST	OTHER INPUT	OUTPUT	
			APPLY	MEASURE
DS55461	V_{IH} V_{IL}	V_{IH} V_{CC}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55462	V_{IH} V_{IL}	V_{IH} V_{CC}	I_{OL} V_{OH}	V_{OL} I_{OH}
DS55463	V_{IH} V_{IL}	Gnd V_{IL}	V_{OH} I_{OL}	I_{OH} V_{OL}
DS55464	V_{IH} V_{IL}	Gnd V_{IL}	I_{OL} V_{OH}	V_{OL} I_{OH}

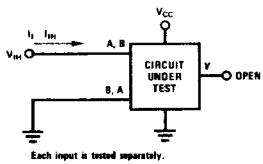
Each input is tested separately.

FIGURE 7. V_{IH}, V_{IL}, I_{OH}, V_{OL}



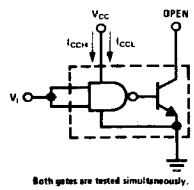
Note 1: Each input is tested separately.
Note 2: When testing DS55463/DS75463 and DS75464, input not under test is grounded.
For all other circuits it is at 4.5V.

FIGURE 8. V_I, I_{IL}



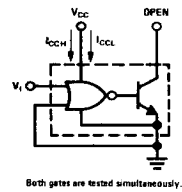
Each input is tested separately.

FIGURE 9. I_I, I_{IH}



Both gates are tested simultaneously.

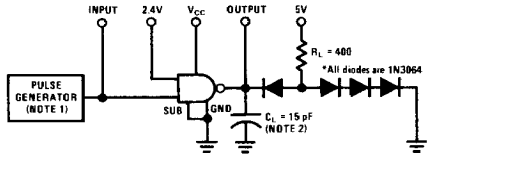
FIGURE 10. I_{CCH}, I_{CCL} for AND, NAND Circuits

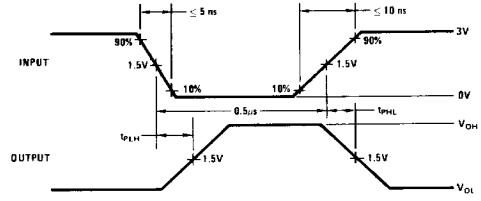


Both gates are tested simultaneously.

FIGURE 11. I_{CCH}, I_{CCL} for OR, NOR Circuits

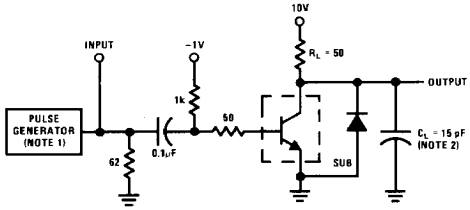
Switching Characteristics

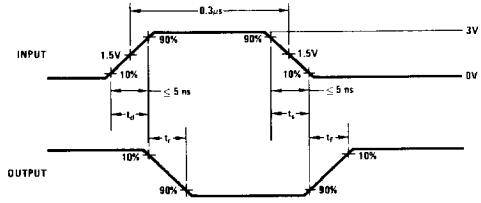




Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} ≈ 50Ω.
Note 2: C_L includes probe and jig capacitance.

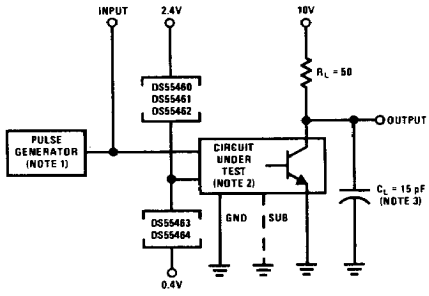
FIGURE 12. Propagation Delay Times, Each Gate (DS55460 and DS75460 Only)

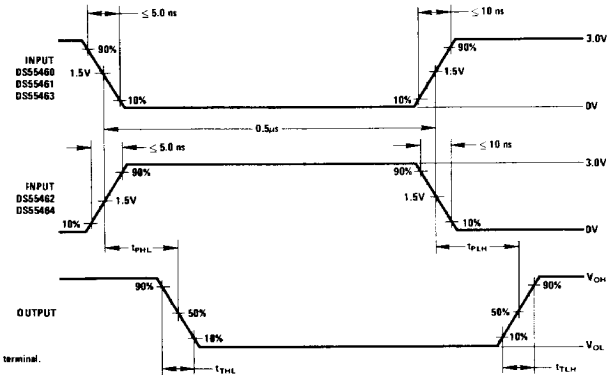




Note 1: The pulse generator has the following characteristics: duty cycle ≤ 1%, Z_{OUT} ≈ 50Ω.
Note 2: C_L includes probe and jig capacitance.

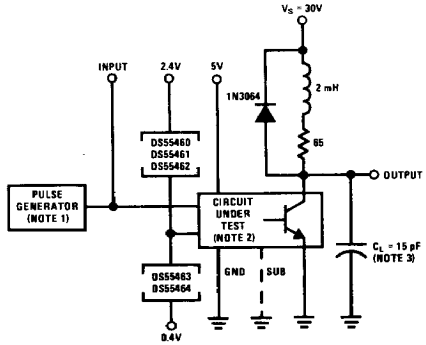
FIGURE 13. Switching Times, Each Transistor (DS55460 and DS75460 Only)

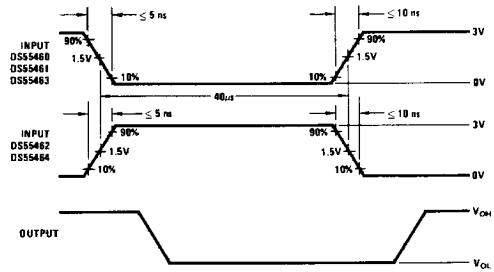




Note 1: The pulse generator has the following characteristics: PRR = 1 MHz, Z_{OUT} ≈ 50Ω.
Note 2: When testing DS55460 or DS75460, connect output Y to transistor base and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 14. Switching Times of Complete Drivers





Note 1: The pulse generator has the following characteristics: PRR = 12.5 kHz, Z_{OUT} = 50Ω.
Note 2: When testing DS5546 or DS75460, connect output Y to transistor base with a 500Ω resistor from there to ground, and ground the substrate terminal.
Note 3: C_L includes probe and jig capacitance.

FIGURE 15. Latch-Up Test of Complete Drivers