UNITRODE

PRELIMINARY

Low Voltage Differential SCSI (LVD) 27 Line Regulator Set

FEATURES

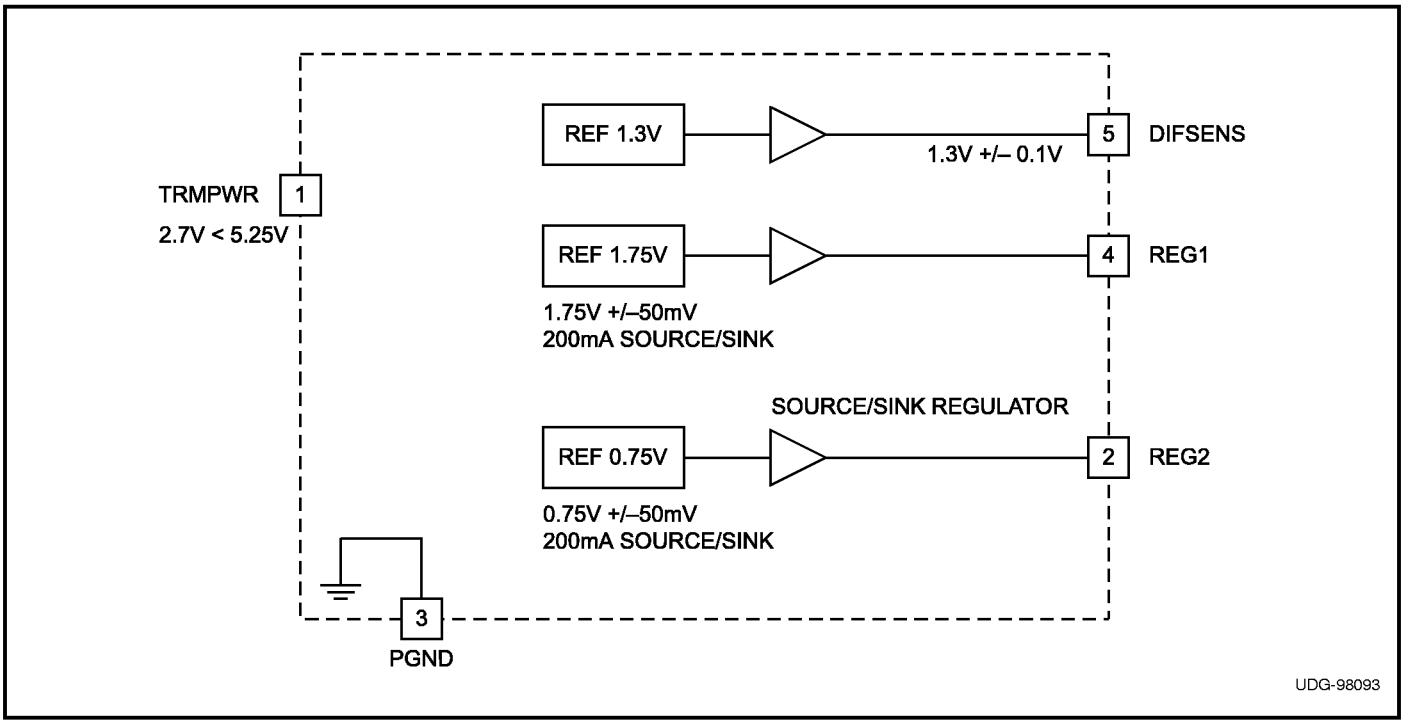
- SCSI SPI-2 LVD SCSI 27 Line Low Voltage Differential Regulator
- 2.7V to 5.25V Operation
- Integrated Regulator Set for LVD SCSI
- Differential Failsafe Bias

DESCRIPTION

The UCC561 LVD Regulator set is designed to provide the correct references voltages and bias currents for LVD termination resistor networks (475Ω, 121Ω, and 475Ω). The device also provides a 1.3V output for Diff Sense signaling. With the proper resistor network, the UCC561 solution will meet the common mode bias impedance, differential bias, and termination impedance requirements of SPI-2 (Ultra2).

This device incorporates into a single monolith, two sink/source reference voltage regulators, a 1.3V buffered output and protection features. The protection features include thermal shut down and active current limiting circuitry. The UCC561 is offered in 16-pin SOIC(DP), 5-pin TO263(TD), and 5-pin TO-220(T) packaging,

BLOCK DIAGRAM



Pinout refers to the 5 pin TO220 and TO263 packages.

ABSOLUTE MAXIMUM RATINGS

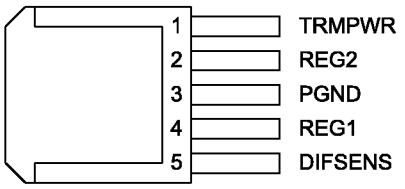
TERMPWR . . . . . +6V
Package Dissipation 3W
Junction Temperature . . . . . –55°C to +150°C
Storage Temperature . . . . . –65°C to +150°C

Currents are positive into, negative out of the specified terminal. Consult Packaging Section of Databook for thermal limitations and considerations of packages.

RECOMMENDED OPERATING CONDITIONS

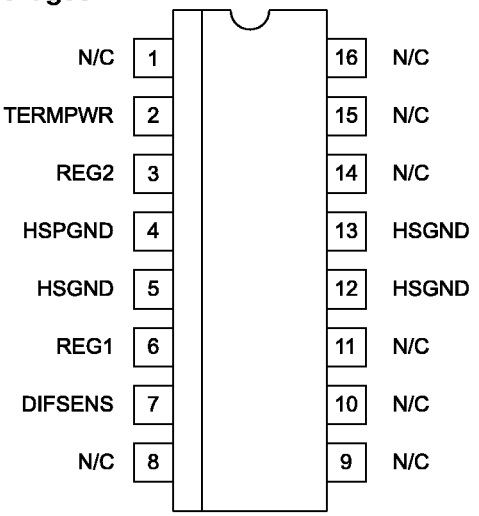
TERMPWR Voltage . . . . . 2.7V to 5.25V

TO220-5 , TO263-5 (TOP VIEW)
T or TD Packages



CONNECTION DIAGRAMS

SOIC-16 (TOP VIEW)
DP Packages



ELECTRICAL CHARACTERISTICS: Unless otherwise specified these specifications apply for TA = 0°C to 70°C, TERMPWR = 3.3V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TERMPWR Supply Current Section					
TERMPWR Supply Current	No Load			40.0	mA
TERMPWR Voltage		2.7		5.25	V
Regulator Section					
1.75 Volt Regulator	REG1 (± 125mA)	1.7	1.75	1.8	V
1.3 Volt Regulator	DIFSENS , No Load	1.2	1.3	1.4	V
0.75 Volt Regulator	REG2 (± 125mA)	0.7	0.75	0.8	V
1.75 Volt Regulator Source Current	(1.25V)	–200			mA
1.75 Volt Regulator Sink Current	(2.25V)	200			mA
1.75 Sink Current Limit				600	mA
1.75 Source Current Limit		–600			mA
1.3 Volt Regulator Source Current	DIFSENS, GND	–5		–15	mA
1.3 Volt Regulator Sink Current	DIFSENS, 2.4V	50		200	mA
0.75 Volt Regulator Source Current	0.25V	–200			mA
0.75 Volt Regulator Sink Current	1.25V	200			mA
0.75 Current Limit				600	mA
0.75 Current Limit		–600			mA

Note 1: Guaranted by design. Not 100% tested in production.

APPLICATION INFORMATION

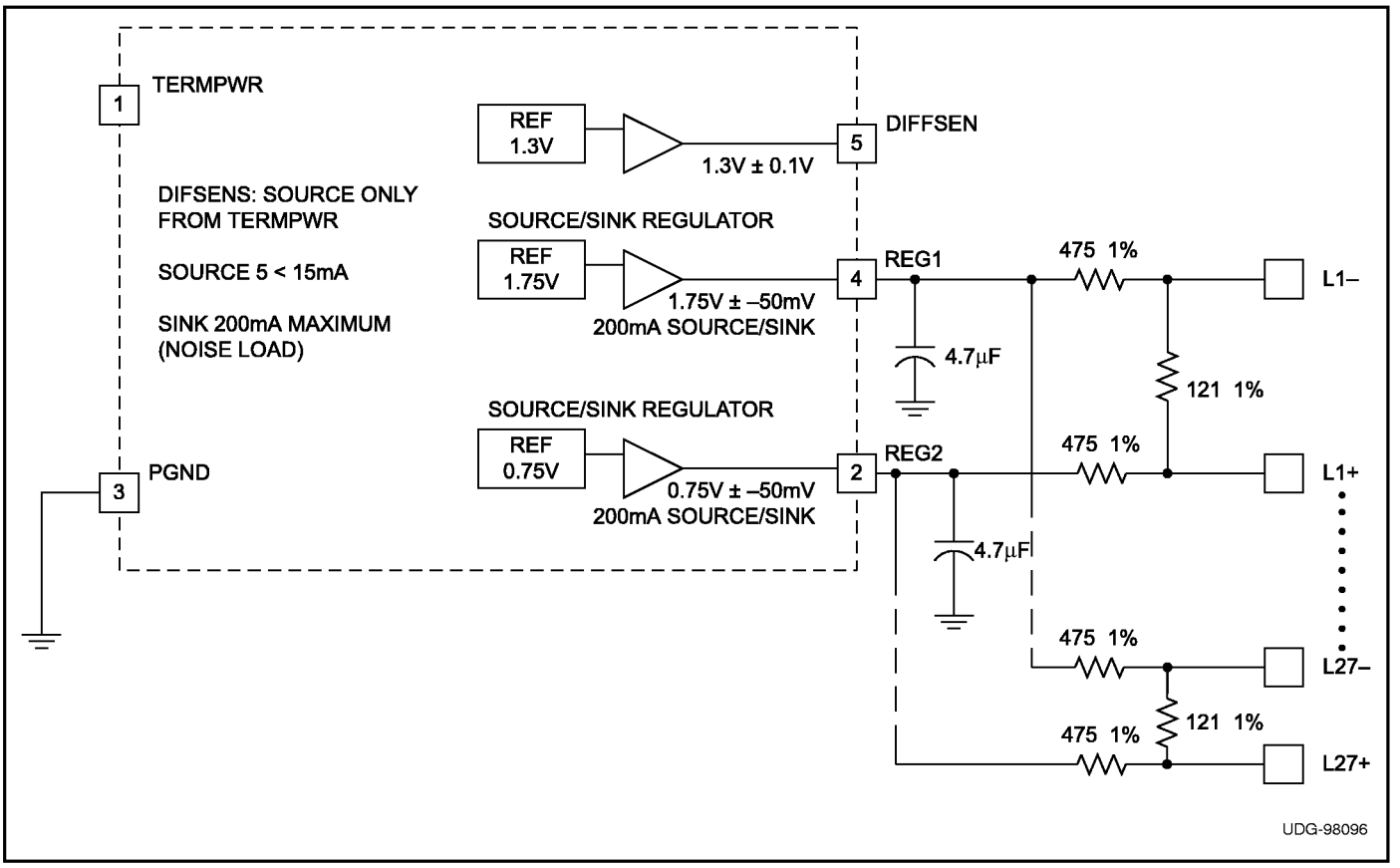


Figure 1. LVD SCSI Discrete Resistor Stack

Table I. Resistor Stack vs. Standard

Outputs	Specification
107.3Ω Diff	100Ω to 110Ω
112.9mV Diff Bias	100mV to 125mV
237Ω Common Mode	100Ω to 300Ω
1.25V Common Mode	1.2V to 1.30V

Application Note: The resistor stack with the 1.75V and 0.75V reference will give the correct differential impedance, bias voltage, common mode differential impedance and common mode voltage as show in Table 1.

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Mechanical Drawings

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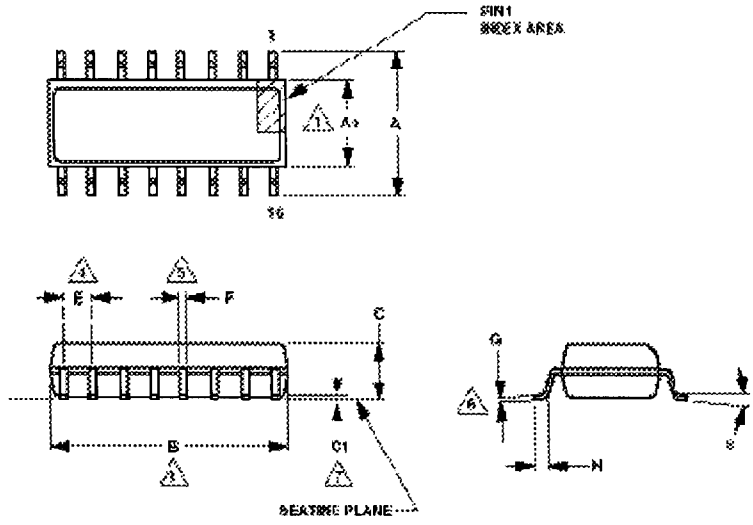
16-PIN SOIC SURFACE MOUNT~ D, DP, DS PACKAGE SUFFIX

DIMENSIONS				
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.228	.244	5.80	6.20
A1	.150	.158	3.80	4.00
B	.386	.393	9.80	9.98
C	.053	.069	1.35	1.75
C1	.004	.009	0.10	0.22
E	.050 BSC		1.27 BSC	
F	.014	.019	0.36	0.48
G	.007	.010	0.19	0.25
H	.016	.035	0.41	0.89
θ	0°	8°	0°	8°



NOTES:

1. 'A1' AND 'B' DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 IN. PER SIDE.
2. LEADS SHALL BE COPLANAR WITHIN 0.004 IN. AT THE SEATING PLANE.
3. THE BASIC LEAD SPACING IS 0.050 IN. BETWEEN CENTERLINES. EACH LEAD CENTERLINE SHALL BE LOCATED WITHIN ±0.004 IN. OF ITS EXACT TRUE POSITION.
4. CONTROLLING DIMENSION: INCHES. MILLIMETERS SHOWN FOR REFERENCE ONLY.
5. DIMENSION 'F' DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 'F' MAXIMUM BY MORE THAN 0.003 IN. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
6. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.004 IN. AND 0.010 IN. FROM THE LEAD TIP.
7. 'C1' IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY (BASE PLANE).

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