Signetics

74AC/ACT11175

Quad D-Type Flip-Flop w/Reset; Positive-Edge Trigger

Preliminary Specification

ACL Products

FEATURES

- **Output capability: ±24 mA**
- **CMOS (AC) and TTL (ACT) voltage level inputs**
- **50Ω incident wave switching**
- **Center-pin V_{CC} and ground configuration to minimize high-speed switching noise**
- **I_{CC} category: MSI**

DESCRIPTION

The 74AC/ACT11175 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11175 provides four D-type flip-flops with independent Data inputs, shared Clock and Master Reset inputs, and complementary Q and $\overline{Q}$ outputs.

Master Reset ($\overline{MR}$) is an asynchronous active-Low input and operates independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the Low-to-High transition of the clock pulse. Clock triggering is threshold voltage dependent. The D inputs must be stable one set-up time prior to the Low-to-High clock transition for predictable operation.

GENERAL INFORMATION

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL		UNIT
			AC	ACT	
t_{PLH}/t_{PHL}	Propagation delay CP to Q_n or $\overline{Q}_n$	C_L = 50pF	6.3	7.3	ns
C_{PD}	Power dissipation capacitance per flip-flop[1]	f = 1MHz; C_L = 50pF	47	42	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	3.5	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	135	120	MHz

Note:

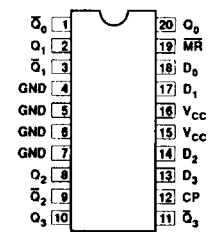
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_I + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_I = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

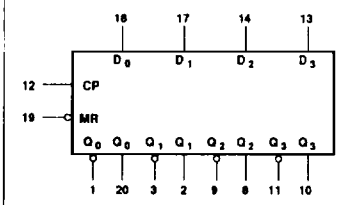
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11175N 74ACT11175N
20-pin plastic SO (300mil-wide)	-40°C to +85°C	74AC11175D 74ACT11175D

PIN CONFIGURATION

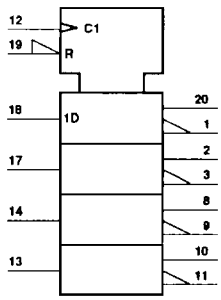
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



PIN DESCRIPTION

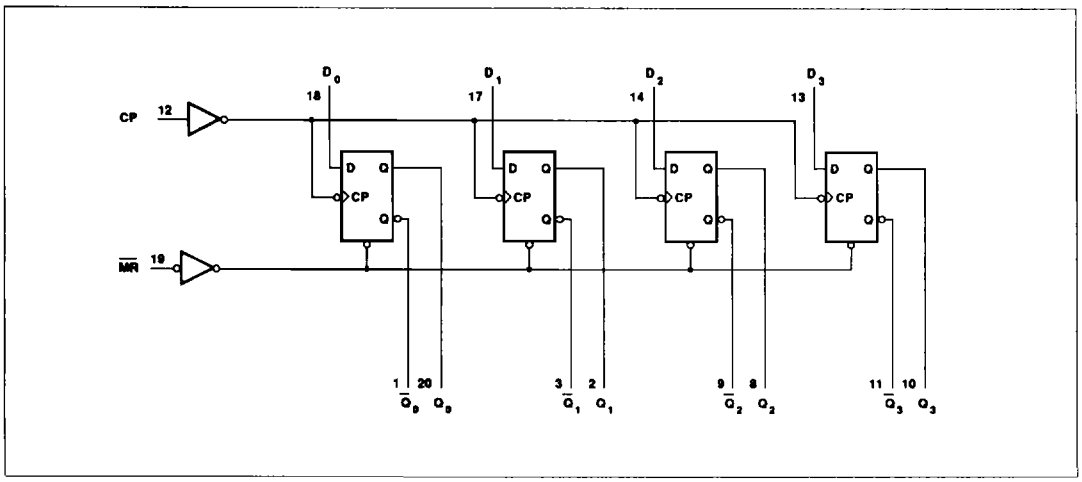
PIN NUMBER	SYMBOL	NAME AND FUNCTION
18, 17, 14, 13	D_0 - D_3	Data inputs
20, 2, 8, 10	Q_0 - Q_3	Data outputs
1, 3, 9, 11	$\overline{Q}_0$ - $\overline{Q}_3$	Data outputs (complements of Q_n outputs)
19	$\overline{MR}$	Master reset input (active Low)
12	CP	Clock input
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS	
	$\overline{MR}$	CP	D_n	Q_n	$\overline{Q}_n$
Asynchronous reset	L	X	X	L	H
Load "1" (set)	H	↑	h	H	L
Load "0" (reset)	H	↑	l	L	H

H = High voltage level steady state
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level steady state
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Quad D-Type Flip-Flop w/Reset; Positive-Edge Trigger

74AC/ACT11175

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74AC11175			74ACT11175			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_A	Operating free-air temperature	-40		+85	-40		+85	°C

NOTE:

1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to+7.0	V
I_{IK} or V_I	DC input diode current[2]	$V_I < 0$	-20	mA
		$V_I > V_{CC}$	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	$V_O < 0$	-50	mA
		$V_O > V_{CC}$	50	
	DC output voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±200	mA
	DC ground current		±200	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package Plastic DIP	Above 70°C:derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C:derate linearly by 6mW/K	400	mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11175				74ACT11175				UNIT
					T_A = +25°C		T_A = -40°C to +85°C		T_A = +25°C		T_A = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

AC ELECTRICAL CHARACTERISTICS AT 3.3V ±0.3V

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	115		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	7.8 10.8	10.0 13.7	1.5 1.5	10.9 14.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	7.9 11.4	9.8 13.7	1.5 1.5	10.6 14.6	ns
t_S	Setup time, High or Low D_n to CP	1	8.0			8.0		ns
t_H	Hold time, High or Low CP to D_n	1	0.0			0.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

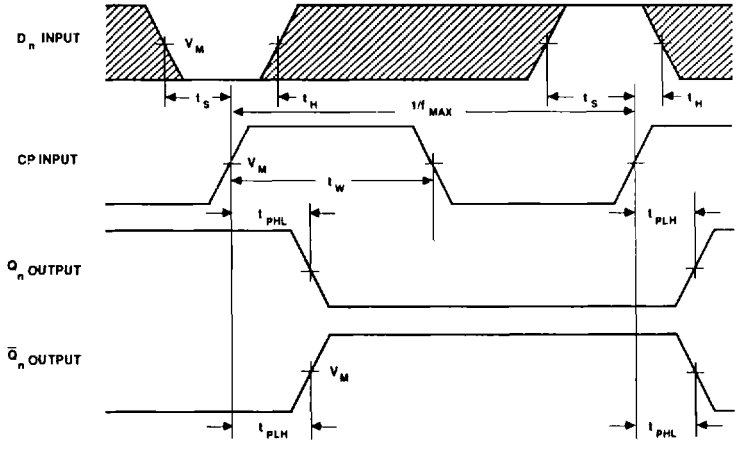
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	135		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	5.4 7.2	7.2 9.8	1.5 1.5	7.8 10.7	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	5.4 8.1	7.0 9.8	1.5 1.5	7.5 10.7	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	0.5			0.5		ns
t_W	Clock pulse width High or Low	1	4.5			4.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.0			1.0		ns

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

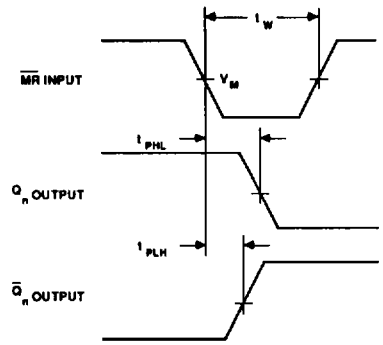
SYMBOL	PARAMETER	WAVEFORM	74ACT11175					UNIT
			T_A = +25°C			T_A = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	120		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n, $\overline{Q}_n$	1	1.5 1.5	6.1 8.4	7.8 10.6	1.5 1.5	8.3 11.6	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{MR}$ to Q_n, $\overline{Q}_n$	2	1.5 1.5	6.9 9.5	8.4 11.6	1.5 1.5	8.9 12.5	ns
t_S	Setup time, High or Low D_n to CP	1	5.5			5.5		ns
t_H	Hold time, High or Low CP to D_n	1	1.0			1.0		ns
t_W	Clock pulse width High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	3	1.5			1.5		ns

AC WAVEFORMS

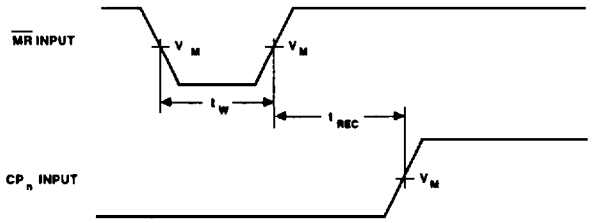


Waveform 1. Waveforms Showing Clock to Output Delays, Data Setup, and Clock Pulse Width

AC WAVEFORMS (Continued)



Waveform 2. Waveforms Showing Master Reset to Output Delay and Master Reset Pulse Width

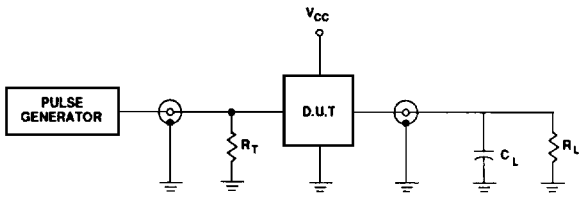


Waveform 3. Waveforms Showing Recovery Time

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	V_M = 50% V_{CC}

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns