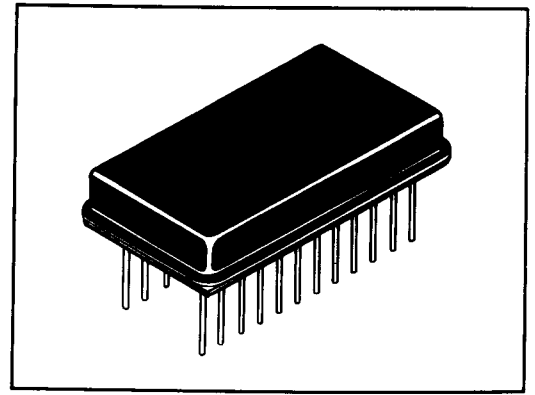


4065

12 Bit/60nsec Current Output D/A Converter



The 4065 is a true 12 bit, straight binary, current-output digital to analog converter with TTL compatible inputs and externally programmable output ranges of 0 to +4mA and ± 2 mA. Its speed and the low capacitance of the resistor network are responsible for the 4065's ability to settle a full 4mA step to $\pm 0.01\%$ FSR in 100nsec maximum.

The 4065 is packaged in an industry-standard, hermetically sealed, metal, 24 pin dual-in-line package. Active laser trimming results in integral and differential linearity errors guaranteed not to exceed $\pm 1/2$ LSB and an initial offset error no greater than $\pm 1/2$ LSB. For the most critical applications, external gain and offset adjustments are user optional. The 4065 operates from ± 15 V supplies with no need for a +5V logic supply. Power consumption, at 645mW maximum, is extremely low for a device of this speed.

The standard 4065 is fully specified for 0°C to +70°C operation. The -83 version is specified over the -55°C to +125°C temperature range and meets the high reliability requirements of MIL-STD-883C, Class "B". This device may also be ordered screened to Class "S".

FEATURES

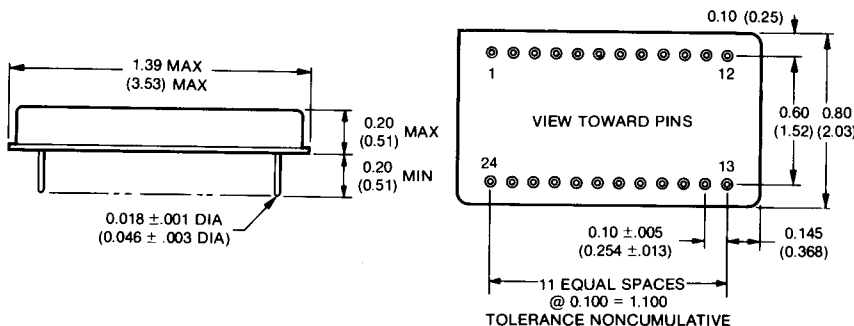
- 60nsec Settling 4mA Step to $\pm 1/2$ LSB Max.
- $\pm 1/2$ LSB Max. Integral and Differential Nonlinearities
- Monotonicity Guaranteed Over Temperature
- Power Consumption 645mW Max.
- -55°C to +125°C Operation

APPLICATIONS

- Military Environments
- High Reliability Industrial Equipment
- Data Distribution Systems
- Fast A to D Converters
- Precision Displays
- Portable Instrumentation

PACKAGE DIMENSIONS

Dimensions are in inches. Those in parentheses are expressed in centimeters.



PIN DESIGNATION	
1. BIT 12 (LSB)	24. -10V REF. OUT
2. BIT 11	23. -15V SUPPLY
3. BIT 10	22. POWER GROUND
4. BIT 9	21. +15V SUPPLY
5. BIT 8	20. 20V SCALE
6. BIT 7	19. 10V SCALE
7. BIT 6	18. BIPOLAR OFFSET
8. BIT 5	17. GAIN ADJUST
9. BIT 4	16. ANALOG GROUND
10. BIT 3	15. N/C
11. BIT 2	14. N/C
12. BIT 1 (MSB)	13. Iout

ABSOLUTE MAXIMUM RATINGS

+15V Supply (+V _{cc} , Pin 21)	+18V
-15V Supply (-V _{cc} , Pin 23)	-18V
Digital Input Voltage (Pins 1-12)	0 to +7V
Output Short Circuit Duration (1)	Continuous to Ground
Operating Temperature Range	-55°C to +125°C
Specified Temperature Range	
4065	0°C to +70°C
4065-83 (2)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

SPECIFICATIONS (T_A = +25°C, ±V_{cc} = ±15V, unless otherwise indicated.)

PARAMETER	MIN.	TYP.	MAX.	UNITS
DIGITAL INPUTS				
Logic Levels: Logic "1"	+2.0	---	+5.5	V
Logic "0"	0	---	+0.8	V
Loading (3)	---	---	1	TTL Load
Logic Coding: Unipolar Range	---	Straight Binary	---	---
Bipolar Range	---	Offset Binary	---	---
ANALOG OUTPUT				
Output Range: Unipolar	---	0 to +4	---	mA
Bipolar	---	±2	---	mA
Compliance Voltage	±0.6	---	---	V
Output Resistance: Unipolar	---	1.5	---	kΩ
Bipolar	---	1.2	---	kΩ
TRANSFER CHARACTERISTICS				
Integral Linearity Error: +25°C	---	±¼	±½	LSB
0 to +70°C (4065)	---	±½	---	LSB
-55°C to +125°C (4065-83)	---	±½	---	LSB
Differential Linearity Error	---	±¼	±½	LSB
Guaranteed Monotonicity: 4065	0	---	+70	°C
4065-83	-55	---	+125	°C
Zero Offset Error (4): Unipolar (000...000)	---	±¼	±½	LSB
Bipolar (100...000)	---	±¼	±½	LSB
Gain Error (4) (5)	---	±0.1	±1	%
STABILITY				
Zero Offset Drift: Unipolar	---	±0.5	±1	ppm of FSR/°C
Bipolar	---	±3	±10	ppm of FSR/°C
Gain Drift (6)	---	±7	±20	ppm/°C
Reference Drift	---	±5	±15	ppm/°C
Power Supply Rejection Ratio	---	±0.001	±0.0024	%FSR/%V _s
Warm Up Time to Within ±1LSB	---	30	---	Seconds
DYNAMIC CHARACTERISTICS				
Settling Time (4mA Step to ±½LSB)	---	60	100	nsec
REFERENCE				
Voltage	---	-10.0	---	V
Accuracy	---	±1	---	%
External Load	---	---	2	mA
POWER SUPPLIES				
Range	---	±2	---	%
Current Drain: +15V Supply	---	+20	+25	mA
-15V Supply	---	-13	-18	mA
Power Consumption	---	495	645	mW

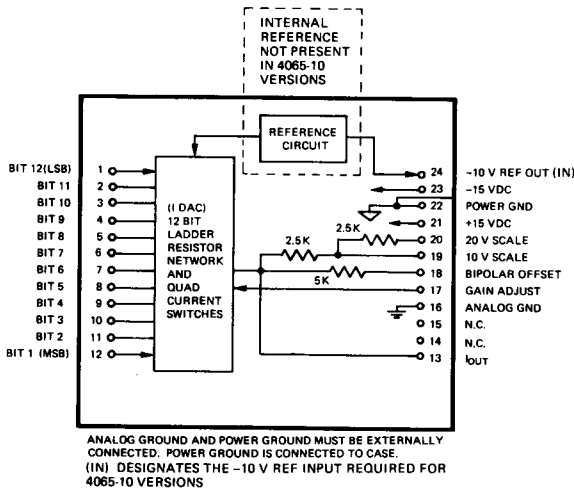
NOTES

- The 4065's output can withstand a continuous short to ground. The reference output (pin 24) can withstand a short for approximately 2 seconds.
- Screened to the high reliability requirements of MIL-STD-883C, Class "B". May also be ordered screened to Class "S".
- A TTL load is defined as sinking 40μA with a logic "1" applied and sourcing 1.6mA with a logic "0" applied.
- Adjustable to zero with optional external trim potentiometer.
- Gain error is defined as the error in the slope of the converter transfer function. It is expressed as a percentage and is equivalent to the deviation (divided by the ideal value) between the actual and the ideal value for the full output current span from the 0000 0000 0000 output to the 1111 1111 1111 output.
- Gain drift is measured using the internal feedback resistors. Using an external resistor, the gain drift is typically 35ppm/°C.

APPLICATIONS INFORMATION

Grounding and Bypassing

High speed systems require added care in power distribution for maximum accuracy and speed. Although power supply inputs on the 4065 are internally bypassed with 0.01 μ F ceramic capacitors, it is recommended that an additional 1 μ F tantalum capacitor be added externally between each supply input and analog ground for optimum performance. It is important to realize that power ground (pin 22) is internally connected to the case and must be connected to system analog ground to minimize ground loop errors. It is preferable to have the 4065's analog and power ground pins soldered directly to a large analog ground plane beneath the 4065.



Functional Block Diagram

Logic Inputs

Logic inputs are standard TTL/DTL compatible. If any bits are not used, it is recommended they be grounded since an "open" bit input line is equivalent to a logic "1". Opening the bit lines should not, however, be used as a means of generating a logic "1" due to the possibilities of noise pickup. The table below shows the binary input code used by the 4065. If desired, virtually any other binary code can be used with the addition of the necessary external logic.

DIGITAL INPUT CODING

ANALOG OUTPUT	DIGITAL INPUT	
	Unipolar Binary	Bipolar Offset Binary
Current		
-F.S.	---	000...000
-1/2 F.S.	---	010...000
-1LSB	---	011...111
0	000...000	100...000
+1LSB	000...001	100...001
+1/2 F.S.	100...000	110...000
+F.S.-1LSB	111...111	111...111

Output Range Selection

The table below shows pin connections for 4065 output range selection.

OUTPUT		PIN PROGRAMMING
Output Range	Output Pin	Jumper Pin 18 to
0 to +4mA	Pin 13	---
\pm 2mA	Pin 13	Pin 24

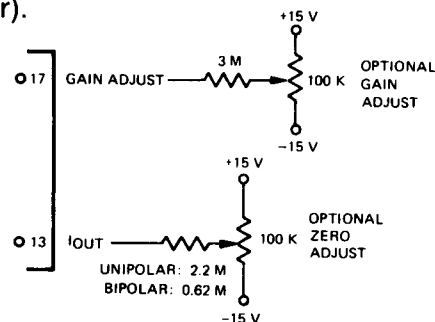
Optimizing Settling Time

To optimize settling time of the 4065 and to make the settling time independent of the characteristics of the digital driver, 2.2k Ω 1/8 Watt pull-down resistors are recommended at all logic inputs.

Trim Procedures

Initial zero and gain errors may be trimmed to zero using external potentiometers as shown in the diagram below. Adjustments should be made following warm-up, and to avoid interaction, zero should be adjusted before gain. Fixed resistors can be \pm 20% carbon composition or better. Multi-turn potentiometers with TCRs of 100ppm/ $^{\circ}$ C or less are recommended to minimize drift with temperature.

Offset Adjustment — When utilizing the internal feedback resistors with an external amplifier, set the digital input code to 000...000, and adjust the offset trim potentiometer for zero voltage (unipolar) or plus full scale voltage (bipolar) at the amplifier output. For current output operation, set the digital input code to 000...000, and adjust the offset trim potentiometer for zero output current (unipolar) or minus full scale output current (bipolar).



External Gain and Offset Adjust

Gain Adjustment — When utilizing the internal feedback resistors with an external amplifier, set the digital input code to 111...111, and adjust the gain trim potentiometer for minus full scale plus 1LSB voltage at the amplifier output. For current output operation, set the digital input code to 111...111, and adjust the gain trim potentiometer for plus full scale minus 1LSB output current.