ABRIDGED VERSION

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SSI 32P4903A

PRML Read Channel with PR4, 8/9 ENDEC, 4-burst Servo

Advance Information

January 1996

DESCRIPTION

The SSI 32P4903A is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 24 to 90 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8,9 GCR ENDEC, data synchronizer, time base generator, and 4-burst servo capture.

Programmable functions such as data rate, filter cutoff, filter boost, etc., are controlled by writing to the serial port registers so no external component changes are required to change zones.

The SSI 32P4903A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption. The part requires a single +5V power supply.

FEATURES

GENERAL

- Register programmable data rates from 24 to 90 Mbit/s
- Sampled data read channel with Viterbi qualification
- Programmable filter for PR4 equalization
- Three tap transversal filter for adaptive PR4 equalization
- 8/9 GCR ENDEC
- Data Scrambler/Descrambler
- Programmable write precompensation
- Low operating power (0.75W typical at 5V)
- Register programmable power management
- Dual-bit and byte wide bi-directional NRZ data interfaces
- Serial interface port for access to internal program storage registers
- Single power supply (5V ±10%)
- Small footprint 80-lead TQFP package

AUTOMATIC GAIN CONTROL

- Dual mode AGC, analog during acquisition, sampled during data reads
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents for data reads
- Charge pump currents track programmable data rate during data reads
- Low drift AGC hold circuitry
- Low Z input switch
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

FILTER/EQUALIZER

- Programmable, 7-pole, continuous time filter provides
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency, 3 to 24 MHz
  - Programmable boost /equalization, 0 to 13 dB
  - ±0.6 ns group delay variation from 0.2 fc to fc, with fc = 24 MHz
  - Minimizes size and power
  - Low Z input switch
- Three tap self adapting transversal filter for fine equalization to PR4
- No external components required

PULSE QUALIFICATION

- Sampled Viterbi qualification of signal equalized to PR4
- Dual level pulse qualifier for servo reads

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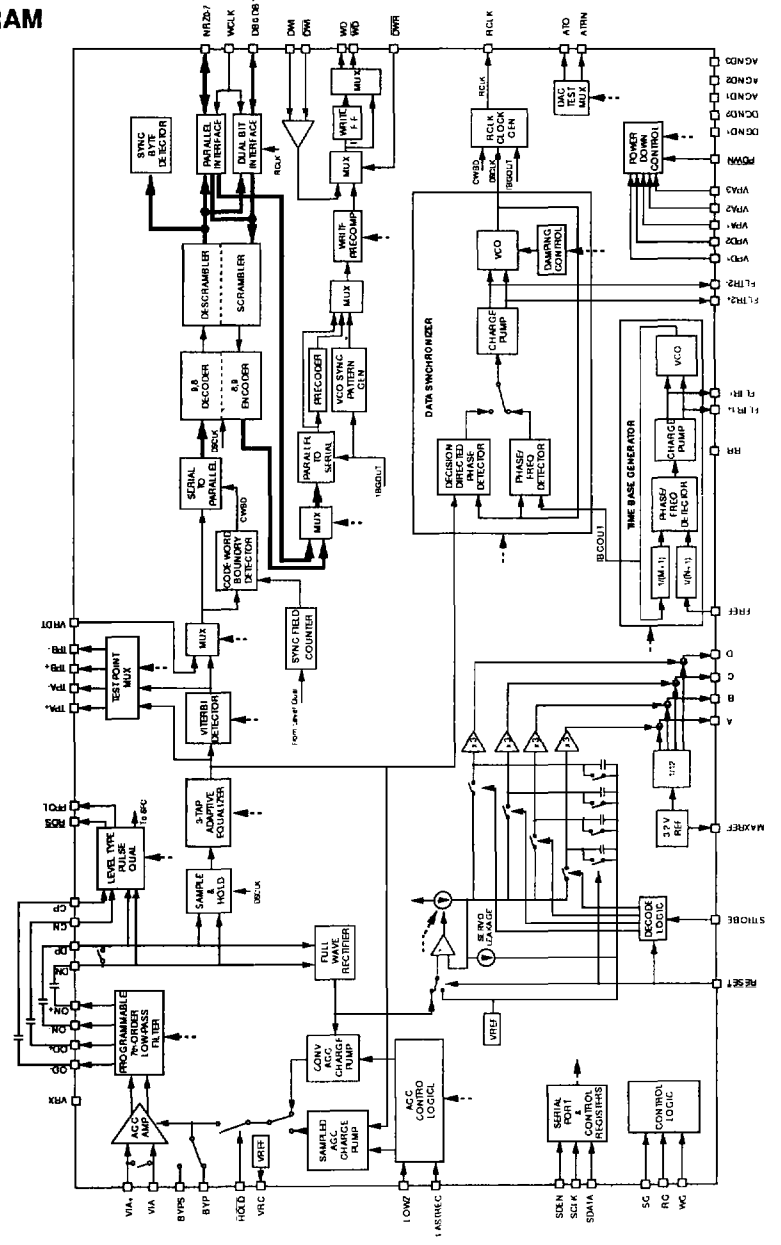
BLOCK DIAGRAM



FEATURES (continued)

TIME BASE GENERATOR

- Less than 1% frequency resolution
- Up to 101 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR

- Fully integrated data separator includes data synchronizer and 8,9 GCR ENDEC
- Register programmable to 80 Mbit/s operation
- Fast Acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive (+) and (-) clock recovery thresholds for use with asymmetrical amplitude signals (e.g., from MR heads)
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- Dual-bit and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync byte detection

SERVO

- Four-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- "Soft Landing" charge pump architecture
- Separate, automatically selected, registers for servo fc, boost, and threshold
- Programmable charge pump current
- Wide bandwidth, precision full-wave rectifier

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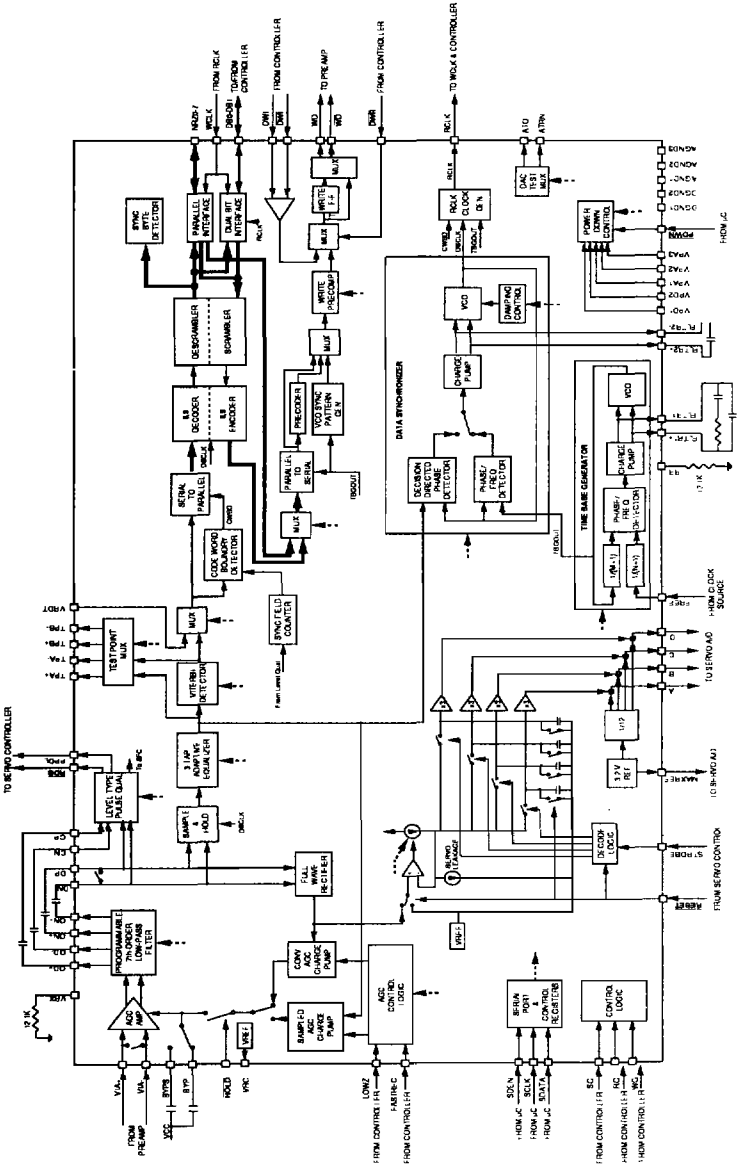
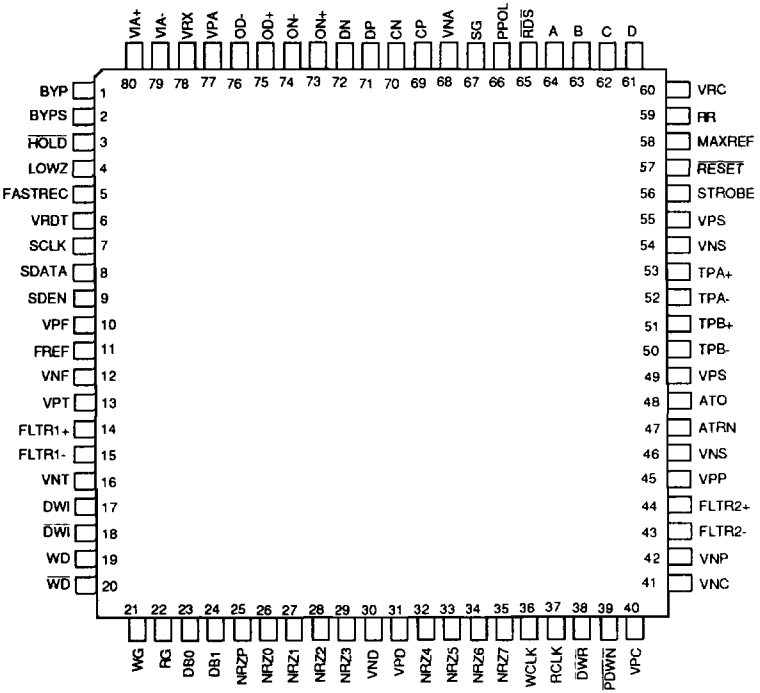


FIGURE 1: SSI 32P4903 Application Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



80-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: *Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.*

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