HARRIS

HI-565A/883

High Speed, Monolithic Digital-to-Analog Converter With Reference

January 1989

Features

- **This Circuit Is Processed In Accordance to Mil-Std-883 and Is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **DAC and Reference on a Single Chip**
- **Pin Compatible With AD565A**
- **Very High Speed: Settles to 1/2 LSB In 500ns Max**
- **Monotonicity Guaranteed Over Temperature**
- **1/2 LSB Max Nonlinearity Guaranteed Over Temp**
- **Low Gain Drift (Max, DAC Plus Reference) .. 25ppm/°C**
- **Low Power Dissipation (Max Over Temp) 425mW**

Applications

- **High Speed A/D Converters**
- **Precision Instrumentation**
- **CRT Display Generation**
- **Signal Reconstruction**

Description

The HI-565A/883 is a fast, 12 bit current output, digital to analog converter. The monolithic chip includes a precision voltage reference, thin-film R-2R ladder, reference control amplifier and twelve high-speed bipolar current switches.

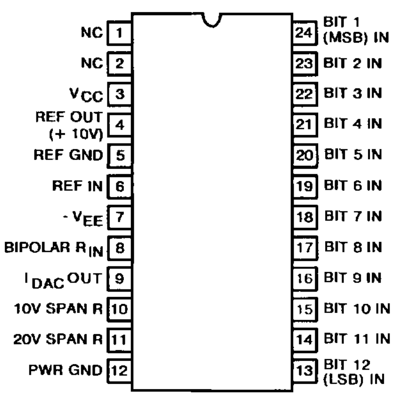
The Harris Semiconductor Dielectric Isolation process provides latch-free operation while minimizing stray capacitance and leakage currents, to produce an excellent combination of speed and accuracy. Also, ground currents are minimized to produce a low and constant current through the ground terminal, which reduces error due to code-dependent ground currents.

HI-565A/883 dice are laser trimmed for a maximum integral nonlinearity error of ±1/4 LSB at +25°C. In addition, the low noise buried zener reference is trimmed both for absolute value and minimum temperature coefficient.

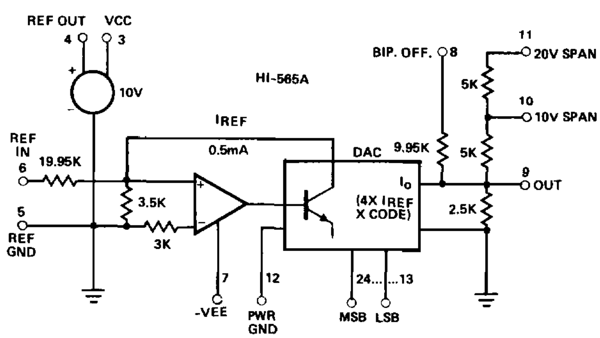
The HI-565A/883 is packaged in a 24 pin Ceramic Sidebrazed DIP.

Pinout

HA1-565A/883 (CERAMIC SIDEBRAZED DIP)
TOP VIEW



Functional Diagram



Absolute Maximum Ratings (Note 1)

Power Supply Inputs (Referred to Power GND)
- V_{CC} .... +18V
- $-V_{EE}$ .... -18V

Reference (Referred to Ref. GND)
- Input .... ±12V
- Output .... Indefinite Short to Power GND

Analog Output .... -3V to +12V

Bipolar Offset (Referred to Ref. GND) .... ±12V

Digital Inputs
- Bits 1 to 12 .... -1V to +7V

Storage Temperature Range .... -65°C to +150°C

Lead Temperature (Soldering 10s) .... 275°C

Junction Temperature .... 175°C

Thermal Information

Thermal Resistance, Junction-to-Case (θ_{jc})
- Ceramic DIP Package .... 19°C/W

Thermal Resistance Junction-to-Ambient (θ_{ja})
- Ceramic DIP Package .... 79°C/W

Power Dissipation at 75°C
- Ceramic DIP Package 1270mW

Power Dissipation Derating Factor (Above +75°C)
- Ceramic DIP Package .... 12.7mW/°C

Recommended Operating Conditions

Operating Temperature Range .... -55°C to +125°C

Operating Supply Voltages
- $+V_{CC}$ .... +12V to +15V
- $-V_{EE}$ .... -12V to -15V

Reference Input Voltage 10V

Logic Low Level .... 0V to 0.8V

Logic High Level .... 2.0V to +5.5V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, Reference In Connected to Reference Out, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	HI-565AS/883		HI-565AT/883		UNITS
					MIN	MAX	MIN	MAX	
Supply Current From V_{CC}	I_{CC}	All Bits = 2.0V	1	+25°C	-	11.8	-	11.8	mA
			2, 3	+125°C, -55°C	-	12.8	-	12.8	mA
Supply Current From V_{EE}	I_{EE}	All Bits = 2.0V	1	+25°C	-	-14.5	-	-14.5	mA
			2, 3	+125°C, -55°C	-	-15.5	-	-15.5	mA
Power Dissipation	PD	Calculated	1	+25°C	-	375	-	375	mW
			2, 3	+125°C, -55°C	-	425	-	425	mW
Digital Input High Current	I_{IH}	Bit Under Test = 5.5V, Others = 0.8V	1	+25°C	-400	400	-400	400	nA
			2, 3	+125°C, -55°C	-1	1	-1	1	μA
Digital Input Low Current	I_{IL}	Bit Under Test = 0V, Others = 0.8V	1	+25°C	-10	-	-10	-	μA
			2, 3	+125°C, -55°C	-20	-	-20	-	μA
Unipolar Offset Error	V_{OS}	All Bits = 0.8V Note 2	1	+25°C	-0.05	0.05	-0.05	0.05	% of FSR
			2, 3	+125°C, -55°C	-0.07	0.07	-0.07	0.07	% of FSR
Unipolar Gain Error	A_E	All Bits = 2.0V Note 2	1	+25°C	-0.25	0.25	-0.25	0.25	% of FSR
			2, 3	+125°C, -55°C	-0.55	0.55	-0.5	0.5	% of FSR
Power Supply Sensitivity to V_{CC}	$+P_{SS1}$	V_{CC} = 11.4V to 16.5V All Bits = 2.0V, Unipolar	1	+25°C	10	10	10	10	ppm of FSR / %ΔV_{CC}
			2, 3	+125°C, -55°C	20	20	20	20	
Power Supply Sensitivity to V_{EE}	$-P_{SS1}$	V_{EE} = -11.4V to -16.5V. All Bits = 2.0V Unipolar	1	+25°C	25	25	25	25	ppm of FSR / %ΔV_{EE}
			2, 3	+125°C, -55°C	50	50	50	50	
Output Current Unipolar	I_{OUT1}	I_{DAC} Out = 0V, All Bits = 2.0V	1	+25°C	-2.4	-1.6	-2.4	-1.6	mA
Output Current Bipolar	I_{OUT2}	$BIPR_{IN}$ Tied to V_{REF} All Bits = 2V, I_{DAC} = 0	1	+25°C	±0.8	±1.2	±0.8	±1.2	mA
Bipolar Offset Error	BPO_E	B.P. ±10V Range All Bits = 0.8V, Notes 2, 3	1	+25°C	-0.15	0.15	-0.1	0.1	% FSR
			2, 3	+125°C, -55°C	-0.25	0.25	-0.2	0.2	% FSR
Bipolar Zero Error	BPZ_E	B.P. ±10V Range, Note 2, MSB = 2V, Bit 1 thru 11 = 0.8V	1	+25°C	-0.15	0.15	-0.1	0.1	% FSR
			2, 3	+125°C, -55°C	-0.25	0.25	-0.2	-0.2	% FSR

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Devices Tested at $+V_{CC}$ = +15V, $-V_{EE}$ = -15V, Reference In Connected to Reference Out, Unless Otherwise Specified

D.C. PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	HI-565AS/883 MIN	HI-565AS/883 MAX	HI-565AT/883 MIN	HI-565AT/883 MAX	UNITS
Bipolar Gain Error	BPA_E	B.P.±10V Range All Bits = 2.0V, Note 2	1	+25°C	-0.25	0.25	-0.25	0.25	% FSR
			2, 3	+125°C, -55°C	-0.55	0.55	-0.5	0.5	% FSR
Integral Linearity Error	L_E	Note 2	1	+25°C	-0.5	0.5	-0.25	0.25	LSB
			2, 3	+125°C, -55°C	-0.75	0.75	-0.5	0.5	LSB
Differential Linearity Error	DL_E	Note 2	1	+25°C	-0.5	0.5	-0.5	0.5	LSB
			2, 3	+125°C, -55°C	-1	1	-1	1	LSB
Ref. Voltage (Unipolar)	$V_{REF(U)}$	No Load on V_{REF}, $V_{REF(OUT)}$ not tied to $V_{REF(IN)}$, All Bits = 0.8V	1	+25°C	9.95	10.05	9.95	10.05	V
			2, 3	+125°C, -55°C	9.95	10.05	9.95	10.05	V
Ref. Voltage (Bipolar)	$V_{REF(B)}$	No Load on V_{REF}, $V_{REF(OUT)}$ Not Tied To $V_{REF(IN)}$, All Bits = 0.8V	1	+25°C	9.95	10.05	9.95	10.05	V
			2, 3	+125°C, -55°C	9.95	10.05	9.95	10.05	V
Ref. Voltage (Loaded)	$V_{REF(L)}$	Pull Additional 1.5mA Out of V_{REF}. $V_{REF(OUT)}$ Tied to $V_{REF(IN)}$ and $BIPR_{IN}$. All Bits = 0.8V	1	+25°C	9.95	10.05	9.95	10.05	V
			2, 3	+125°C, -55°C	9.95	10.05	9.95	10.05	V
Unipolar Offset Drift	$\frac{dV_{OS}}{dT}$	Note 4	1, 2	+25°C to +125°C	-2.0	2.0	-2.0	2.0	ppm of FSR per °C
			1, 3	+25°C to -55°C	-2.0	2.0	-2.0	2.0	
Unipolar Gain Drift	$\frac{d_{AE}}{dT}$	Note 4	1, 2	+25°C to +125°C	-40	40	-25	25	
			1, 3	+25°C to -55°C	-40	40	-25	25	
Bipolar Zero Drift	$\frac{dBP_Z}{dT}$	Note 4	1, 2	+25°C to +125°C	-10	10	-10	10	
			1, 3	+25°C to -55°C	-10	10	-10	10	
Bipolar Gain Drift	$\frac{dBP_{AE}}{dT}$	Note 4	1, 2	+25°C to +125°C	-40	40	-25	25	
			1, 3	+25°C to -55°C	-40	40	-25	25	

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

This Table Intentionally Left Blank. See A.C. Parameters on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Characterized at V_{CC} = +15V, V_{EE} = -15V, $V_{REF(OUT)}$ Tied to $V_{REF(IN)}$, Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	HI-565AS/883 MIN	HI-565AS/883 MAX	HI-565AT/883 MIN	HI-565AT/883 MAX	UNITS
Settling Time	t_S	All Bits OFF to ON, and ON to OFF. 10V Unipolar Mode to 0.01%. V_{IL} = 0.8V V_{IH} = 3.5V, R_L = 50Ω	5	+25°C	-	500	-	500	ns

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLE 1)
Interim Electrical Parameters (Pre-Burn-In)	-
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

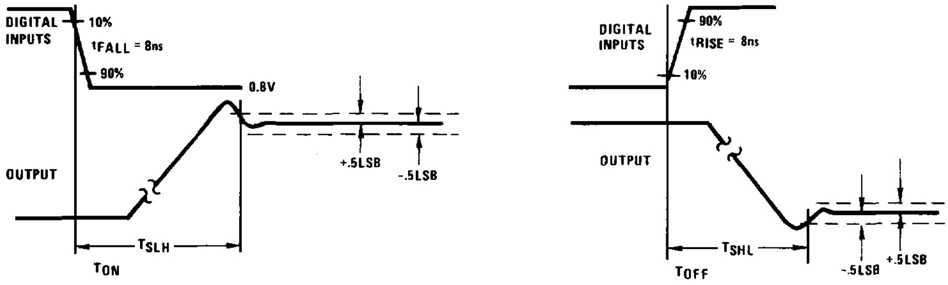
*PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

ELECTRICAL CHARACTERISTICS (Continued)

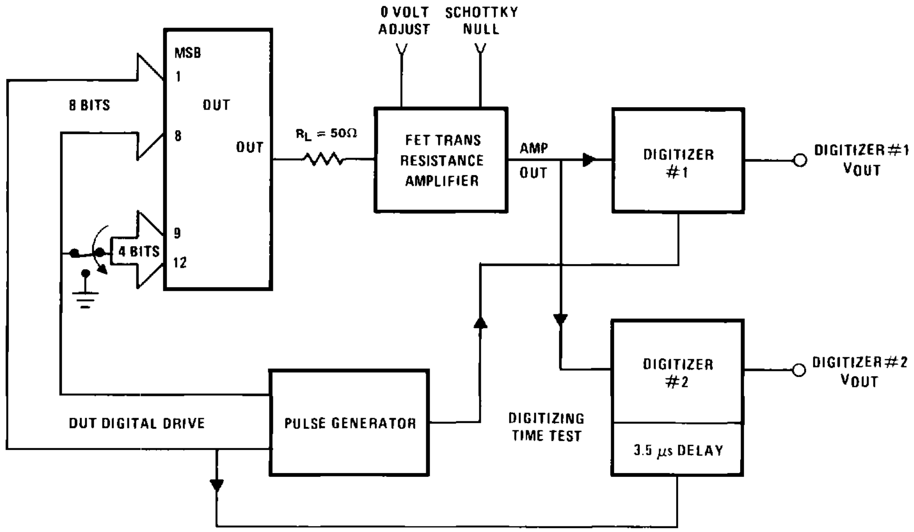
NOTES:
1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. An external reference voltage is set to the measured internal reference value - I_{REF} (50Ω)
3. Adjustable to zero using external potentiometers.
4. See Definitions.
5. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

Waveforms

SETTLING TIME



Test Circuit



SETTLING TIME TEST FIXTURE

CHART A.

DIGITAL CODE	NOTE	DIGITAL CODE	NOTE
MSB ———— LSB		MSB ———— LSB	
0 0 0 0 0 0 0 0 0 0 0 1		0 1 1 0 X X X X X X X X	7
0 0 0 0 0 0 0 0 0 0 1 0		0 1 1 1 X X X X X X X X	6
0 0 0 0 0 0 0 0 0 1 0 0		0 1 1 1 X X X X X X X X	7
0 0 0 0 0 0 0 0 1 0 0 0		1 0 0 0 X X X X X X X X	6
0 0 0 0 0 0 0 1 0 0 0 0		1 0 0 0 X X X X X X X X	7
0 0 0 0 0 0 1 0 0 0 0 0		1 0 0 1 X X X X X X X X	6
0 0 0 0 0 1 0 0 0 0 0 0		1 0 0 1 X X X X X X X X	7
0 0 0 0 1 0 0 0 0 0 0 0		1 0 1 0 X X X X X X X X	6
0 0 0 1 0 0 0 0 0 0 0 0		1 0 1 0 X X X X X X X X	7
0 0 1 0 0 0 0 0 0 0 0 0		1 0 1 1 X X X X X X X X	6
0 1 0 0 0 0 0 0 0 0 0 0		1 0 1 1 X X X X X X X X	7
1 0 0 0 0 0 0 0 0 0 0 0		1 1 0 0 X X X X X X X X	6
0 0 0 1 X X X X X X X X	6	1 1 0 0 X X X X X X X X	7
0 0 0 1 X X X X X X X X	7	1 1 0 1 X X X X X X X X	6
0 0 1 0 X X X X X X X X	6	1 1 0 1 X X X X X X X X	7
0 0 1 0 X X X X X X X X	7	1 1 1 0 X X X X X X X X	6
0 0 1 1 X X X X X X X X	6	1 1 1 0 X X X X X X X X	7
0 0 1 1 X X X X X X X X	7	1 1 1 1 X X X X X X X X	6
0 1 0 0 X X X X X X X X	6	1 1 1 1 X X X X X X X X	7
0 1 0 0 X X X X X X X X	7	X X X X X X X X X X X X	6
0 1 0 1 X X X X X X X X	6	X X X X X X X X X X X X	7
0 1 0 1 X X X X X X X X	7		
0 1 1 0 X X X X X X X X	6		

NOTES: 6. X = 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a positive error. X = 1 (V_{IH} = 2.0V) if the linearity error for that bit was measured as a negative error.

7. X = 0 (V_{IL} = 0.8V) if the linearity error for that bit was measured as a negative error. X = 1 (V_{IH} = 2.0V) if the linearity error error for that bit was measured as a positive error.

Integral Linearity Error Measurements

The transfer characteristics of the DUT are first determined by measuring its end points (all bits OFF, all bits ON). The end points of the reference DAC are then matched to the DUTs through software and hardware adjustments, to establish an ideal transfer characteristic for the DUT. The reference DAC then supplies one 12-bit LSB of current (DUT, all Bits OFF) to the input of the error amplifier and R_T* is adjusted to obtain an output of 1V. The integral linearity error, measured at the output of the error amplifier is a scaled voltage conversion of the difference between the ideal current supplied by the reference DAC through the DUT span resistor and the output current of the DUT for the code under test

LSB's of Error =

$$(\text{Ideal voltage} - \text{measured voltage}) \times \frac{\text{LSBs}}{\text{Volt}}$$

*R_T = Trim resistor in error amplifier

CHART B.

TO CODE	FROM CODE
MSB ———————— LSB	MSB ———————— LSB
0 0 0 0 0 0 0 0 0 0 0 1	0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 1 0	0 0 0 0 0 0 0 0 0 0 0 1
0 0 0 0 0 0 0 0 0 1 0 0	0 0 0 0 0 0 0 0 0 0 1 1
0 0 0 0 0 0 0 0 1 0 0 0	0 0 0 0 0 0 0 0 0 1 1 1
0 0 0 0 0 0 0 1 0 0 0 0	0 0 0 0 0 0 0 0 1 1 1 1
0 0 0 0 0 0 1 0 0 0 0 0	0 0 0 0 0 0 0 1 1 1 1 1
0 0 0 0 0 1 0 0 0 0 0 0	0 0 0 0 0 0 1 1 1 1 1 1
0 0 0 0 1 0 0 0 0 0 0 0	0 0 0 0 0 1 1 1 1 1 1 1
0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1
1 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1
0 0 0 1 0 0 0 0 0 0 0 0	0 0 0 0 1 1 1 1 1 1 1 1
0 0 1 0 0 0 0 0 0 0 0 0	0 0 0 1 1 1 1 1 1 1 1 1
0 0 1 1 0 0 0 0 0 0 0 0	0 0 1 0 1 1 1 1 1 1 1 1
0 1 0 0 0 0 0 0 0 0 0 0	0 0 1 1 1 1 1 1 1 1 1 1
0 1 0 1 0 0 0 0 0 0 0 0	0 1 0 0 1 1 1 1 1 1 1 1
0 1 1 0 0 0 0 0 0 0 0 0	0 1 0 1 1 1 1 1 1 1 1 1
0 1 1 1 0 0 0 0 0 0 0 0	0 1 1 0 1 1 1 1 1 1 1 1
1 0 0 0 0 0 0 0 0 0 0 0	0 1 1 1 1 1 1 1 1 1 1 1
1 0 0 1 0 0 0 0 0 0 0 0	1 0 0 0 1 1 1 1 1 1 1 1
1 0 1 0 0 0 0 0 0 0 0 0	1 0 0 1 1 1 1 1 1 1 1 1
1 0 1 1 0 0 0 0 0 0 0 0	1 0 1 0 1 1 1 1 1 1 1 1
1 1 0 0 0 0 0 0 0 0 0 0	1 0 1 1 1 1 1 1 1 1 1 1
1 1 0 1 0 0 0 0 0 0 0 0	1 1 0 0 1 1 1 1 1 1 1 1
1 1 1 0 0 0 0 0 0 0 0 0	1 1 0 1 1 1 1 1 1 1 1 1
1 1 1 1 0 0 0 0 0 0 0 0	1 1 1 0 1 1 1 1 1 1 1 1

Differential Linearity Error Measurements

The DUT and the reference DAC supply the code under test (less 1 LSB) to the input of the error amplifier, and the resulting output error is measured (E_1). The digital code of the DUT is then increased by 1 LSB and the output error is measured a second time (E_2). The differential linearity error is calculated as,

$$\frac{(E_2 - E_1)}{\text{Volts/LSB}} - 1 \text{ LSB} = \text{LSBs of error.}$$

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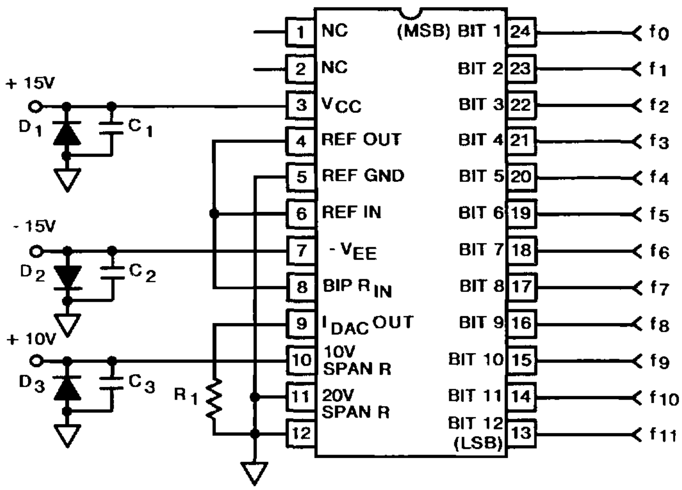
DATA CONVERSION PRODUCTS

Burn-In Circuit

HI-565A/883 CERAMIC SIDEBRAZE DIP



PARTS:

R_1 = 0Ω or Jumper Wire

$C_1 = C_2 = C_3$ = 0.01μF (per socket) or 0.1μF (per row) minimum

$D_1 = D_2 = D_3$ = IN4002 or equivalent (per board)

NOTES: TTL Levels 50% Duty Cycle

f_0 = 100kHz	$f_6 = f_0/64$
$f_1 = f_0/2$	$f_7 = f_0/128$
$f_2 = f_0/4$	$f_8 = f_0/256$
$f_3 = f_0/8$	$f_9 = f_0/512$
$f_4 = f_0/16$	$f_{10} = f_0/1024$
$f_5 = f_0/32$	$f_{11} = f_0/2048$

Die Characteristics

DIE DIMENSIONS:
107 x 180 x 19 mils

METALLIZATION:
Type: Aluminum
Thickness: 20kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.75 \times 10^5 A/cm^2$

GLASSIVATION:
Type: Silox
Thickness: 14kÅ ± 2.0kÅ

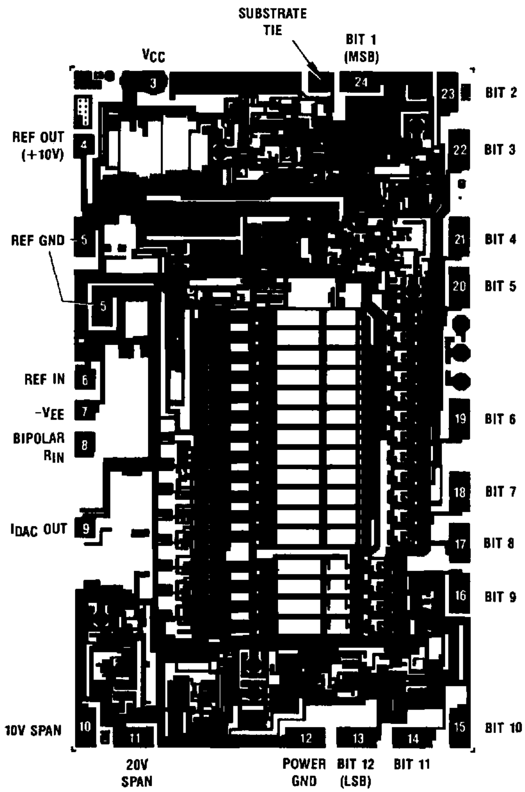
TRANSISTOR COUNT: 200

PROCESS: Bipolar-DI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Sidebraze Ceramic DIP — 460°C (Max)

Metallization Mask Layout

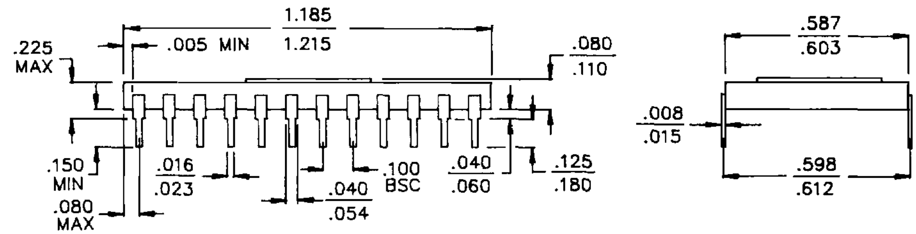
HI-565A/883



6
DATA CONVERSION PRODUCTS

Packaging†

24 PIN CERAMIC SIDEBRAZE DIP



LEAD MATERIAL: Type B
LEAD FINISH: Type C
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-3

NOTE: All Dimensions are Min/Max, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

The information contained in this section has been developed through characterization by Harris Semiconductor and is for use as application and design aid only. These characteristics are not 100% tested and no product guarantee is implied.

Definitions of Specifications

Digital Inputs

The HI-565A accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement*, or Offset Binary, (see Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	STRAIGHT BINARY	OFFSET BINARY	TWO'S COMPLEMENT*
MSB...LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	1/2 FS	Zero	-FS
111...111	+FS - 1 LSB	+FS - 1 LSB	Zero - 1 LSB
011...111	½FS - 1 LSB	Zero - 1 LSB	+FS - 1 LSB

* Invert MSB with external inverter to obtain Two's Complementing Coding

Accuracy

NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonicity; i.e., the output always increases and never decreases for an increasing input.

Settling Time

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition, settling to within 1/2 LSB of final value.

Drift

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C, -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

Power Supply Sensitivity

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

Compliance

Compliance Voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance Limit implies functional operation only and makes no claims to accuracy.

Glitch

A glitch on the output of a D/A converter is a transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches toward zero output. Matched switching times and fast switching will reduce glitches considerably.

Applying the HI-565A

Op Amp Selection

The HI-565A's current output may be converted to voltage using the standard connections shown in Figures 1 and 2. The choice of operational amplifier should be reviewed for each application, since a significant trade-off may be made between speed and accuracy.

For highest precision, use an HA-5177. This amplifier contributes negligible error, but requires about 11µs to settle within ±0.1% following a 10V step.

The Harris Semiconductor HA-2600 is the best all-around choice for this application, and it settles in 1.5µs (also to ±0.1% following a 10V step). Remember, settling time for the DAC-amplifier combination is $\sqrt{t_D2 + t_A2}$, where t_D, t_A are settling times for the DAC and amplifier.

No-Trim Operation

The HI-565A will perform as specified without calibration adjustments. To operate without calibration, substitute 50Ω resistors for the 100Ω trimming potentiometers: In Figure 1 replace R2 with 50Ω; also remove the network on pin 8 and connect 50Ω to ground. For bipolar operation in Figure 2, replace R3 and R4 with 50Ω resistors.

Typical unipolar zero will be ±1/2 LSB plus the op amp offset.

The Feedback capacitor C must be selected to minimize settling time.

Calibration

Calibration provides the maximum accuracy from a converter by adjusting its gain and offset errors to zero. For the HI-565A, these adjustments are similar whether the current output is used or whether an external op amp is added to convert this current to a voltage. Refer to Table 5 for the voltage output case, along with Figure 1 or 2.

Calibration is a two step process for each of the five output ranges shown in Table 1. First adjust the negative full scale (zero for unipolar ranges). This is an offset adjust which translates the output characteristic, i.e. affects each code by the same amount.

Next adjust positive FS. This is a gain error adjustment, which rotates the output characteristic about the negative FS value.

For the bipolar ranges, this approach leaves an error at the zero code, whose maximum value is the same as for integral nonlinearity error. In general, only two values of output may be calibrated exactly; all others must tolerate some error. Choosing the extreme end points (plus and minus full scale) minimizes this distributed error for all other codes.

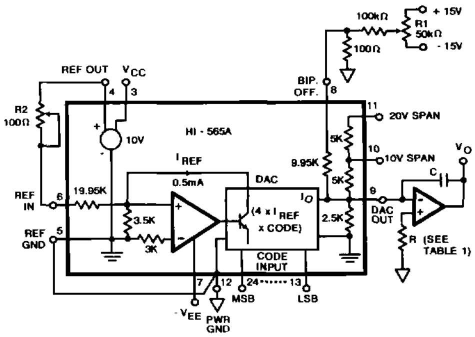


FIGURE 1. UNIPOLAR VOLTAGE OUTPUT

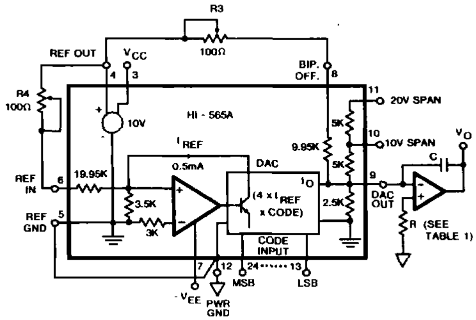


FIGURE 2. BIPOLAR VOLTAGE OUTPUT

TABLE 5. OPERATING MODES AND CALIBRATION

MODE	CIRCUIT CONNECTIONS				CALIBRATION		
	OUTPUT RANGE	PIN 10 TO	PIN 11 TO	RESISTOR (R)	APPLY INPUT CODE	ADJUST	TO SET V_O
Unipolar (See Fig. 1)	0 to +10V	V_O	Pin 10	1.43K	All 0's All 1's	R1 R2	0V +9.99756V
	0 to +5V	V_O	Pin 9	1.1K	All 0's All 1's	R1 R2	0V +4.99878V
Bipolar (See Figure 2)	±10V	NC	V_O	1.69K	All 0's All 1's	R3 R4	-10V +9.99512V
	±5V	V_O	Pin 10	1.43K	All 0's All 1's	R3 R4	-5V +4.99756V
	±2.5V	V_O	Pin 9	1.1K	All 0's All 1's	R3 R4	-2.5V +2.49878V

Other Considerations

Grounds

The HI-565A has two ground terminals, pin 5 (REF GND) and pin 12 (PWR GND). These should not be tied together near the package unless that point is also the system signal ground to which all returns are connected. (If such a point exists, then separate paths are required to pins 5 and 12).

The current through pin 5 is near-zero DC*; but pin 12 carries up to 1.75mA of code — dependent current from bits 1, 2 and 3. The general rule is to connect pin 5 directly to the system "quiet" point, usually called signal or analog ground. Then, of course, a single path must connect the analog/signal and digital/power grounds.

Layout

Connections to pin 9 (I_{OUT}) on the HI-565A are most critical for high speed performance. Output capacitance of the DAC is only 20pF, so a small change or additional capacitance may alter the op amp's stability and affect settling time. Connections to pin 9 should be short and few. Component leads should short on the side connecting to pin 9 (as for feedback capacitor C).

Bypass Capacitors

Power supply bypass capacitors on the op amp will serve the HI-565A also. If no op amp is used, a 0.01μF ceramic capacitor from each supply terminal to pin 12 is sufficient, since supply current variations are small.

*Current cancellation is a two-step process within the HI-565A in which code-dependent variations are eliminated, then the resulting DC current is supplied internally. First an auxilliary 9 bit R-2R ladder is driven by the complement of the DACs input code. Together, the main and auxilliary ladders draw a continuous 2.25mA from the internal ground node, regardless of input code. Part of this DC current is supplied by the zener voltage reference, and the remainder is sourced from the positive supply via a current mirror which is laser trimmed for zero current through the external terminal (pin 5).