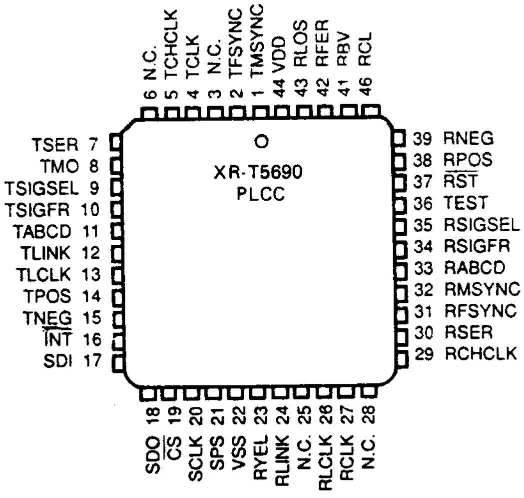
T1/ISDN Primary Rate Framer

GENERAL DESCRIPTION

The XR-T5690 is a monolithic CMOS IC designed to implement primary rate PCM (1.544 MHz) T-Carrier transmitter and receiver functions. It supports 193S framing (12 frames per superframe) and also 193E framing which is the extended superframe format (24 frames per superframe). Clear channel capability is provided by selection of appropriate zero suppression and signaling modes.

FEATURES

Single +5V Supply
Low Power CMOS Digital Technology
Single Chip DS1 Rate Transceiver
Supports 12 Frames per Superframe and 24 Frames per Superframe
B8ZS, B7 Stuffing and Transparent Zero Suppression Modes
No Host Processor for Hardware Mode
Supports Host Processor for Serial Data Transmission
Selectable 0, 2, 4, 16 State Robbed Bit Signaling Mode
Allows Mix of "CLEAR" and "NON CLEAR" DSO Channels on the same DS1 Link
Alarm Generation and Detection
Receive Error Detection and Counting for Transmission Performance Monitoring
Pin to Pin and Functionally Compatible with DS2180A



APPLICATIONS

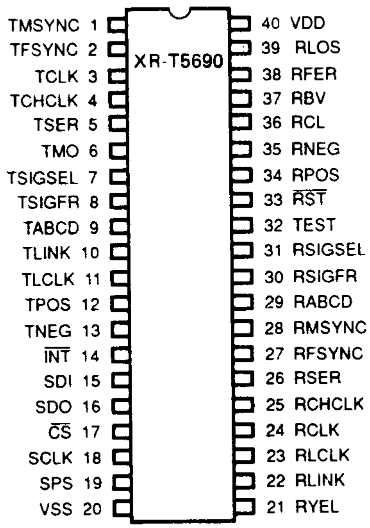
Digital Multiplexers
Channel Banks

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7V
Storage Temperature	−65°C to 150°C

ORDERING INFORMATION

Part Number	Package	Operating Temperature
XR-T5690CP	Plastic DIP	0°C to 70°C
XR-T5690CJ	PLCC	0°C to 70°C
XR-T5690IP	Plastic DIP	−40°C to 85°C
XR-T5690IJ	PLCC	−40°C to 85°C



SYSTEM DESCRIPTION

Transmitter Section

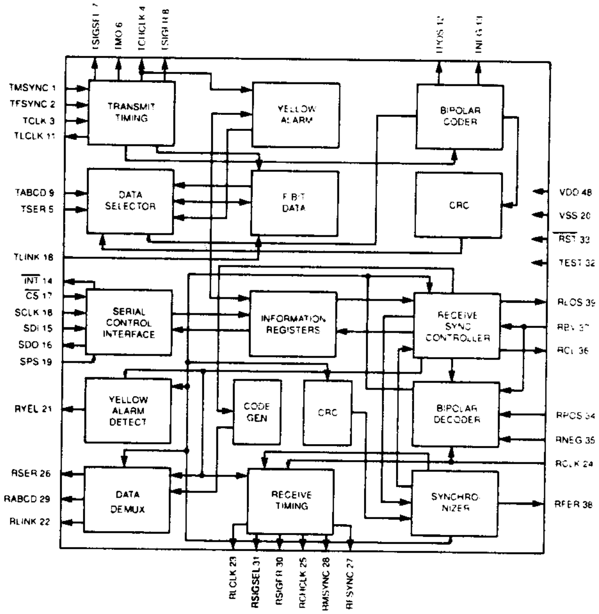
The XR-T5690 is compatible with the existing BELL system D4 (193S) framing standard described in ATT PUB 43801 and new extended superframe format (193E) as described in ATT C.B. #142. Programmable features of the XR-T5690 allows support of other framing standards which are derivatives of 193S and 193E. The salient differences between the 193S and 193E formats are the number of frames per superframe and use of the F-bit position. In 193S, 12 frames make up a superframe as opposed to 24 frames in 193E mode. Each frame consists of 24 channels of 8 bit data transmitted and received MSB first and preceded by an F-bit.

The transmit side of the XR-T5690 is made up of 6 major functional blocks: timing and clock generation, data selector, bipolar coder, yellow alarm, F-bit data and CRC block. The timing and clock generation circuit develops all on board and output system clocks from its inputs TCLK (Transmit Clock), TFSYNC (Transmit Frame Sync) and TMSYNC (Transmit Multiframe Sync). The yellow alarm circuitry generates mode dependent yellow alarms which is a repeating pattern of FF(hex) and 00(hex) on the 4KHz Facility Data Link (FDL). The CRC block generates checksum results utilized in 193E framing and the F-bit data provides mode dependent framing patterns which allow insertion of link or S-bit data externally. All of these blocks feed into the data selector, where it is possible to modify the outgoing data stream by bit selection and insertion of the transmit registers (CCR, TCR, TIR and TTR). The bipolar coder formats the output of the data selector, supports on board loopback features and inserts zero suppression codes to make it compatible with bipolar transmission techniques.

2

Receiver Section

The heart of the receiver is the synchronizer and sync monitor. This circuit serves two purposes: (A) that of monitoring the incoming data stream for loss of frame or multiframe alignment, and (B) searching for new frame alignment pattern when sync loss is detected. When sync loss is detected, the synchronizer begins an off line search for the new alignment. Whenever this occurs, all output timing signals remain at the old alignment with the exception of RSIGFR (Receive Signaling Frame), which is forced low during resync. At the instant a valid sequence is detected, the output timing will move to the new alignment at the beginning of the next multiframe. One frame later, RLOS (Receive Loss of Sync) will transition low, indicating valid sync and the resumption to the normal sync monitoring mode. Several bits in the RCR (Receive Control Register) allow tailoring of the resync algorithm by the user.



FUNCTIONAL BLOCK DIAGRAM

DC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, unless otherwise specified.

MODEL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	Supply Current		3	10	mA	Note 1,2
I_L	Input Leakage			1	µA	
I_{LO}	Output Leakage			1	µA	Note 3
I_{OH}	Output Current @2.4V	-1		+1	mA	Note 4
I_{OL}	Output Current @0.4V	-4			mA	Note 5
C_{IN}	Input Capacitance		5		pF	
C_{OUT}	Output Capacitance		7		pF	
V_{IH}	Logic 1	2		V_{DD} +0.3	V	
V_{IL}	Logic 0	-0.3		+0.8	V	

Notes:
1. TCLK = RCLK = 1.544MHz
2. Outputs Open
3. Applies to SDO when tristated
4. All outputs except INT, which is open collector
5. All outputs

AC ELECTRICAL CHARACTERISTICS -Serial Port

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, unless otherwise specified.
Measured at $V_{IH} = 2.0V$ or $V_{IL} = 0.8V$ and 10ns maximum rise and fall time.

MODEL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
t_{DC}	SDI to SCLK Set-up	50			ns	
t_{CDH}	SCLK to SDI Hold	50			ns	
t_{CD}	SDI to SCLK	50			ns	
t_{CL}	SCLK Low Time	250			ns	
t_{CH}	SCLK High Time	250			ns	
t_R, t_F	SCLK Rise & Fall			500	ns	
t_{CC}	$\overline{CS}$ to SCLK Set Up	50			ns	
t_{CCH}	SCLK to CS Hold	50			ns	
t_{CWH}	$\overline{CS}$ Inactive Time	250			ns	
t_{CDV}	SCLK to SDO Valid			200	ns	Note 1
t_{CDZ}	$\overline{CS}$ to SDO High Z			75	ns	

Notes: 1. Output load capacitance = 100pF

AC ELECTRICAL CHARACTERISTICS

Test Conditions: $T_A = 25°C$, $V_{DD} = 5V \pm 5\%$, unless otherwise specified.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
TRANSMITTER						
t_P	TLCK		648		ns	
t_{WL}, t_{WH}	TCLK Pulse Width		324		ns	
t_F, t_R	TCLK, RCLK Rise/Fall		20		ns	
t_{STD}	TSER, TABCD Set Up to TCLK Falling	50			ns	
t_{HTD}	TSER, TABCD Hold to TCLK Rising	50			ns	
t_{STL}	TLINK Set Up to TCLK Rising	50			ns	
t_{HTL}	TLINK Hold to TCLK Rising	50			ns	
t_{STS}	TFSYNC,TMSYNC Set Up to TCLK Rising	125			ns	
t_{FTS}	Propagation Delay TFSYNC to TMO, TSIGSEL,TSIGFR,TLCLK			75	ns	
t_{PTCH}	Propagation Delay TCLK to TCHCLK			75	ns	
t_{SP}	TFSYNC,TMSYNC Pulse Width	100			ns	
RECEIVER						
t_{PRS}	Propagation Delay RCLK to RMSYNC, RFSYNC, RLCLK RSIGSEL, RSIGFR, RCHCLK			75	ns	
t_{PRD}	Propagation Delay RCLK to RSER, RABCD, RLINK			75	ns	
t_{TTR}	Transition Time All Outputs			20	ns	
t_P	RCLK Period		648		ns	
t_{WL}, t_{WH}	RCLK Pulse Width		324		ns	
t_F, t_R	RCLK Rise and Fall		20		ns	
t_{PRA}	Propagation Delay RCLK to RYEL, RCL, RFER, RLOS, RBV			75	ns	
t_{RST}	RESET Pulse Width	1			µs	

PIN DESCRIPTION

Pin	Symbol	Description
1	TMSYNC	**Transmit Multiframe Sync:** May be pulsed high at multiframe boundaries to reinforce multiframe alignment, or tied low, which allows internal multiframe counter to free run.
2	TFSYNC	**Transmit Frame Sync:** Rising edge indentifies frame boundary, may be pulsed every frame to reinforce internal frame counter, or tied low (allowing TMSYNC to establish frame and multi-frame alignment).
3	TCLK	**Transmit Clock:** 1.544MHz primary clock.
4	TCHCLK	**Transmit Channel Clock:** 192KHz clock which identifies time slot boundaries. For parallel to serial conversion of channel data.
5	TSER	**Transmit Serial Data:** NRZ data input, sampled on falling edge of TCLK.
6	TMO	**Transmit Multiframe Out:** Output of internal multiframe counter, indicates multiframe boundaries. 50% duty cycle.
7	TSIGSEL	**Transmit Signaling Select:** 667Hz clock which identifies signaling frames A and C in 193E framing. 1.33KHz clock in 193S.
8	TSIGFR	**Transmit Signaling Frame:** High during signaling frames, low otherwise.
9	TABCD	**Transmit ABCD Signaling:** When enabled via TCR (bit-4), sampled during channel LSB time in signaling frames on falling edge of TCLK.
10	TLINK	**Transmit Link Data:** Sampled during the F-bit time (falling edge of TCLK) of odd frames for insertion into the outgoing data stream (193E-FDL insertion). Sampled during the F-bit time of even frames for insertion into the outgoing data (193S-External S-bit insertion).
11	TLCLK	**Transmit Link Clock:** 4KHz demand clock for TLINK input.
12	TPOS	**Transmit Bipolar +D Data Output.** Updated on rising edge or TCLK.
13	TNEG	**Transmit Bipolar -D Data Output.** Updated on rising edge of TCLK
14	$\overline{INT}$	**Receive Alarm Interrupt:** Flags host controller during alarm conditions. Active low, open drain output.
15	SDI	**Serial Data In:** Data for on-board registers. Sampled on the rising edge of SCLK.
16	SDO	**Serial Data Out:** Control and status information from on-board registers. Updated on falling edge of SCLK, and tristated duringserial port write or when $\overline{CS}$ is high.
17	$\overline{CS}$	**Chip Select:** Active low during read or write operation from or to serial port.
18	SCLK	**Serial Data Clock:** Used to read or write the serial port registers.
19	SPS	**Serial Port Select:** Tie to V_{DD} to select serial port. Tie to Vss to select hardware mode.
20	V_{SS}	**Ground.**

Pin	Symbol	Description
21	RYEL	**Receive Yellow Alarm:** Transitions high when yellow alarm is detected; goes low when alarm clears.
22	RLINK	**Receiver Link Data:**Updated with extracted FDL data one RCLK before start of odd frames (193E) and held until next update. Updated with extracted S-bit data one RCLK before start of even frames (193S) and held until next update.
23	RLCLK	**Receive Link Clock:** 4KHz demand clock for RLINK.
24	RCLK	**Receive Clock:** 1.544MHzprimary clock.
25	RCHCLK	**Receive Channel Clock:** 192KHz clock, identifies time slot (channel) boundaries.
26	RSER	**Receive Serial Data:** Received NRZ serial data, updated on rising edges of RCLK.
27	RFSYNC	**Receive Frame Sync:** Extracted 8KHz clock, one RCLK wide, indicates F-bit position in each frame.
28	RMSYNC	**Receive Multiframe Sync:** Extracted multiframe sync; edge indicates start of multiframe, 50% duty cycle.
29	RABCD	**Receive ABCD Signaling:** Extracted signaling data output valid for each channel time in signaling frames, In non-signaling frames. RABCD outputs the LSB of each channel word.
30	SIGFR	**Receive Signaling Frames:** High during signaling frames, low during resync and non-signaling frames.
31	RSIGSEL	**Receive Signaling Select:** In 193E framing a 667Hz clock which identifies signaling frames A and C. A 1.33KHz clock in 193S.
32	TEST	**Test Mode:** Tie to V_{SS} for normal operation.
33	$\overline{RST}$	**Reset:** A high to low transition clears all internal registers and resets receive side counters. A high to low to high transition will initiate a receive resync.
34	RPOS	**Receive Bipolar +D Data Input:** Sampled on falling edge of RCLK.
35	RNEG	**Receive Bipolar –D Data Input:** Sampled on falling edge of RCLK. Tie RPOS and RNEG together to receive NRZ data and disable bipolar violation monitoring circuitry.
36	RCL	**Receive Carrier Loss:** High if 32 consecutive "0's" appear at RPOS and RNEG, goes low after next "1".
37	RBV	**Receive Bipolar Violation:** High during accused bit time at RSER if bipolar violation is detected, low otherwise.
38	RFER	**Receive Frame Error:** High during F bit time when F_T, or Fs errors occur (193S), or when FPS or CRC errors occur (193E), low during resync.
39	RLOS	**Receive Loss Sync:** Indicates sync status; high when internal resync is in progress, low otherwise.
40	V_{DD}	**+5 -0V Power Supply.**

REGISTER ADDRESS SUMMARY

Register	Address	T/R[1]	Function
RSR	0000	R*	**Receive Status Register.** Reports all receive alarm conditions.
RIMR	0001	R	**Receive Interrupt Mask Register.** Allows masking of individual alarm generated interrupts.
BVCR	0010	R	**Bipolar Violation Count Register.** 8 bit preset table counter which records individual bipolar violation.
ECR	0011	R	**Error Count Register.** 2 independent 4-bit counters which record OOF occurrences, and individual bipolar violation.
CCR	0100	T/R	**Common Control Register.** Selects device operating characteristics common to receive and transmit sides.
RCR	0101	R	**Receive Control Register.** Programs device operating characteristics unique to the receive side.
TCR	0110	T	**Transmit Control Register.** Selects additional transmit side modes.
TIR1 TIR2 TIR3	0111 1000 1001	T T T	**Transmit Idle Register 1.** Designate which outgoing channels are to be substituted with idle code.
TTR1 TTR2 TTR3	1010 1011 1100	T T T	**Transmit Transparent Register 1.** Designate which outgoing channels are to be treated transparently. (No robbed bit signaling or bit 7 zero insertion.)
RMR1 RMR2 RMR3	1101 1110 1111	R R R	**Receive Mark Register 1.** Designate which incoming channels are to be replaced with idle or digital milliwatt codes (under control or RCR.)

NOTES:
1. *Transmit or receive side register*
2. *RSR is Read only register, all other registers are read/write*
3. *Reserved bit locations in the control registers should be programmed to 0, to maintain compatibility with fuure transceiver products.*

REGISTER DESCRIPTION

Receive Status Register (RSR)
Reports all receive alarm conditions

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

Symbol	Bit #	Description
BVCS	RSR.7	**Bipolar Violation Count Saturation:** Set when the 8 bit counter at BVCR saturates.
ECS	RSR.6	**Error Count Saturation:** Set when either of the 4 bit counters at ECR satu rates.
RYEL	RSR.5	**Receive Yellow Alarm:** Set when yellow alarm is detected. (Detected yellow alarm format determined by CCR bit-4 and CCR bit-3).
RCL	RSR.4	**Receive Carrier Loss:** Set when 32 consecutive "0's" appears at RPOS and RNEG.
FERR	RSR.3	**Frame Bit Error:** Set when Ft (193S) or FPs (193E) bit error occurs.
B8ZSD	RSR.2	**Change of Frame Alignment Set via CCR.6:** When CCR.6=0; detected B8ZS code word is reported at RSR.2. When CCR.6=1; COFA (Change of frame alignment) is reported when last resync resulted in change of frame or multiframe alignment.
RBL	RSR.1	**Receive Blue Alarm:** Set when 2 consecutive frames have less than 3 zeros in the data stream.
RLOS	RSR.0	**Receive Loss Sync:** Set when resync is in process; if RCR bit-1=0, RLOS transitions high on an OOF event or carrier loss, indicating auto resync.

Receive Interrupt Mask Register (RIMR)
Allows masking of individual alarm generated interupts

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVCS	ECS	RYEL	RCL	FERR	B8ZSD	RBL	RLOS

BVCS RIMR.7 **Bipolar Violation Count Saturation Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

ECS RIMR.6 **Error Count Saturation Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RYEL RIMR.5 **Receive Yellow Alarm Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RCL RIMR.4 **Receive Carrier Loss Mask:**
1 =interrupt enabled
0=interrupt disabled (masked)

FERR RIMR.3 **Frame Bit Error Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

B8ZSD RIMR.2 **B8ZS Detect Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RBL RIMR.1 **Receive Blue Alarm Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

RLOS RIMR.0 **Receive Loss of Sync Mask:**
1=interrupt enabled
0=interrupt disabled (masked)

Bipolar Violation Count Register (BVCR)
This is an 8 bit presetable counter which records individual bipolar violations.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
BVD7	BVD6	BVD5	BVD4	BVD3	BVD2	BVD1	BVD0

BVD7 BVCR.7 **MSB of Bipolar Violation Count**

BVD0 BVCR.0 **LSB of Bipolar Violation**

Error Count Register (ECR)
There are 2 independent 4 bit counters which record out-of frame occurences and CRC (Cyclic Redundancy Check) errors.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
00F3	00F2	00F1	00F0	ESF3	ESF2	ESF1	ESF0

OOFD3	ECR.7	**MSB of OOF Event Count**
OOFD0	ECR.4	**LSB of OOF Event Count**
ESFD3	ECR.3	**MSB of Extended Superframe Error Count**
ESFDO	ECR.0	**LSB of Extended Superframe Error Count**

Common Control Register (CCR)
Selects device operating characteristics common to receive and transmit sides.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0	B8ZSC	EFYA	FM	YELMD	B8ZS	B7	LPBK

0	CCR.7	This bit must be zero for proper operation.
B8ZSC	CCR.6	**B8ZS/Change of Frame Report:** 0= detected B8ZS code word is reported at RSR.2 1 = detected change of frame or multiframe alignment after last resync is reported at RSR.2
EFYA	CCR.5	**193E Yellow Alarm ModeSelect:** 0= Yellow alarm is a repeating pattern set of 00 hex and FFhex. 1= Yellow alarm is a "0" in the bit 2 position of all channels.
FM	CCR.4	**Frame Mode Select:** 0=193S, 12 frame/superframe 1=193E, 24 frame/superframe
YELMD	CCR.3	**193S Yellow Alarm Mode Select:** Determines yellow alarm type to be transmitted and detected while in 193S framing. If set, yellow alarms are a "1" in the S-bit position of frame 12; if cleared, yellow alarm is a "0" in bit-2 of all channels. Does not affect 193E yellow alarm operation.
B8ZS	CCR.2	**Bipolar Eight Zero Substitution:** 0=Disable B8ZS 1=Enable B8ZS
B7	CCR.1	**Bit Seven Zero Suppression:** If CCR bit-1=1, channels with an all zero content will be transmitted with bit-7 forced to "1". If CCR bit-1=0, no bit-7 stuffing occurs.
LPBK	CCR.0	**Loop Back:** When enabled, the device internally loops output transmit data into the incomming receive data buffers and TCLK is internally substituted for RCLK.

Receive Control Register (RCR)
Programs device operating characteristics unique to the receive side.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ARC	00FC	RCI	RCS	SYNCC	SYNCT	SYNCE	RESYNC

ARC RCR.7 **Auto Resync Criteria:**
0=Resync on 00F or RCL event
1=Resync on 00F only

00FC RCR.6 **Out-of-Frame Condition Detected:**
0=2 of 4 framing bits in error
1=2 of 5 framing bits in error

RCI RCR.5 **Receive Code Insert:**
When set, the receive code selected by RCR.4 is inserted into channels marked by RMR registers. If clear, no code is inserted.

RCS RCR.4 **Receive Code Selection:**
0=idle code (7F HEX)
1=digital milliwatt

SYNCC RCR.3 **Sync Criteria:**
Determines the type of algorithm utilized by the receiver synchronizer and differs for each frame mode.

193S Framing (CCR.4=0)
0=Synchronize to frame boundaries using F_T pattern, then search for multiframe by using F_S.
1=Cross couple F_T and F_S patterns in sync algorithm.

193E Framing (CCR.4=1)
0=Normal sync. (Fps only)
1=Validate new alignment with CRC before declaring sync.

SYNCT RCR.2 **Sync Time:**
If set, 24 consecutive F-bits of the framing pattern must be qualified before sync is declared. If clear, 10 bits are qualified.

SYNCE RCR.1 **Sync Enable:**
If clear, the transceiver will automatically begin a resync if 2 of the previous 4 framing bits were in error, or if carrier loss is detected. If set, no auto resynic occurs.

RESYNC RCR.0 **Resync:**
When toggled low to high, the transceiver will initiate resync immediately. The bit must be cleared, then set again for subsequent resyncs.

Transmit Control Register (TCR)
selects additional transmit side modes.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
ODF	FTPT	TCP	RBSE	TIS	193SI	TBL	TYEL

ODF TCR.7 **Output Data Format:**
0= Bipolar data at TPOS & TNEG
1= NRZ data at TPOS; TNEG= 0

FTPT TCR.6 **FT/FPS Pass Through:**
0= FT/FPS sourced internally
1= FT/FPS sampled at TSER during F-bit time

TCP TCR.5 **Transmit CRC Pass-Through:**
0= transmit CRC code internally generated.
1= TSER sampled at CRC F-bit time for external CRC insertion.

RBSE TCR.4 **Robbed Bit Signaling Enable:**
1= Signaling inserted in all channels during signaling frames.
0= No signaling inserted. (The TTR registers allow the user to disable signaling insertion on selected DSO channels.)

TIS TCR.3 **Transmit Idle Code Selection:**
Determines idle code format to be inserted into channels marked by the TIR registers.
0=insert 7F (hex) into marked channels.
1=insert FF (hex) into marked channels.

193S1 TCR.2 **193S S-Bit Insertion:**
Determines source of transmitted S-bit.
0=internal S-bit generator
1 =external

TBL TCR.1 **Transmit Blue Alarm:**
0=disabled
1 =enabled

TYEL TCR.0 **Transmit Yellow Alarm:**
0=disabled
1 =enabled

Transmit Idle Registers (TIR1-TIR3)
Each of these bit positions represents a DS0 channel in the outgoing frame. When set, the corresponding channel will output an idle code format determined by TCR bit-3.

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24	TIR3.7	**Channel 24 Transmit Idle Register**
CH1	TIR1.0	**Channel 1 Transmit Idle Register**

Transmit Transparency Register (TTR1-TTR3)
Each of these bit positions represents a DS0 channel in the outgoing frame. When set the corresponding channel is transparent.

TTR1	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

TTR2	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

TTR3	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24	TTR.3.7	**Channel 24 Transmit Transparent Register**
CH1	TTR1.0	**Channel 1 Transmit Transparent Register**

Receive Mark Registers (RMR)
Each of these bit positions represents a DS0 channel in the incoming T1 frame. When set the corresponding channel will output codes determined by RCR bit-4 and RCR bit-5.

RMR1	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH8	CH7	CH6	CH5	CH4	CH3	CH2	CH1

RMR2	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH16	CH15	CH14	CH13	CH12	CH11	CH10	CH9

RMR3	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
CH24	CH23	CH22	CH21	CH20	CH19	CH18	CH17

CH24	RMR3.7	**Channel 24 Receive Mark Register**
CH1	RMR1.0	**Channel 1 Receive Mark Register**

GLOSSARY

GENERAL FUNCTIONS

Line Coding

T1 line data is transmitted in a bipolar alternative mark inverted line format; ones are transmitted as alternating negative and positive pulses and zeros are simply the absence of pulses. This technique minimizes DC voltage on the T1 span and allows clock to be extracted from data. The network currently has a one's density constraint to keep clock extraction circuitry functioning, which is usually met by forcing bit-7 of any channel consisting of all 0's to 1. The use of bipolar eight zero substitution (B8ZS) satisfies the one's density requirement, while allowing data traffic to be transmitted without corruption. This feature is known as clear channel and is explained more completely in ATT C.B. #144. When the B8ZS feature is enabled, any outgoing stream of eight consecutive zeros is replaced with a B8ZS code word. If the last "1" transmitted was positive, the inserted code is 0 0 0 + – 0 – +; if negative, the code word inserted is 0 0 0 – + 0 + –. Bipolar violations occur in the fourth and seventh bit positions, which are ignored by the XR-T5690 error monitoring logic when B8ZS is enabled. Any received B8ZS code word is replaced with all "0's" if B8ZS is enabled. Also, the receiver status register will report any occurrence of B8ZS code words to the host controller. This allows the user to monitor the link for upgrade to clear channel capability, and respond to it. The B8ZS monitoring feature works at all times and is independent of the state of CCR bit-7.

F-BITS

The use of the F-bit position in 193S is split between the terminal framing pattern (known as F^T bits) which provides frame alignment information, and the signaling framing pattern (known as F^S bits) which provides multiframe alignment information (See Table 2). In 193E framing, the F bit position is shared by the framing patten sequence (FPS), which provides frame and multiframe alignment information, a 4 KHz data link known as FDL, and CRC (cyclic redundancy check) bits. The FDL bits are used for control and maintenance (inserted by the user at TLINK) and the CRC bits are an indicator of link quality and may be monitored by the user to establish error performance. (See Table 1)

SIGNALING

During frames 6 and 12 in 193S, A and B signaling information is inserted into the LSB of all channels transmitted (Table 2). In 193E, A and B data is inserted into frames 6 and 12, and C and D data is inserted into Frames 18 AND 24. This allows a maximum of 4 signaling states to be transmitted per superframe in 193S and 16 states in 193E (Table 1).

B8ZS

The XR-T5690 supports existing and emerging zero suppression formats. Selection of B8ZS coding maintains system "l's" density requirements without disturbing data integrity as required in emerging clear channel applications. B8ZS coding replaces 8 consecutive outgoing zeros with a B8ZS code word. Any received B8ZS code word is replaced with all zeros.

BIT SEVEN STUFFING

Existing systems meet one's density requirements by forcing bit 7 of all zero channels to 1. Bit 7 stuffing is "globally" enabled by asserting CCR bit-1, and may be disabled on an individual channel basis by setting appropriate bits in TTR1-TTR3.

LOOP BACK

Enabling loop back will typically induce an out of frame "OOF" condition. If appropriate bits are set in the receive control register, the receiver will resync to the looped transmit frame alignment. During the looped condition, the transmit outputs (TPOS, TNEG) will transmit unframed all "1's". All operating modes are available in loop back.

ALARMS

The XR-T5690 supports all alarm pattern generation and detection required in typical BELL system applications. These alarm modes are explained in ATT PUB 43801, ATT C.B.#142

TABLE 1
193E FRAMING FORMAT

Frame No.	F-Bit Use			Bit Use per Channel		Signaling Bit Use		
	FPS[1]	FDL[2]	CRC[3]	Data Bits	Signaling Bits[4,5]	2 State	4 State	16 State
1	-	M	-	Bits 1-8				
2	-	-	C1	Bits 1-8				
3	-	M	-	Bits 1-8				
4	0	-	-	Bits 1-8				
5	-	M	-	Bits 1-8				
6	-	-	C2	Bits 1-7	Bit 8	A	A	A
7	-	M	-	Bits 1-8				
8	0	-	-	Bits 1-8				
9	-	M	-	Bits 1-8				
10	-	-	C3	Bits 1-8				
11	-	M	-	Bits 1-8				
12	1	-	-	Bits 1-7	Bit 8	A	B	B
13	-	M	-	Bits 1-8				
14	-	-	C4	Bits 1-8				
15	-	M	-	Bits 1-8				
16	0	-	-	Bits 1-8				
17	-	M	-	Bits 1-8				
18	-	-	C5	Bits 1-7	Bit 8	A	A	C
19	-	M	-	Bits 1-8				
20	1	-	-	Bits 1-8				
21	-	M	-	Bits 1-8				
22	-	-	C6	Bits 1-8				
23	-	M	-	Bits 1-8				
24	1	-	-	Bits 1-7	Bit 8	A	B	D

Notes:
1. FPS - Framing Pattern Sequence
2. FDL - Facility Data Link (4 KHz M = Message Bits)
3. CRC - Cyclic Redundancy Check Bits
4. In case of clear channel, bit 8 will be used for data and not signaling.
5. Users can support 2 state, 4 state or 16 state signaling with the following outputs (TMO, TSIGFR, TSIGSEL, RMSYNC, RSIGFR, RSIGSEL).

TABLE 2
193S FRAMING FORMAT

Frame No.	F-Bit Use		Bit Use per Channel		Signaling
	FT[1]	FS[2]	Data Bits	Signaling Bits[4]	Bit Use
1	1	-	Bits 1-8		
2	-	0	Bits 1-8		
3	0	-	Bits 1-8		
4	-	0	Bits 1-8		
5	1	-	Bits 1-8		
6	-	1	Bits 1-7	Bit 8	A
7	0	-	Bits 1-8		
8	-	1	Bits 1-8		
9	1	-	Bits 1-8		
10	-	1	Bits 1-8		
11	0	-	Bits 1-8		
12	-	0[3]	Bits 1-7	Bit 8	B

Notes:
1. FT - Terminal Framing Bits provide frame alignment.
2. FS - Signaling Frame Bits provide multiframe alignment.
3. For clear channel, bit 8 is used for data and not signalining.
4. The S bit in frame 12 may be used for yellow alarm transmission and detection for some applications.

RECEIVER FUNCTIONS

RECEIVE CODE INSERTION

Incoming receiver channels can be replaced with idle (7F Hex) or digital milliwatt (u-LAW format) codes. The receiver mark registers indicate which channels are inserted. When set, RCR bit-5 serves as a "global" enable for marked channels, and RCR bit-4 selects inserted code format: 0=idle code, 1=digtal milliwatt.

RECEIVER SYNCHRONIZER

RCR bit-0 through RCA bit-3 allow the user to control operational characteristics of the synchronizer. Sync algorithm, candidate quality testing, auto resync, and command resync modes may be altered at any time in response to changing span conditions.

SYNC TIME

The RCR bit-2 determines the number of consecutive framing pattern bits to be qualified before SYNC is declared. If RCR bit-2 is set to "1", the algorithm will validate 24 bits; if RCA bit-2 is set to "0", 10 bits are validated. 24 bit testing results in superior false framing protection, while 10 bit testing minimizes reframe time (although in either case, the synchronizer will only establish resync when one and only one candidate is found).

RESYNC

A zero to one transition of RCR bit-0 causes the synchronizer to search for the framing pattern sequence immediately, regardless of the internal sync status. In order to initiate another resync command, this bit must be cleared and then set again.

SYNC ENABLE

When RCR bit-1 is cleared, the receiver will initiate automatic resync if any of the following events occur: A) an out of frame (OOF), or B) carrier loss (32 consecutive 0's appear at RPOS and RNEG). An OOF event occurs any time that 2 of 4 F_T or FPS bits are in error. When RCR bit-1 is set, the automatic resync circuitry is disabled; in this case, resync can only be initiated by setting RCR bit-0 to "1", or externally via a low to high transition on $\overline{RST}$. Note that using $\overline{RST}$ to initiate resync resets the receiver output timing while $\overline{RST}$ is low; use of RCR bit-1 does not affect output timing until the new alignment is located.

RECEIVER LOSS OF SYNC OUTPUT

The RLOS output of XR-T5690 indicates the status of the receiver synchronizer circuitry: when high, an off line resynchronization is in progress and a high low transition indicates resync is completed. The RLOS bit (RSR bit-0) is a "latched" version of the RLOS output. If the auto resync mode is selected (RCR bit-1=0) RLOS is a real time indication of a carrier loss or OOF event occurrence.

RESET

A high to low transition on $\overline{RST}$ clears all registers and forces immediate receive resync when $\overline{RST}$ returns high. This reset has no effect on transmit frame, multiframe, or channel counters. $\overline{RST}$ must be held low on system power up to insure proper initialization of transceiver counters and registers. Following reset, the host processor should restore all control modes by writing appropriate registers with control data.

RECEIVE SIGNALING

Robbed bit signaling data is presented at RABCD during each channel time in signaling frames for all 24 incoming channels. Logical combination of clocks RMSYNC, RSIGFR and RSIGSEL allow the user to identify and extract AB or ABCD signaling data.

TRANSMITTER FUNCTIONS

TRANSMIT BLUE ALARM

The blue alarm is an unframed, all 1's sequence enabled by asserting TCR bit-1. Blue alarm overrides all other transmit data patterns and is disabled by clearing TCR bit-1. Use of the TIR registers allows a framed, all 1's alarm transmission if required by the network.

TRANSMIT YELLOW ALARM

In 193E framing a yellow alarm is a repeating pattern set of FF (HEX) and 00 (HEX) on the 4 KHz facility data link (FDL). In 193S framing, the yellow alarm format is dependent on the state of CCR bit- 3. In all modes, yellow alarm is enabled by asserting TCR bit-0 and disabled by clearing TCR bit-0.

TRANSMIT SIGNALING

When enabled (Via TCR bit-4) channel signaling is inserted in frames 6 and 12 (193S), or 6, 12, 18 and 24 (193E) in the 8th bit position of every channel word. Signaling data is sampled at TABCD on the falling edge of TCLK during bit 8 of each input word during signaling frames. Logical combination of clocks TMO, TSIGFR and TSIGSEL allow external multiplexing of separate serial links for A, B, or A, B, C, D signaling sources.

TRANSMIT CHANNEL TRANSPARENCY

Individual DS0 channels in the T1 frame may be programmed clear by setting the appropriate bits in the transmit transparency registers. Channel transparency is required in mixed voice/data or data only environments such as ISDN, where data integrity must be maintained.

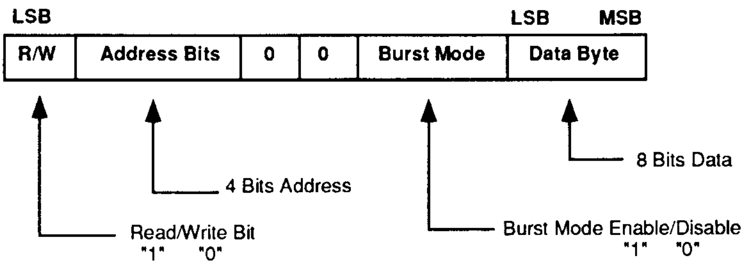


Figure 1 Serial Address /Command Format

Reading or writing the control, configuration or status registers requires writing one address/command byte prior to transferring register data. The first bit written (LSB) of the address/command word specifies register read or write. the following 4 bit nibble identifies register address. The next two bits are reserved and must be zero for proper operation. The last bit of the address/command word enables burst mode when set; the burst mode causes all registers to be consecutively written or read. Data is written to and read from the transceiver LSB first. (see Figure 1)

TRANSMIT IDLE CODE INSERTION

Individual outgoing channels in the frame can be programmed with idle code by asserting the appropriate bits in the transmit idle registers. One of the two idle code formats, 7F (Hex) and FF (Hex) may be selected by the user via TCR bit-3. If enabled, robbed bit signaling data is inserted into the idle channel, unless the appropriate TTR bit is set for that channel. This feature eliminates extenal hardware currently required to intercept and stuff unoccupied channels in the DS1 bit stream.

SERIAL CONTROL INTERFACE

(See Figure 1 on previous page)

SERIAL PORT

Pin 14 through 18 of the XR-T5690 serve as a microprocessor or microcontroller compatible serial port. Sixteen on board registers allow the user to update operational characteristics and monitor device status via a host controller, minimizing hardware interfaces. Port read/write timing is unrelated to the system transmit and receive timing, allowing asynchronous read and/or writes by the host.

CHIP SELECT AND CLOCK CONTROL

All data transfers are initiated by driving the $\overline{CS}$ input low. Input data is latched on the fishing edge of SCLK and must be valid during the previous low period of SCLK to prevent momentary corruption of register data during writes. Data is output on the falling edge of SCLK and held to the next falling edge. All data transfers are terminated if the $\overline{CS}$ input transitions high. Port control logic is disabled and SDO is tristated when $\overline{CS}$ is high.

DATA I/O

Following the 8 SCLK cycles that input an address/command byte to write, a data byte is strobed into the addressed register on the rising edge of the next 8 SCLK cycles. Following an address/command word to read, contents of the selected register are output on the falling edge of the next 8 SCLK cycles. The SDO pin is tristated during device write, and may be tied to SDI in applications where the host processor has a bidirectional I/O pin.

BURST MODE

The burst mode allows all on board registers to be consecutively read or written by the host processor. A burst read is used to poll all registers; RSR contents will be unaffected. This feature minimizes device initialization time on power up or system reset. Burst mode is initiated when ACB bit-7 is set and the address nibble is "0000". Burst is terminated by low to high transition on $\overline{CS}$.

HARDWARE MODE

For preliminary system prototyping or applications which do not require the features offered by the serial port, the transceiver can be reconfigured by the SPS pin. Tying this pin to Vss disables the serial port, clears all internal registers except CCR, TCR and redefines pins 14 through 18 as mode control inputs. The hardware mode allows device retrofit into existing applications where mode control and alarm conditioning hardware is often designed with discrete logic.

HARDWARE COMMON CONTROLS

In the hardware mode TCR bit-2, CCR bit-4, TCR bit-0, CCR bit-1 and CCR bit-2 map to pins 14 through 18. The loopback feature (CCR bit-0) is enabled by tying pins 17 (zero suppression) and 18 (B8ZS) to 1. (The last states of pins 17 and 18 are latched when both pins are taken high, preserving the current zero suppression mode). Robbed bit signaling (TCR bit-4) is enabled for all channels. The user may tie TSER to TABCD externally to disable signaling if so desired. CCR bit-3 is forced to 0, which selects yellow alarm bit- 2 in 193S framing. Contents of the RCR, as well as the remaining bit locations in the CCR and TCR, are cleared in hardware mode. The $\overline{RST}$ input may be used to force immediate receiver resync, and has no effect on transmit.

ALARMS

ALARM OUTPUTS

The transceiver provides direct alarm outputs for applications when additional decoding and demuxing are required to supplement the on board alarm logic.

YELLOW ALARM OUTPUT

The RYEL output of XR-T5690 will go high when a yellow alarm is detected. A high to low transition indicates the alarm condition has been cleared. The RYEL bit (RSR bit-5) is a "latched" version of the RYEL output. In 193E framing, the yellow alarm pattern detected is 16 pattern sets of 00 HEX and FF HEX received at RLINK or a "O" in the bit 2 position of all channels. In 193S framing the yellow alarm format is dependent on CCR bit-3: if CCR bit-3=0, the RYEL output transitions high if bit 2 of 156 or more consecutive channels is 0; if CCR bit-3=1, yellow alarm is detected when the S- bit received in frame 12 is 1.

BIPOLAR VIOLATION OUTPUT

The RBV output transitions high when accused bit emerges at RSER. RBV will go low at the next bit time if no additional violations are detected.

RECEIVE FRAME OUTPUT

The receive frame error output transitions high at the F-bit time and is held high for two bit periods when a frame bit error occurs. In 193S framing F^T and F^S patterns are tested. The FPS pattern is tested in 193E framing. Additionally, in 193E framing, RFER reports a CRC error by a low to high to low transition (one bit period wide) one half RCLK period before a low to high transition on RMSYNC.

RECEIVE ALARM REPORTING

Incoming serial data is monitored by the transceiver for alarm occurrence. Alarm conditions are reported in two ways: via transitions on the alarm output pins and registered interrupt. Interrupts may be direct, in which case the transceiver demands service for a real time alarm, or count overflow triggered, in which case an on board alarm event counter exceeds a user-programmed threshold. The user may mask individual alarm conditions by clearing the appropriate bits in the receive interrupt mask register.

ALARM SERVICING

The host controller must service the transceiver in order to clear an interrupt condition. Clear appropriate bits in the RIMR will unconditionally clear an interrupt. Direct interrupt will be cleared when the RSR is read, unless the alarm condition still exists. Count overflow interrupts will be conditionally cleared by reading the RSR; the next event will trigger interrupt unless the user presents the appropriate count register.

COUNTERS

ALARM COUNTERS

The three on board alarm event counters allow the transceiver to monitor and record error events without processor intervention on each event occurrence. All of these counters are presentable by the user, establishing an event count interrupt threshold. As each counter saturates, it will set a bit in RSR and generate an interrupt unless masked. The user may read these registers at any time; in many systems, the host will periodically poll these registers to establish link error rate performance.

OOF EVENTS AND ERRORED SUPERFRAMES

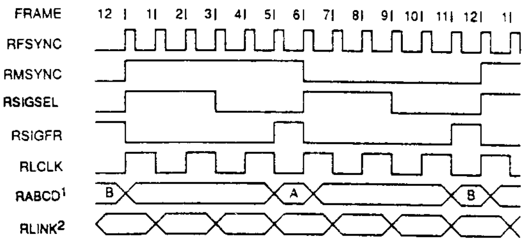
Out of frame is declared when two of four consecutive framing bits are in error. F_T bits are tested for OOF occurrence in 193S; the FPS bits are tested in 193E. OOF events are recorded by the 4 bit OOF counter in the error count register. In the 193E framing mode, the OOF event is logically "OR'ed" with an on chip generated CRC checksum. This event, known as errored superframe, is recorded by the 4 bit ESF error counter in the error count register. In the 193S framing mode, the 4 bit ESF error counter records individual F_T and F_S errors when RCR bit-3=1, or F_T errors only when RCR bit-3=0.

BIPOLAR VIOLATION COUNTER

This 8 bit binary up counter saturates at 255 and will generate an interrupt for each occurrence of a bipolar violation (RIMR bit-7=1). Presetting this register allows the user to establish specific count interrupt thresholds. The counter will count "UP" to saturation from the preset value, and may be read at any time. Counter increments occur at all times and are not disabled by resync.

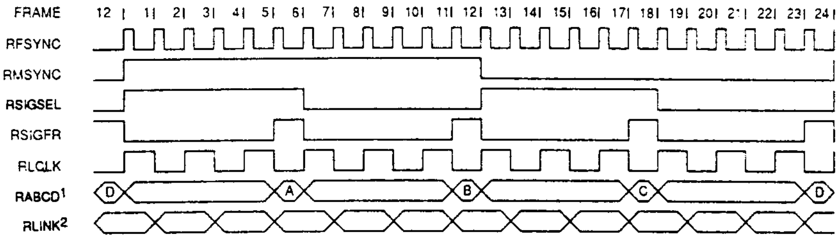
OOF AND ESF ERROR COUNTERS

These separate 4-bit binary up counters saturate at a count of 15 and will generate an interrupt for each occurrence of an OOF event or an ESF error event after saturation (RIMR bit-6=1). Presetting these counters allows the user to establish specific count interrupt thresholds. The counter will count "UP" to saturation from the present value, and may be read at any time. These counters share the same register address, and must be written to or read from simultaneously. The OOF counter records out of frame events in both 193S and 193E. The ESF error counter records errored superframes in 193E. In 193S the ESF counter records individual F_T and F_S errors when RCR bit-3=1; F_T errors only when RCR bit-3=0. ECR counter increments are disabled when resync is in progress (RLOS high).



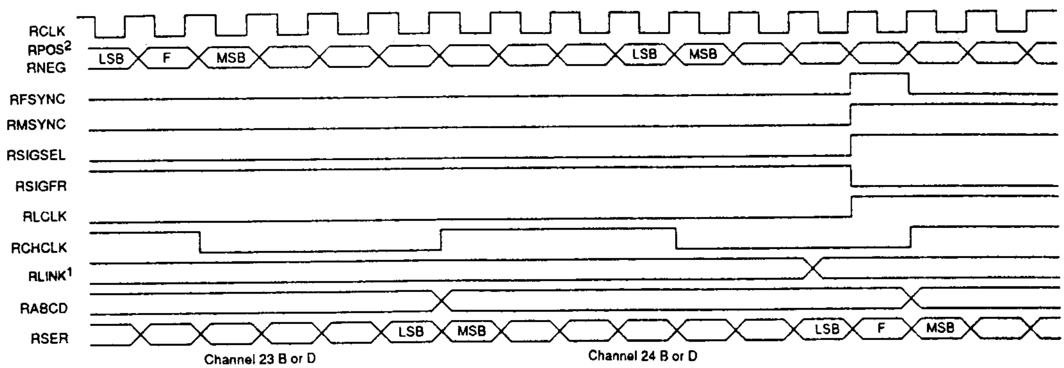
Note:
1. Signaling data is undated during signaling frames or channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (S-bit) is updated one bit time prior to S-bit frames and held for two frames.

193S Receive Multiframe Timing



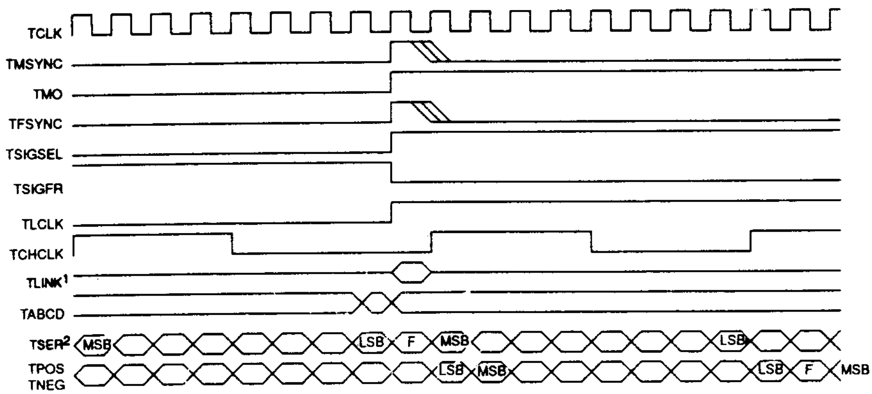
Note:
1. Signaling data is updated during signaling frames on channel boundaries. RABCD is the LSB of each channel word in non-signaling frames.
2. RLINK data (FDL-bit) is updated one bit-time prior to S-bit frames and held for two frames.

193E Receive Multiframe Timing



Note:
1. RLINK timing is shown for 193E; in 193S RLINK is updated on even frame boundaries and is held across multiframe edges.
2. Total delay from RPOS and RNEG output is 13 clock periods.

Receive Multiframe Boundary Timing

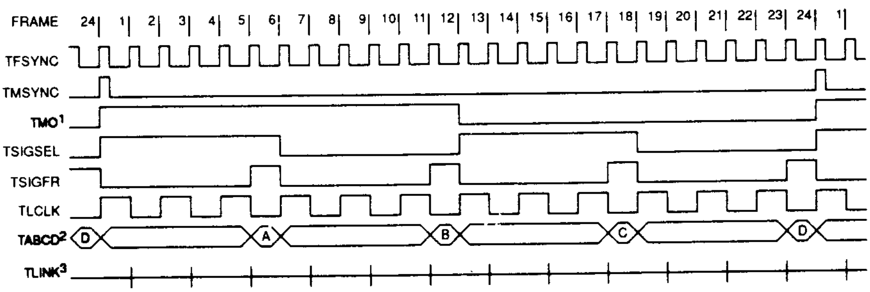


Note:

1. TLINK timing shown is for 193 E framing; where TLINK is a sampled as shown for insertion into F bit position of cold frames. When S-bit insertion is enabled in 193S. TLINK is sampled during even frames.

2. If TCR bit S=1; TSER is sampled during the F-bit time of CRC frames for insertion into the ougoing data stream (193E Framing only).

Transmit Multiframe Boundry Timing



Notes:

1. Establishing frame and multiframe:

a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries.

b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNC once establishes multiframe boundaries.

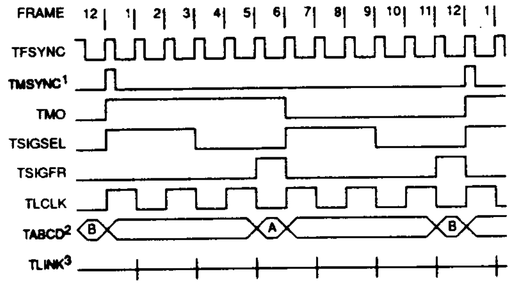
c) TMSYNC and TFSYNC may be continously pulsed to establish and reinforce frame and superframe timing.

d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitary multiframe boundary as indicated by TMO.

2. Channels with Robbed Bit Signaling enabled will sample TABCD during the LSB bit time in the frames indicated

3. TLINK is sampled during the F-Bit time of odd frames and inserted into the outgoing data stream (FDL data).

103E Transmit Multiframe Timing



Notes:

1. Establishing frame and multiframe:

a) With TFSYNC tied low, TMSYNC may be pulsed high once every multiframe period to establish multiframe boundaries.

b) TFSYNC may be pulsed every 125 microseconds; pulsing TMSYNBC once establishes multiframe boundaries.

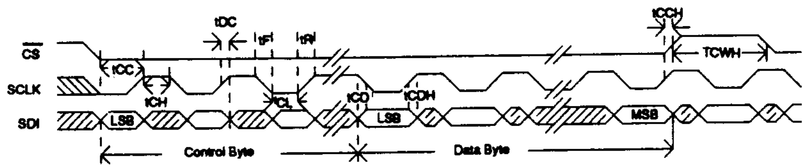
c) TMSYNC and TFSYNC may be continously pulsed to establish and reinforce frame and superframe timing.

d) If TMSYNC is tied low and TFSYNC is pulsed at frame boundaries, the transmitter will establish an arbitrary multiframe boundary as indicated by TMO.

2. Channels with Robbed Bit Signaling enabled will sample TABCD during the LSB bit time in the frames indicated.

3. When external S-bit insection is enabled. TLINK will be sampled during the F-Bit time of even frames and inserted into the outgoing data stream.

193S Transmit Multiframe Timing

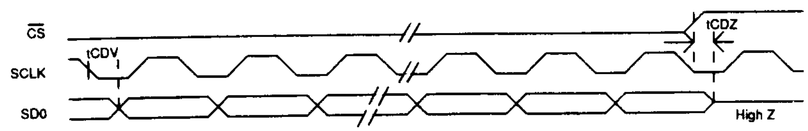


Notes:

1. Data byte must be valid across low clock periods to prevent transients in operating modes.

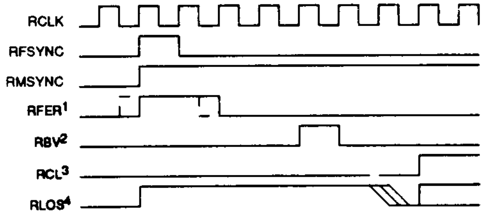
2. The shaded regions are don't care states of input data.

Serial Port Write AC Timing



Notes: 1. Serial port write must precede a port read to provide address information.

Serial Port Read[1] AC Timing



Note:

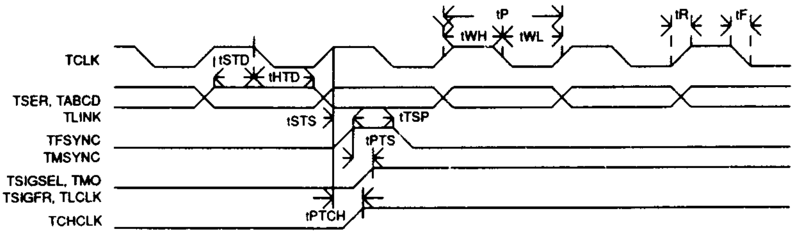
1. RFER goes high during F-Bit if framing pattern is in error (Figure 12 F-bits are ignored if CCR bit 3=1). Also, in 193E Format, RFER transitions half a bit period before the rising edge of RMSYNC to indicate a CRC error.

2. RBV indicates received bipolar violations and transitions high together with the accused bit on RSER. If B8Zs is enabled RBV does not report the zero replacement code.

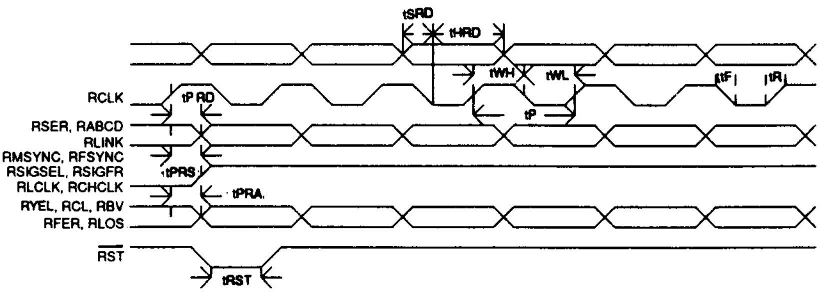
3. RCL transitions high after 32 consecutive "0" bits are received. It goes low when the next "1" is received.

4. RLOS transitions high during the F-bit time that caused the OOF event if autoresync mode is selected (RCR-1 = 0)(2 out of 4 consecutive F-T or FPS bits are in error). Resync will also occur when loss of carrier is detected (RCL = 1). When RCR 1=1 RLOS remains low until resync occurs, regardless of OOF carrier loss flags. In this situation, resync is initiated only when RCR-0 transitions low to high or RST pin transitions, high to low to high.

Alarm Output Timing



Transmit AC Timing



Receive AC Timing