Ordering number : EN7336

Discontinued

SANYO Semiconductors

DATA SHEET

LA6564H — Monolithic Linear IC For CD-R Four-Channel Bridge (BTL) Driver

Overview

The LA6564H is a 4-channel bridge (BTL) driver for CD-R.

Functions

- Three power supply systems (with a separate preamplifier stage)
- Bridge-connection (BTL) POWER AMP 4CH built-in.
- I_O max 1A
- Mute circuit (output ON/OFF) built-in. With three systems (2-1-1)
- With output voltage setting pin (for 4CH only)

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC} max	*1	14	V
Supply voltage 2	VS max	*1	14	V
Allowable power dissipation	Pd max	Independent IC	0.82	W
		A designated substrate*	2	W
Maximum input voltage	$V_{IN}B$		13	V
MUTE pin voltage	VMUTE		13	V
Maximum output current	I_O max	Each output	1	A
Operating temperature	Topr		-30 to +85	°C
Storage temperature	Tstg		-55 to +150	°C

* Specified board size : 114.3×76.1×1.6mm^3, glass epoxy.

1 Note : $V_{CC} \geq VS$

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage 1	V_{CC}	V_{CC} *1	4 to 13.5	V
Supply voltage 2	VS	VS1, 2, 3 *1	4 to 13.5	µA

1 Note : $V_{CC} \geq VS$

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Electrical Characteristics at Ta = 25°C, V_{CC} = 12V, VS1 = VS2 = 5V, VS3 = 12V, VREF = 1.65V, unless especially specified.

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Overall						
V_{CC} No-load current drain	I_{CC}-ON	V_{CC} current, all outputs ON (all MUTE H)		20	30	mA
No-load current drain OFF	I_{CC}-OFF	Total current of V_{CC} and VS1 through 3 (All MUTE : L)			0.5	mA
Output AMP Block						
Output offset voltage	V_{OFF}	Between + and – outputs of each CH	-50		50	mV
Output voltage 1	V_O1	R_L=8Ω. Voltage between outputs of CH1 through CH3 *1	4	4.5		V
Output voltage 2	V_O2	R_L=16Ω. Voltage between outputs of CH4 *1	10.5	11		V
Closed-circuit voltage gain 1	VG1	Input and output gain	10	12	14	dB
Closed-circuit voltage gain 2	VG2	Input and output gain	16	18	20	dB
Input voltage range	V_{IN}	Each input pin	0		VS*	V
Slew rate	SR	AMP Independent Multiply 2 between outputs.		0.5		V/µs
MUTE block						
MUTE ON voltage	VMUTE-ON	MUTE *2	2			V
MUTE OFF voltage	VMUTE-OFF	MUTE *2			0.5	V
MUTE pin inrush current	I-MUTE	Inrush current of each MUTE pin		25	50	µA
VREF AMP block						
VREF-IN input voltage range			1		V_{CC}-1.5	V
Voltage limiter block (Setting the limit value of CH4 output voltage)						
V_O-SET input and output gain	G-V_OSET	*1	11	12	13	dB
V_O-SET input current	I-V_OSET	V_O-SET : Current at 3.3 V			1	µA

Note *1 : Output saturated.

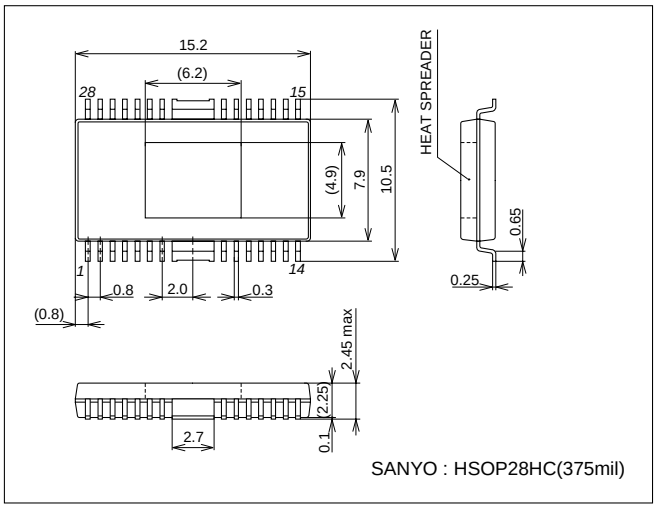
*2 : MUTE output ON with HI and OFF with LOW (High impedance with AMP output OFF)

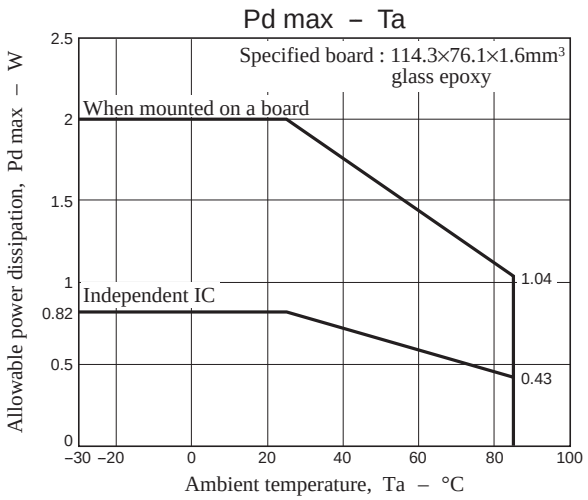
MUTE operates independently for each CH. (Refer to “Relationship of MUTE and output” described below)

Package Dimensions

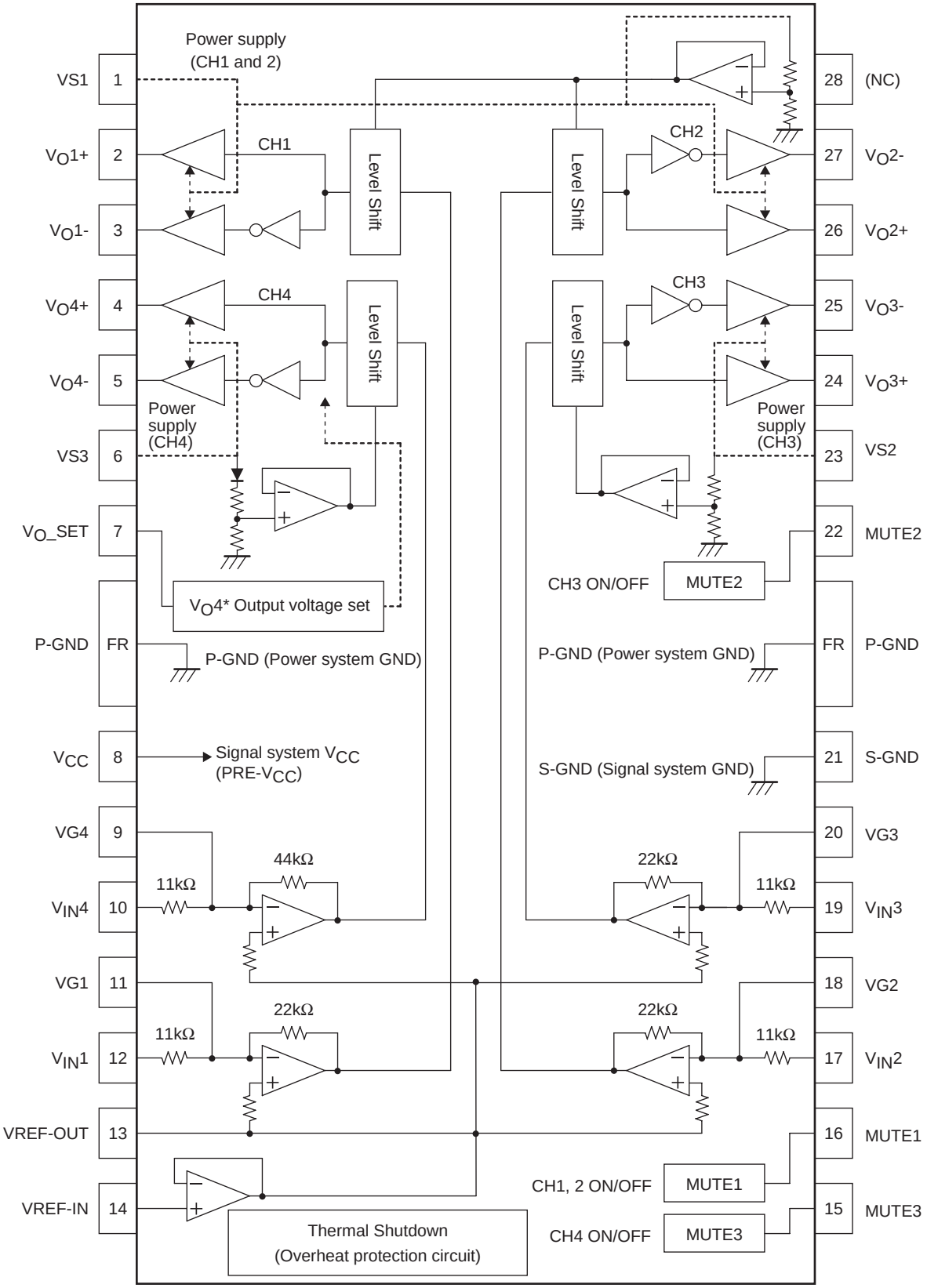
unit : mm (typ)

3234B





Block Diagram

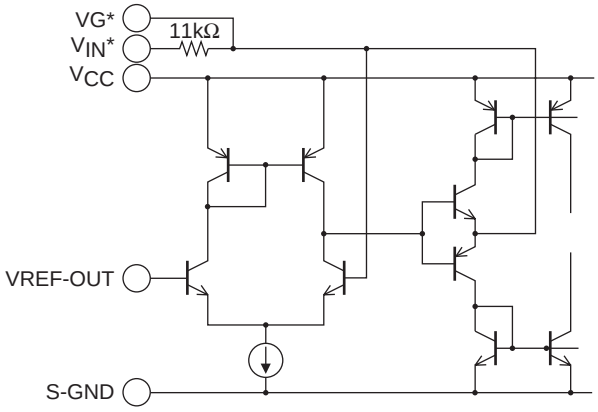
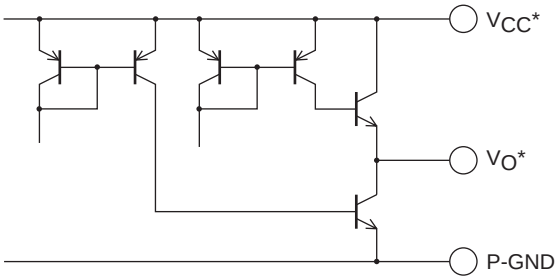
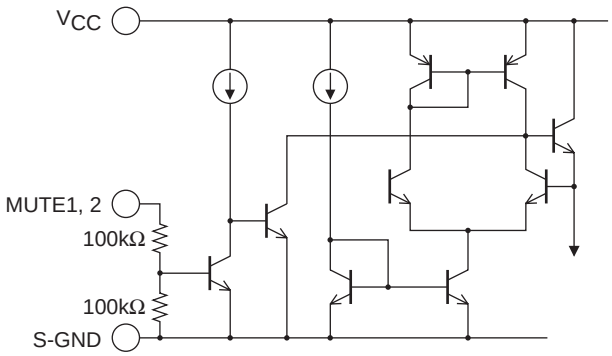


Pin Functions

Pin No.	Symbol	Pin descriptions
1	VS1	Output stage power supplies for channel 1 and 2
2	V_O1+	Output pin (+) for channel 1, non-inverted output for channel 1 input
3	V_O1-	Output pin (-) for channel 1, inverted output for channel 1 input
4	V_O4+	Output pin (+) for channel 4, non-inverted output for channel 4 input
5	V_O4-	Output pin (-) for channel 4, inverted output for channel 4 input
6	VS3	Output stage power supply for channel 4
7	V_O_SET	Pin to adjust channel 4 output voltage
8	V_{CC}	Power supply for preamplifier stage signal system
9	VG4	Input pin for channel 4 (for gain adjustment)
10	$V_{IN}4$	Input pin for channel 4
11	VG1	Input pin for channel 1 (for gain adjustment)
12	$V_{IN}1$	Input pin for channel 1
13	VREF-OUT	VREF-AMP output
14	VREF-IN	Reference voltage input pin
15	MUTE3	ON/OFF for channel 4 output
16	MUTE1	ON/OFF for channel 1 and 2 outputs
17	$V_{IN}2$	Input pin for channel 2
18	VG2	Input pin for channel 2 (for gain adjustment)
19	$V_{IN}3$	Input pin for channel 3
20	VG3	Input pin for channel 3 (for gain adjustment)
21	S-GND	Signal system GND
22	MUTE2	ON/OFF for channel 3 output
23	VS2	Output stage power supply for channel 3
24	V_O3+	Output pin (+) for channel 3, non-inverted output for channel 3 input
25	V_O3-	Output pin (-) for channel 3, inverted output for channel 3 input
26	V_O2+	Output pin (+) for channel 2, non-inverted output for channel 2 input
27	VG2	Output pin (-) for channel 2, inverted output for channel 2 input
28	(NC)	Do not use

Note : Center frame (FR) becomes GND for the power system (P-GND). Set this to the minimum potential together with S-GND.

Pin Description

Pin No.	Symbol	Pin function	Description	Equivalent circuit
12 17 19 10 11 18 20 9	$V_{IN}1$ $V_{IN}2$ $V_{IN}3$ $V_{IN}4$ VG1 VG2 VG3 VG4	Input	Each input pin	
2 3 26 27 24 25 4 5	V_O1+ V_O1- V_O2+ V_O2- V_O3+ V_O3- V_O4+ V_O4-	Output	Each output pin	
16 22 15	MUTE1 MUTE2 MUTE3	MUTE	ON/OFF for each channel output MUTE : H output ON MUTE : L output OFF	

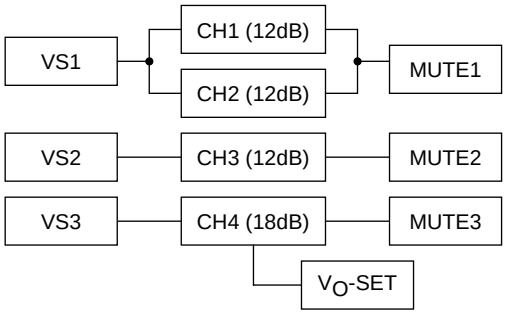
Relation of MUTE and output

	Output			
	CH1	CH2	CH3	CH4
Each MUTE	MUTE1		MUTE2	MUTE3
H	ON			
L	OFF			

*1 The output becomes HI impedance when it is OFF.

*2 MUTE operates independently for each CH. (Refer to the following description). All MUTES enter the STBY mode when they are L (output OFF), turning OFF all of circuits including the output AMP.

Relationship between each CH and V*, MUTE



V_O-SET

V_O-SET operates for CH4. V_O-SET is correlated to CH4 output by 12dB. For example, the output is 4V when V_O-SET is 1V.

Gain set (V_{IN}* and VG*)

Gain of each CH can be equivalently represented as follows :

- CH1 to CH3:12dB, CH4 : 18dB when only V_{IN} pin is used. The similar gain is obtained also when a 11k resistor is used for the VG* pin and the input is provided from its resistor end.
- The input/output gain is determined from the resistance ratio as shown in the figure below. To set the gain with the VG pin, the input-output gain has a slight temperature characteristic depending on the difference in temperature characteristic between internal and external resistances.